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Vishay Siliconix

## Automotive Dual N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	100		
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0255		
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0325		
I <sub>D</sub> (A) per leg	30		
Configuration	Dual		
Package	PowerPAK SO-8L		

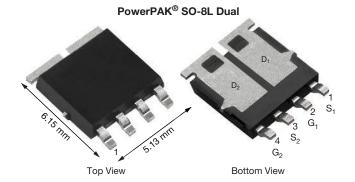
#### **FEATURES**

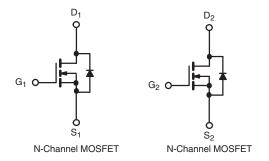
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912





ROHS COMPLIANT HALOGEN FREE





<b>ABSOLUTE MAXIMUM RATING</b>	<b>S</b> ( $T_C = 25$ °C, unles	s otherwise noted	d)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	100		
Gate-Source Voltage		V <sub>GS</sub>	± 20	V	
Continuous Drain Current	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	30		
	T <sub>C</sub> = 125 °C		17		
Continuous Source Current (Diode conduction) <sup>a</sup>		I <sub>S</sub>	30	А	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	65		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	22		
Single Pulse Avalanche Energy	L = U.I IIII	E <sub>AS</sub>	25	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	В	48	W	
	T <sub>C</sub> = 125 °C	P <sub>D</sub>	16		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering Recommendations (Peak temperature) d, e			260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient F	PCB Mount c	R <sub>thJA</sub>	85	°C/W	
Junction-to-Case (Drain)		R <sub>thJC</sub>	3.1	C/VV	

#### **Notes**

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TES	TEST CONDITIONS		TYP.	MAX.	UNIT
Static		•					ı
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		100	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		2.0	2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V	-	-	1	
	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V, T <sub>J</sub> = 125 °C	-	-	50	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V, T <sub>J</sub> = 175 °C	-	-	150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	15	-	-	Α
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A	-	0.0210	0.0255	
	В	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A, T <sub>J</sub> = 125 °C	-	-	0.0426	Ω
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A, T <sub>J</sub> = 175 °C	-	-	0.0539	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 8 A	-	0.0270	0.0325	
Forward Transconductance b	9fs	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		-	27	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>		V <sub>DS</sub> = 25 V, f = 1 MHz	-	785	1050	pF
Output Capacitance	Coss	$V_{GS} = 0 V$		-	405	550	
Reverse Transfer Capacitance	$C_{rss}$			-	30	50	
Total Gate Charge <sup>c</sup>	$Q_g$			-	15	30	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	V <sub>GS</sub> = 10 V	$V_{DS} = 50 \text{ V}, I_{D} = 5 \text{ A}$	-	3	1	nC
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	3	-	
Gate Resistance	$R_g$	f = 1 MHz		0.65	1.41	2.20	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	10	20	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, \text{ R}_L = 10 \Omega$ $I_D \cong 5 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 10 \Omega$		-	5	10	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	20	40	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	5	10	
Source-Drain Diode Ratings and Chara	cteristics <sup>b</sup>						
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	65	Α
Forward Voltage	$V_{SD}$	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V		-	0.87	1.2	V

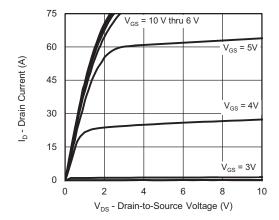
### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

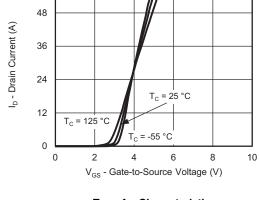
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

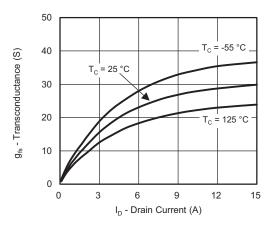


#### **Output Characteristics**

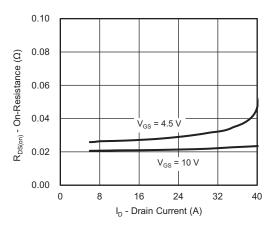


60

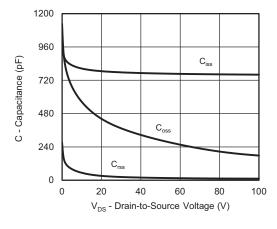
**Transfer Characteristics** 



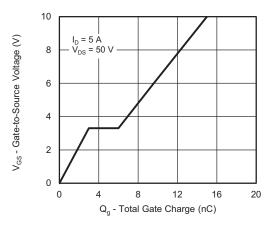
Transconductance



On-Resistance vs. Drain Current



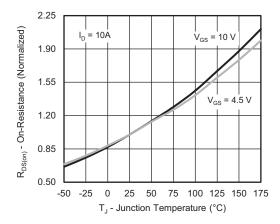
Capacitance



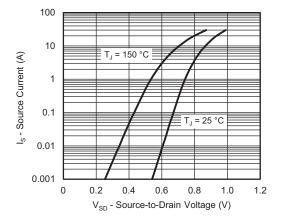
**Gate Charge** 



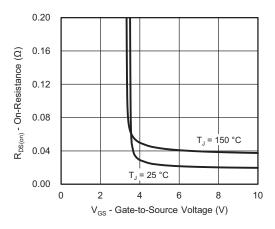
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



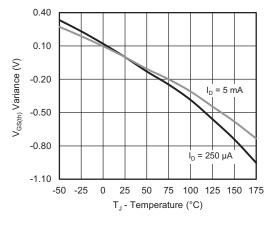
On-Resistance vs. Junction Temperature



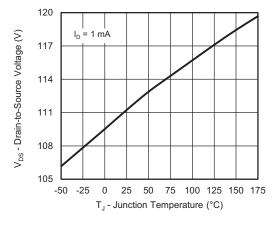
**Source Drain Diode Forward Voltage** 



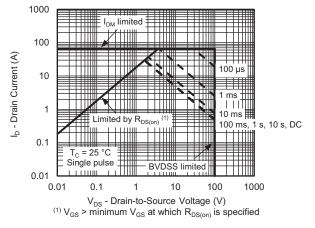
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



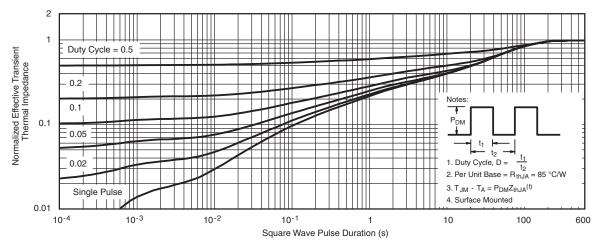
**Drain Source Breakdown vs. Junction Temperature** 



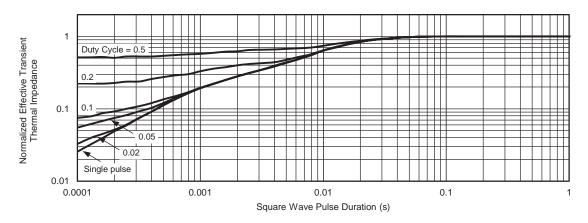
Safe Operating Area



## THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on ac

tual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?78092">www.vishay.com/ppg?78092</a>.





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