SiT8003XT

Low Power Ultra Thin Oscillator

SiTime™ It's About Time

Features, Benefits and Applications

- The world's thinnest oscillator, 0.25 mm (typical) height
- Typical current consumption of 3.2 mA in active mode
- 1 - 110 MHz frequency range
- LVCMOS/LVTTL compatible output
- Standby current as low as 0.5 µA
- Fast resume time of 3.0 ms typical
- Standby or output enable modes
- Outstanding mechanical robustness for portable applications
- All-silicon device with outstanding reliability of 2 FIT (10x improvement over quartz-based devices), enhancing system mean-time-to-failure (MTBF)
- Ultra short lead time
- Ideal for ultra thin applications: High Capacilty (HC) SIM cards, Smart cards, Near Field Communications (NFC), SD cards, multi-chip modules (MCM) and System-in-Package (SiP)

Specifications

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	–	110	MHz	
Frequency Tolerance	F_tol	-100	–	+100	PPM	Inclusive of: Initial stability, operating temperature, rated power, supply voltage change, load change, shock and vibration.
Aging	Ag	–1.0	–	1.0	PPM	1st year at 25°C
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	3.7	4.1	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	3.2	3.5	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
Standby Current	I_std	–	2.4	4.3	µA	$\overline{ST}$ = GND, Vdd = 3.3 V, Output is Weakly Pulled Down
		–	1.2	2.2	µA	$\overline{ST}$ = GND, Vdd = 2.5 or 2.8 V, Output is Weakly Pulled Down
		–	0.4	0.8	µA	$\overline{ST}$ = GND, Vdd = 1.8 V, Output is Weakly Pulled Down
Duty Cycle	DC	45	50	55	%	All Vdds. f <= 75 MHz
		40	50	60	%	All Vdds. f > 75 MHz
Rise/Fall Time	Tr, Tf	–	1	2	ns	20% - 80% Vdd=2.5 V, 2.8 V or 3.3 V, 15 pf load
		–	1.3	2.5	ns	20% - 80% Vdd=1.8V , 15p f load
Output Voltage High	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.3 V) IOH = -3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA (Vdd = 1.8 V)
Output Voltage Low	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.3 V) IOL = 3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOL = 2 mA (Vdd = 1.8 V)
Output Load	Ld	–	–	15	pF	At maximum frequency and supply voltage. Contact SiTime for higher output load option
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Startup Time	T_osc	–	–	10	ms	Measured from the time Vdd reaches its rated minimum value
Resume Time	T_resume	–	3.0	3.8	ms	Measured from the time ST pin crosses 50% threshold
RMS Period Jitter	T_jitt	–	–	4.0	ps	f = 75 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	–	5.5	ps	f = 75 MHz, Vdd = 1.8 V
RMS Phase Jitter (random)	T_phj	–	0.6	–	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz, VDD = 2.5 V, 2.8 V, or 3.3 V
		–	0.8	–	ps	f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz, VDD = 1.8 V

■ Specifications (Cont.)

Pin Description Tables

Pin #1 Functionality
OE
H or Open[1]: specified frequency output
L: output is high impedance
$\overline{ST}$
H or Open: specified frequency output
L: output is low level (weak pull down) Oscillation stops

Pin Map	
Pin	**Connection**
1	OE/$\overline{ST}$
2	GND
3	CLK
4	VDD

Absolute Maximum Ratings

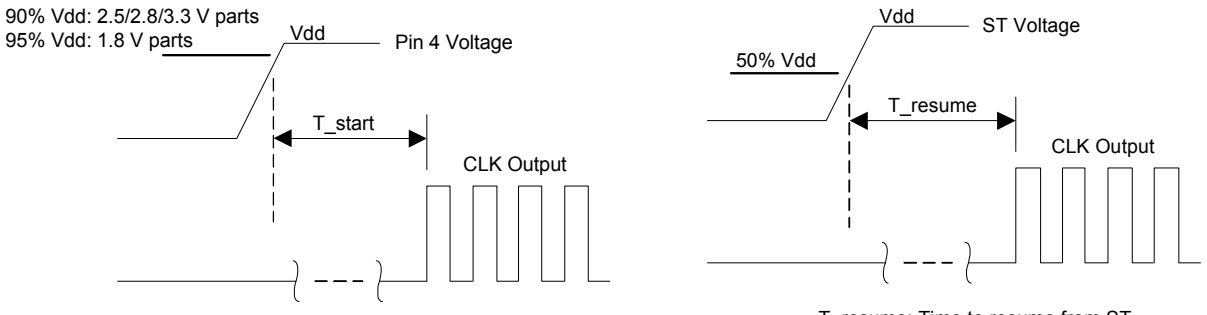
Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	6000	V
Theta JA (with copper plane on VDD and GND)	–	75	°C/W
Theta JC (with PCB traces of 0.010 inch to all pins)	–	24	°C/W
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125°C, Process, VDD (0 to 3.65 V)	1,000+	–	years

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensibility Level	MSL1 @ 260°C

Startup and Resume Timing Diagram

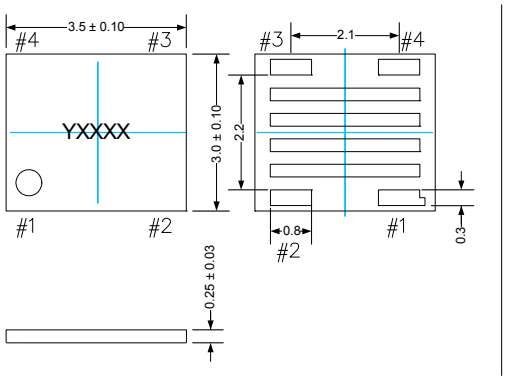
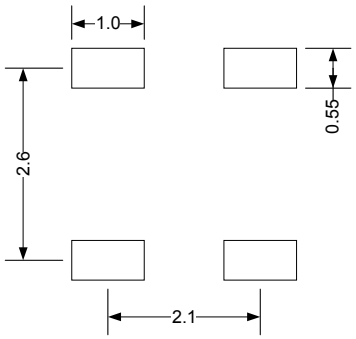


T_start: Time to start from power-off
(ST/OE Mode)

T_resume: Time to resume from ST
(ST Mode Only)

Note:
1. In 1.8 V mode, a resistor of <100 kΩ between OE pin and VDD is recommended.

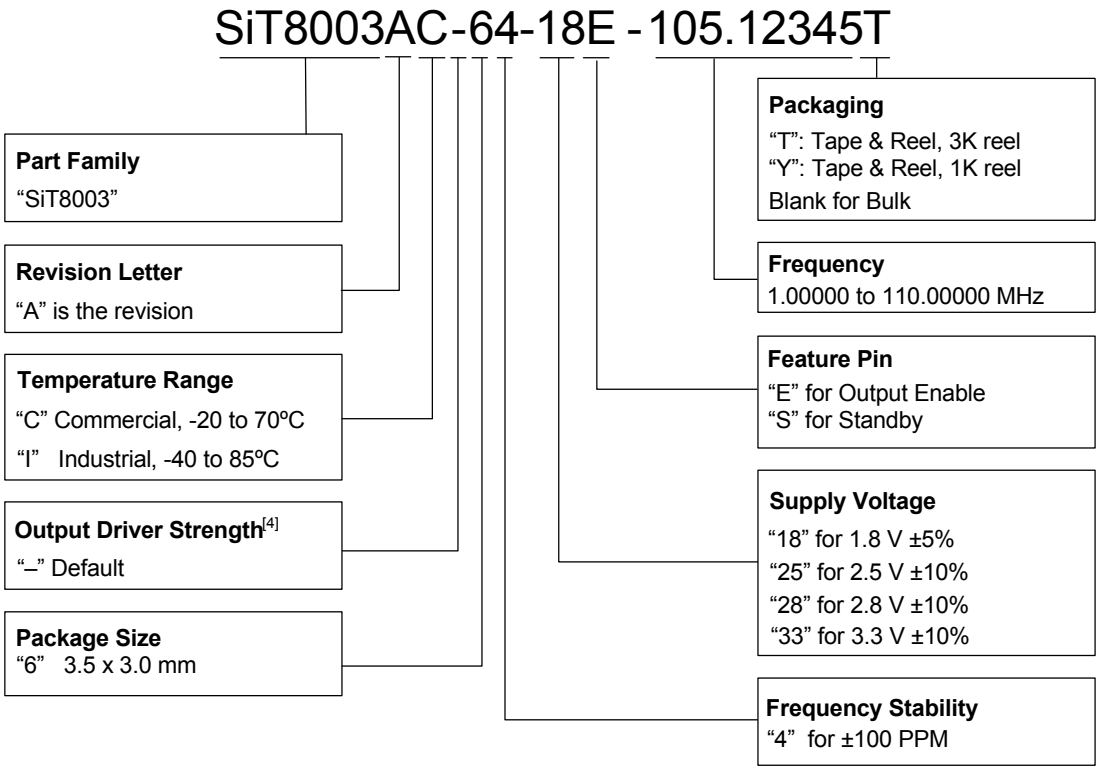
Dimensions and Land Patterns

Package Size – Dimensions (Unit: mm)[2]	Recommended Land Pattern (Unit: mm)[3]
3.5 x 3.0 x 0.25 mm 	

Notes:
2. Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
3. A capacitor of value 0.1μF between Vdd and GND is recommended.

Part No. Guide - How to Order

The Part No. Guide is for reference only. For real-time customization and exact part number, use the SiTime Part Number Generator.



Notes:
4. Contact SiTime for different drive strength options for driving higher loads or reducing EMI.

单击下面可查看定价，库存，交付和生命周期等信息

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