SiT9156

LVPECL, LVDS Oscillator (XO) with 0.3 ps Jitter for 10Gb Ethernet

The Smart Timing Choice™

Features

- 0.3 ps RMS phase jitter (random) for 10GbE applications
- Frequency stability as low as ±10 ppm
- 100% drop-in replacement for quartz and SAW oscillators
- Configurable positive frequency shift, +25, +50, or +75 ppm
- Industry-standard packages: 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mmxmm
- Industrial and extended commercial temperature ranges
- Best in class 1-year and 10-year aging
- Best resilience, up to 40x better than quartz
- For other frequencies, refer to SiT9121 or 9122 datasheet

Applications

- 10GB Ethernet, SONET, SATA, SAS, Fibre Channel, PCI-Express
- Telecom, networking, instrumentation, storage, servers

Electrical Characteristics

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVPECL and LVDS, Common Electrical Characteristics						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
		2.25	–	3.63	V	Termination schemes in Figures 1 and 2 - XX ordering code
Output Frequency Range	f	156.25000, 156.253906, 156.257812, 156.261718, 161.132800			MHz	156.253906 MHz, +25 PPM from 156.250000 156.257812 MHz, +50 PPM from 156.250000 156.261718 MHz, +75 PPM from 156.250000
Frequency Stability	F_stab	-10	–	+10	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, and load variations
		-20	–	+20	ppm	
		-25	–	+25	ppm	
		-50	–	+50	ppm	
First Year Aging	F_aging1	-2	–	+2	ppm	25°C
10-year Aging	F_aging10	-5	–	+5	ppm	25°C
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-20	–	+70	°C	Extended Commercial
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z_in	–	100	250	kΩ	Pin 1, OE logic high or logic low, or $\overline{ST}$ logic high
		2	–	–	MΩ	Pin 1, $\overline{ST}$ logic low
Start-up Time	T_start	–	6	10	ms	Measured from the time Vdd reaches its rated minimum value.
Resume Time	T_resume	–	6	10	ms	In Standby mode, measured from the time $\overline{ST}$ pin crosses 50% threshold.
Duty Cycle	DC	45	–	55	%	Contact SiTime for tighter duty cycle
LVPECL, DC and AC Characteristics						
Current Consumption	Idd	–	61	69	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Standby Current	I_std	–	–	100	µA	$\overline{ST}$ = Low, for all Vdds
Maximum Output Current	I_driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 1(a)
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 1(a)
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 1(b)
Rise/Fall Time	Tr, Tf	–	300	500	ps	20% to 80%, see Figure 1(a)
OE Enable/Disable Time	T_oe	–	–	120	ns	f = 156.25 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Phase Jitter (random)	T_phj	–	0.25	0.3	ps	IEEE802.3-2005 10GbE jitter measurement specifications
LVDS, DC and AC Characteristics						
Current Consumption	Idd	–	47	55	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Differential Output Voltage	VOD	250	350	450	mV	See Figure 2

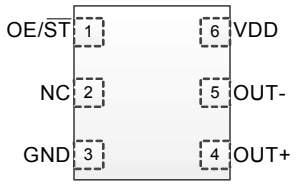
Electrical Characteristics (continued)

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVDS, DC and AC Characteristics (continued)						
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Standby Current	I_std	–	–	100	µA	$\overline{ST}$ = Low, for all Vdds
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 2
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 2
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 2
Rise/Fall Time	Tr, Tf	–	495	600	ps	20% to 80%, see Figure 2
OE Enable/Disable Time	T_oe	–	–	115	ns	f = 156.25 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Phase Jitter (random)	T_phj	–	0.25	0.3	ps	IEEE802.3-2005 10GbE jitter measurement specifications

Pin Description

Pin	Map	Functionality	
1	OE	Input	H or Open: specified frequency output L: output is high impedance
	$\overline{ST}$	Input	H or Open: specified frequency output L: Device goes to sleep mode. Supply current reduces to I_std.
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage

Top View



Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge (HBM)	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Thermal Consideration

Package	θJA, 4 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050, 6-pin	142	27
5032, 6-pin	97	20
3225, 6-pin	109	20

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Waveform Diagrams

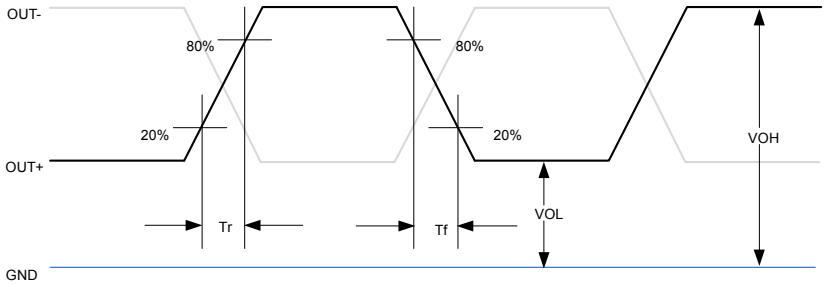


Figure 1(a). LVPECL Voltage Levels per Differential Pin (OUT+/OUT-)

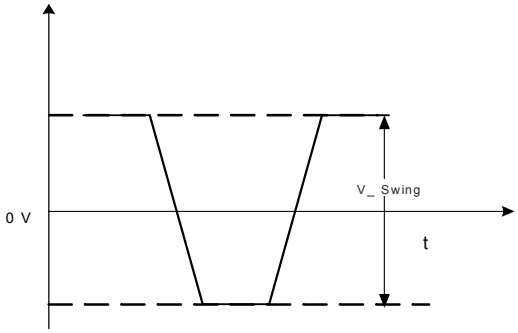


Figure 1(b). LVPECL Voltage Levels Across Differential Pair

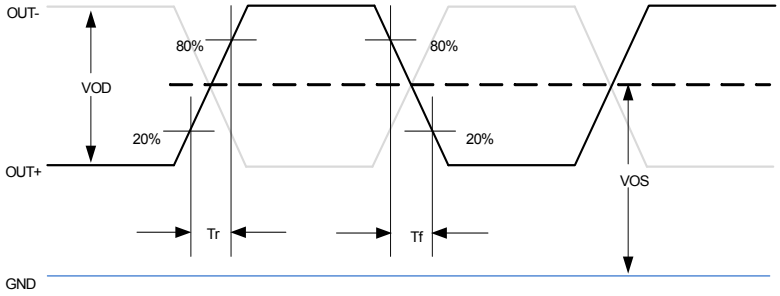


Figure 2. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

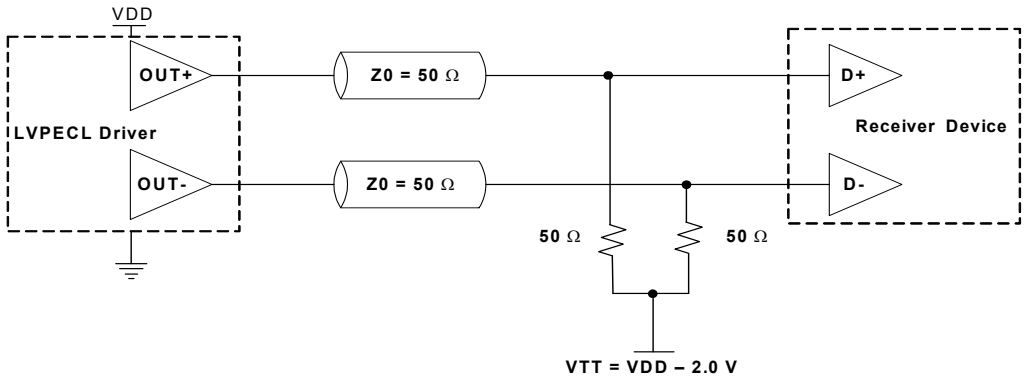


Figure 3. LVPECL Typical Termination

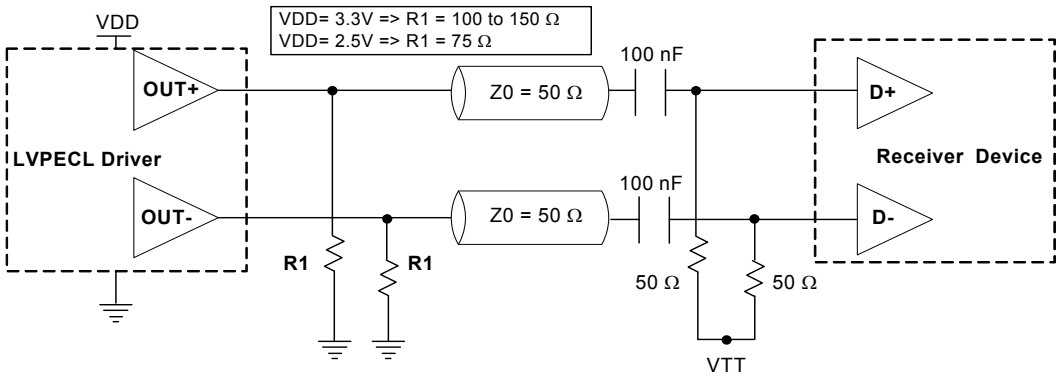


Figure 4. LVPECL AC Coupled Termination

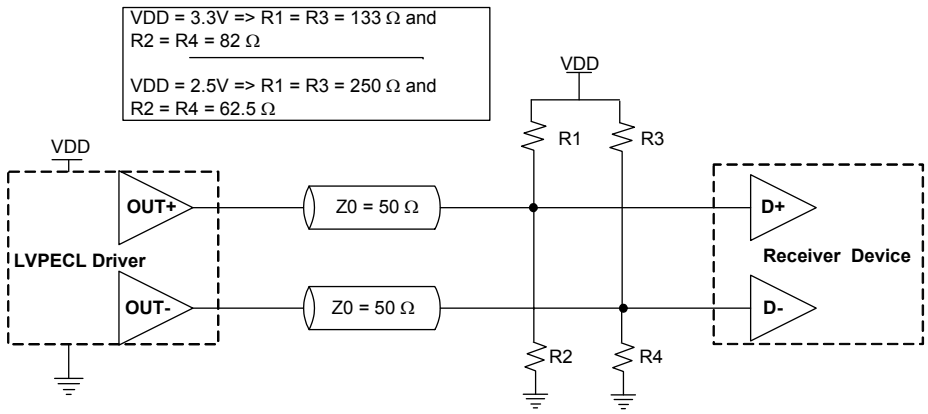


Figure 5. LVPECL with Thevenin Typical Termination

LVDS:

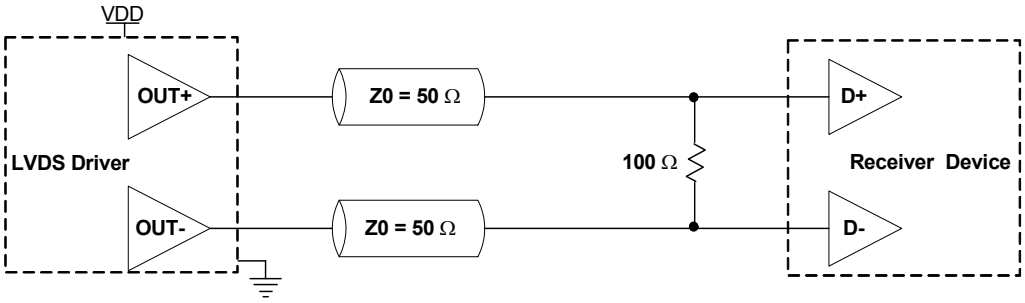
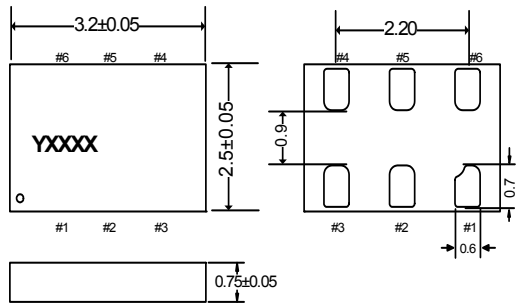
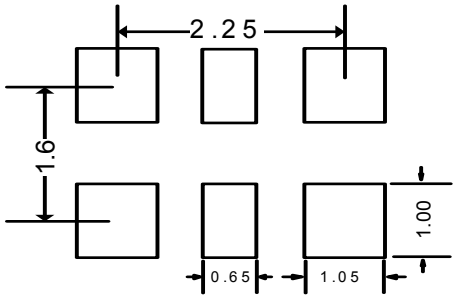


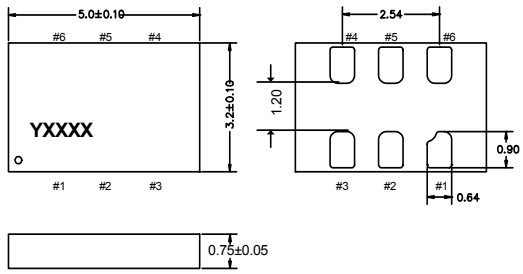
Figure 6. LVDS Single Termination (Load Terminated)

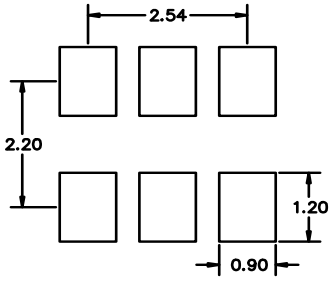
Dimensions and Patterns

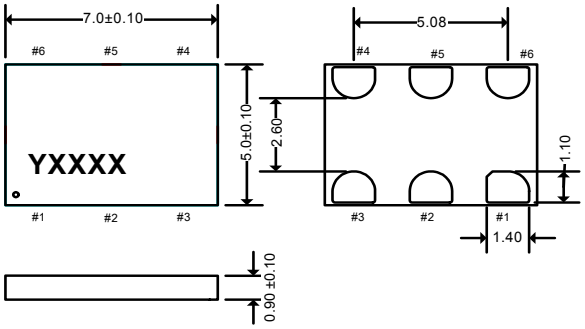
Package Size – Dimensions (Unit: mm)[1]	Recommended Land Pattern (Unit: mm)[2]
3.2 x 2.5x 0.75 mm	
5.0 x 3.2 x 0.75 mm	
7.0 x 5.0x 0.90 mm	

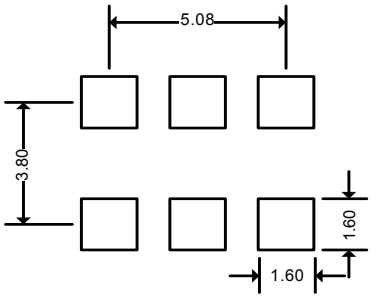








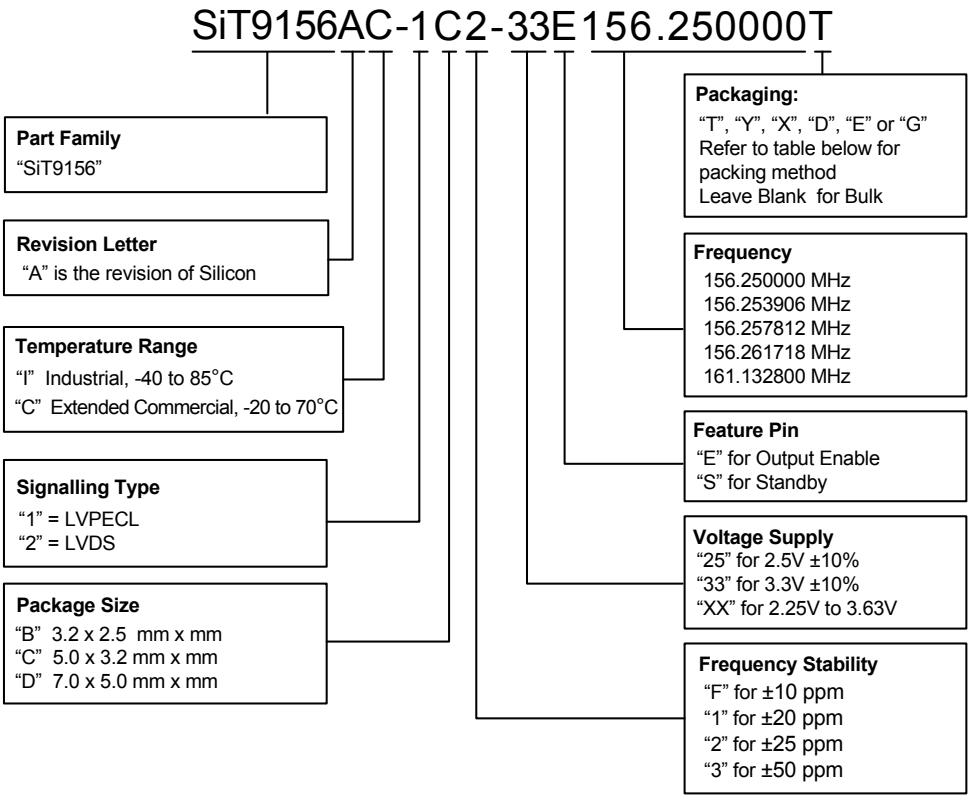




Notes:

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
2. A capacitor of value 0.1 µF between Vdd and GND is recommended.

Ordering Information



Ordering Codes for Supported Tape & Reel Packing Method

Device Size	8 mm T&R (3ku)	8 mm T&R (1ku)	8 mm T&R (250u)	12 mm T&R (3ku)	12 mm T&R (1ku)	12 mm T&R (250u)	16 mm T&R (3ku)	16 mm T&R (1ku)	16 mm T&R (250u)
7.0 x 5.0 mm	–	–	–	–	–	–	T	Y	X
5.0 x 3.2 mm	–	–	–	T	Y	X	–	–	–
3.2 x 2.5 mm	D	E	G	T	Y	X	–	–	–

Revision History

Version	Release Date	Change Summary
1.01	2/20/13	Original
1.02	12/3/13	Added input specifications, LVPECL/LVDS waveforms, packaging T&R options
1.03	2/6/14	Added 8mm T&R option
1.04	3/3/14	Added ±10 ppm
1.05	7/23/14	Include Thermal Consideration Table
1.06	10/6/14	Modified Thermal Consideration values

单击下面可查看定价，库存，交付和生命周期等信息

>>SiTime