

**DUAL N-CHANNEL ENHANCEMENT MODE MOSFET**

**Product Summary**

$V_{(BR)DSS}$	$R_{DS(ON) \max}$	$I_D \max$ $T_A = +25^\circ C$
30V	20mΩ @ $V_{GS} = 10V$	10A

**Description**

This MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

**Applications**

- General Purpose Interfacing Switch
- Power Management Functions
- DC-DC Converters
- Analog Switch

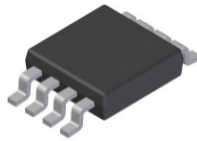
**Features and Benefits**

- Low On-Resistance
- Low Input Capacitance
- Low Input/Output leakage
- Low Gate Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

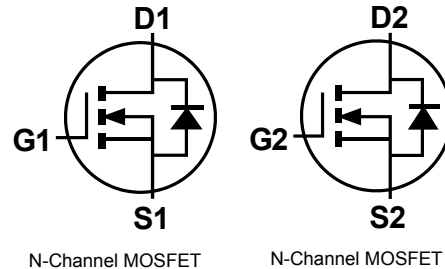
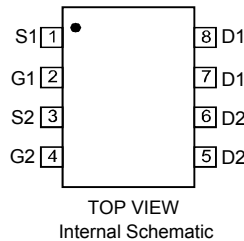
**Mechanical Data**

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.072 grams (approximate)

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Top View

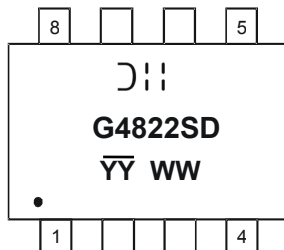


**Ordering Information** (Note 4)

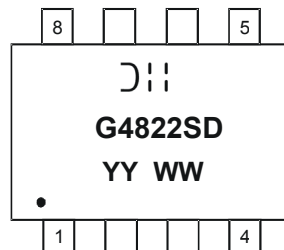
Part Number	Case	Packaging
DMG4822SSD-13	SO-8	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**



Chengdu A/T Site



Shanghai A/T Site

⌋⌋ = Manufacturer's Marking  
 G4822SD = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY or  $\overline{YY}$  = Year (ex: 13 = 2013)  
 WW = Week (01 - 53)  
 YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)  
 $\overline{YY}$  = Date Code Marking for CAT (Chengdu Assembly/ Test site)

**Maximum Ratings** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic		Symbol	Value	Units
Drain-Source Voltage		$V_{DSS}$	30	V
Gate-Source Voltage		$V_{GSS}$	$\pm 25$	V
Continuous Drain Current (Note 5) $V_{GS} = 10\text{V}$	Steady State	$I_D$	10	A
			6.6	
Pulsed Drain Current (Note 6)		$I_{DM}$	60	A
Avalanche Current (Note 7 & 8)		$I_{AR}$	1.68	A
Repetitive Avalanche Energy $L = 0.3\text{mH}$ (Note 7 & 8)		$E_{AR}$	12.8	mJ

**Thermal Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	$P_D$	1.42	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	88.4	$^\circ\text{C/W}$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 9)</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	30	-	-	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS (Note 9)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	1	-	3	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	13.4	20	m $\Omega$	$V_{GS} = 10\text{V}, I_D = 8.5\text{A}$
		-	19.5	31		$V_{GS} = 4.5\text{V}, I_D = 6\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	-	20	-	mS	$V_{DS} = 5\text{V}, I_D = 8.5\text{A}$
Diode Forward Voltage	$V_{SD}$	-	0.4	1.0	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
<b>DYNAMIC CHARACTERISTICS (Note 10)</b>						
Input Capacitance	$C_{iss}$	-	478.9	-	pF	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Output Capacitance	$C_{oss}$	-	96.7	-	pF	
Reverse Transfer Capacitance	$C_{rss}$	-	61.4	-	pF	
Gate resistance	$R_g$		1.1		$\Omega$	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ( $V_{GS} = 4.5\text{V}$ )	$Q_g$		5		nC	$V_{GS} = 10\text{V}, V_{DS} = 15\text{V}, I_D = 8.5\text{A}$
Total Gate Charge ( $V_{GS} = 10\text{V}$ )	$Q_g$	-	10.5	-	nC	
Gate-Source Charge	$Q_{gs}$	-	1.8	-	nC	
Gate-Drain Charge	$Q_{gd}$	-	1.6	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	2.9	-	ns	$V_{DS} = 15\text{V}, V_{GS} = 10\text{V}, R_L = 1.8\Omega, R_G = 3\Omega,$
Turn-On Rise Time	$t_r$	-	7.9	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	14.6	-	ns	
Turn-Off Fall Time	$t_f$	-	3.1	-	ns	

- Notes:
- Device mounted on FR-4 PCB, with minimum recommended pad layout.
  - Device mounted on minimum recommended pad layout test board, 10 $\mu\text{s}$  pulse duty cycle = 1%
  - Repetitive rating, pulse width limited by junction temperature.
  - $I_{AR}$  and  $E_{AR}$  rating are based on low frequency and duty cycles to keep  $T_J = +25^\circ\text{C}$
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to product testing.

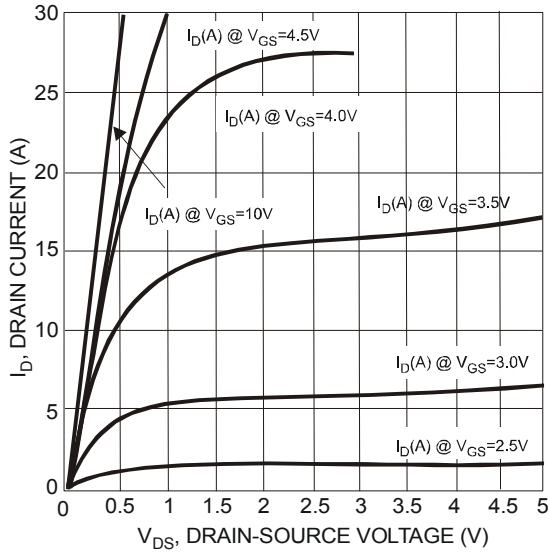


Fig. 1 Typical Output Characteristic

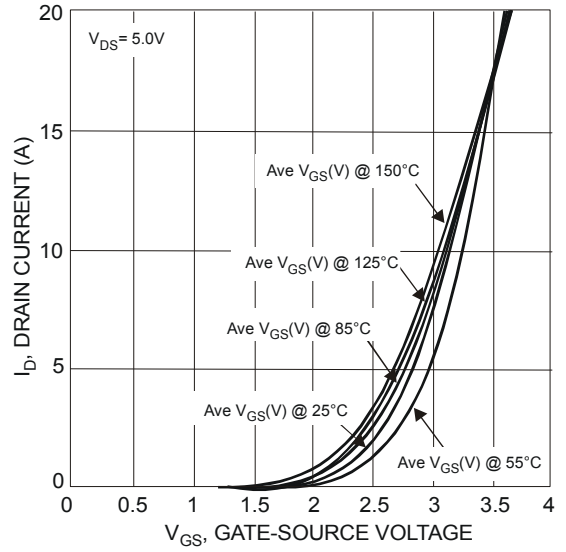


Fig. 2 Typical Transfer Characteristics

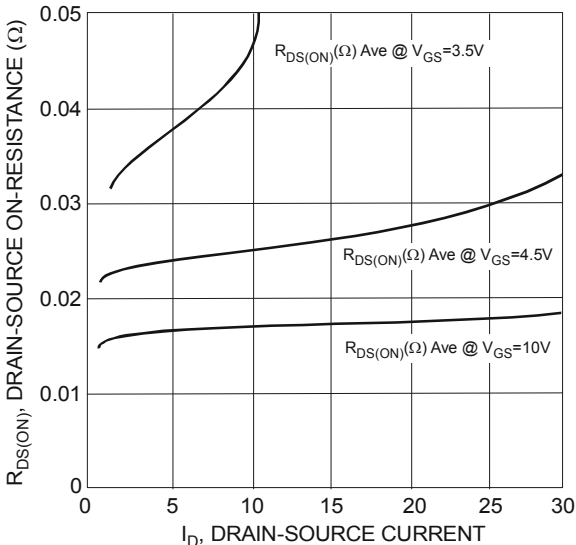


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

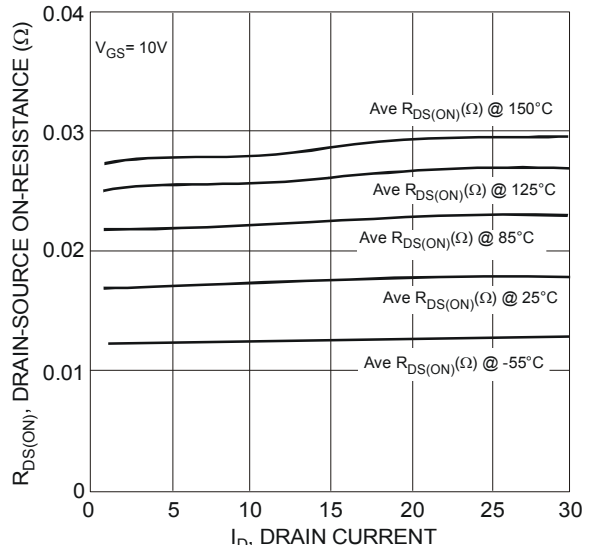


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

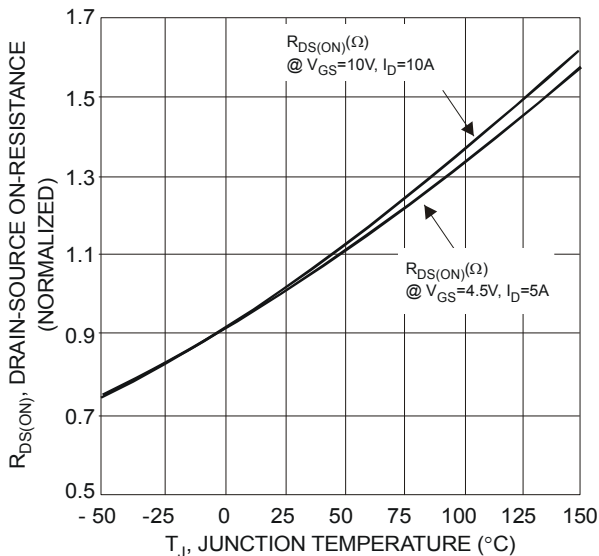


Fig. 5 On-Resistance Variation with Temperature

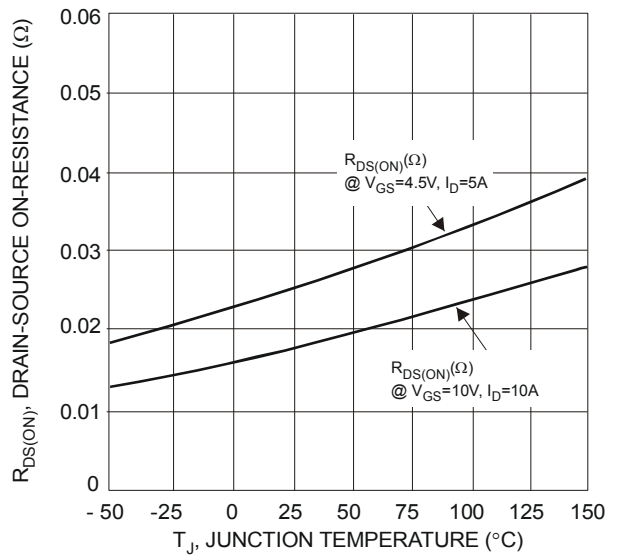


Fig. 6 On-Resistance Variation with Temperature

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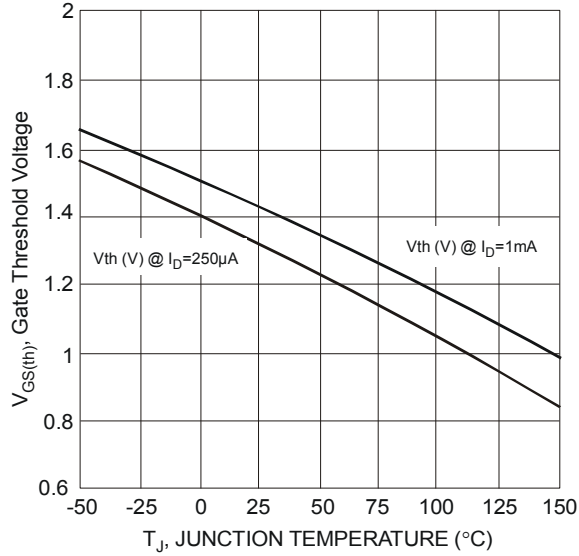


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

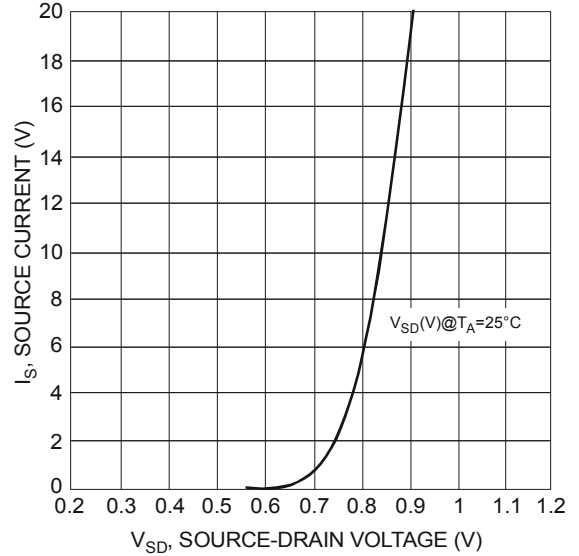


Fig.8 Diode Forward Voltage vs. Current

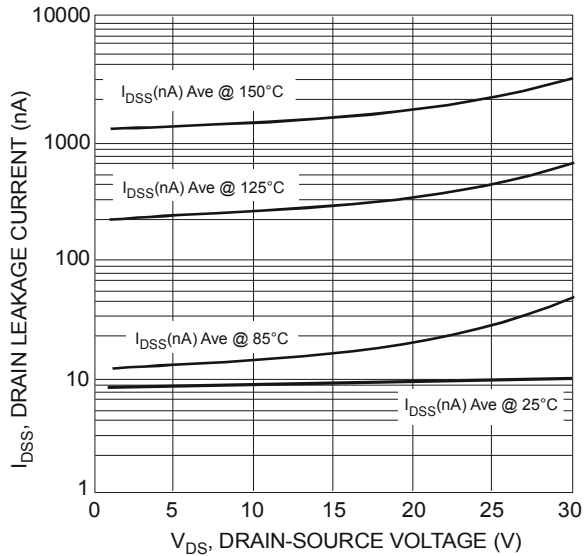


Fig. 9 Typical Drain-Source Leakage Current vs. Voltage

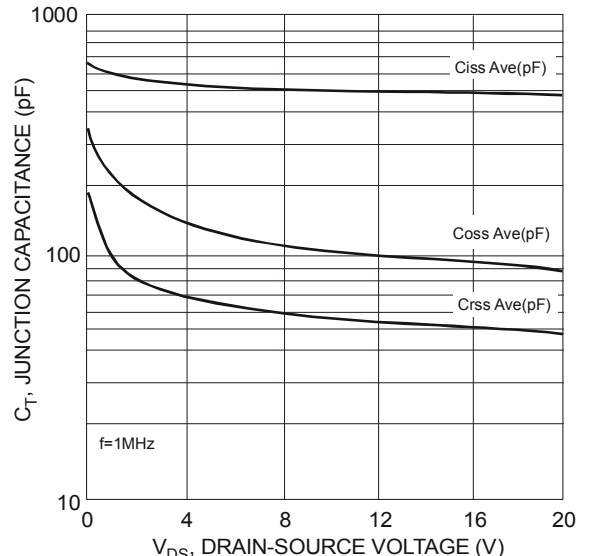


Fig. 10 Typical Junction Capacitance

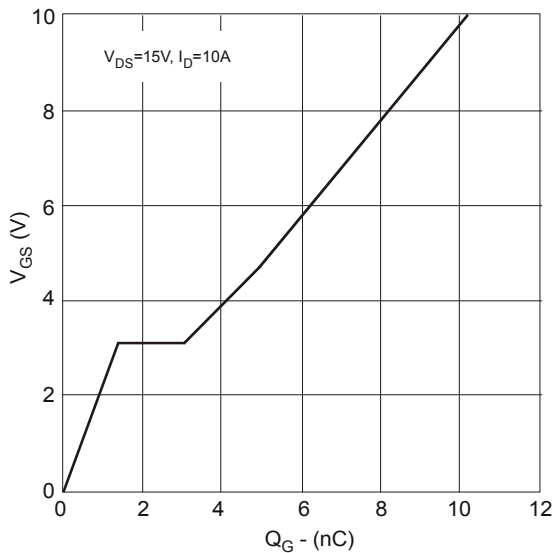


Fig. 11 Gate Charge

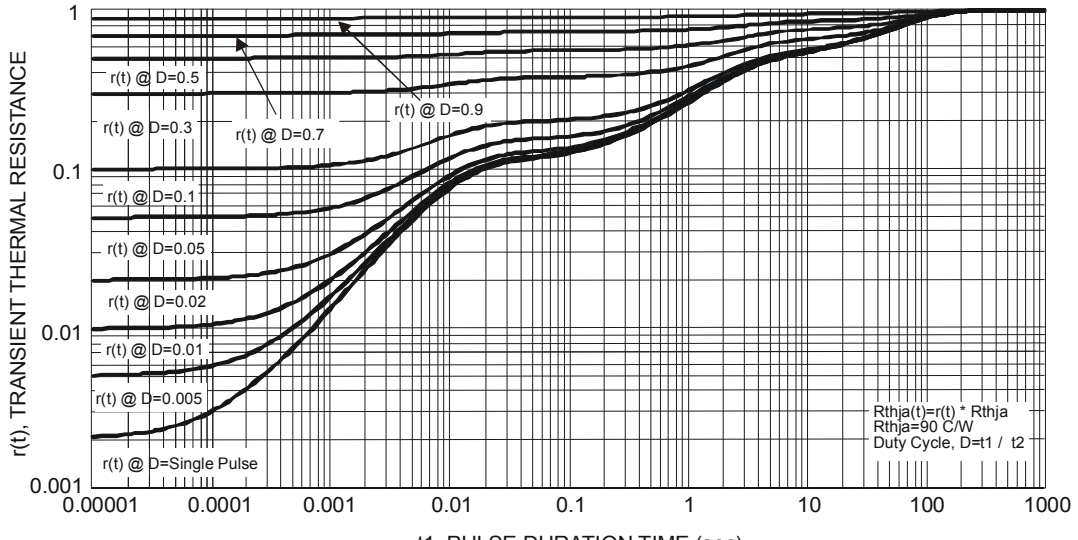
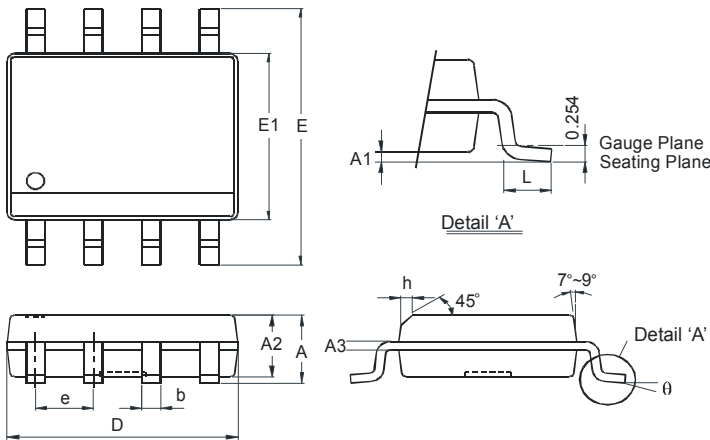


Fig. 12 Transient Thermal Resistance

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**Package Outline Dimensions**

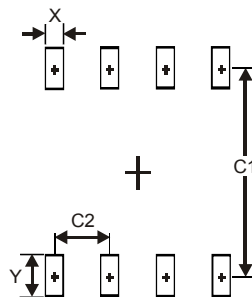
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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