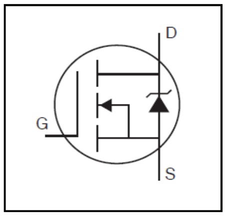
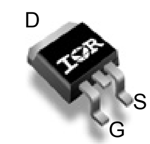
Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- Enhanced dv/dt and di/dt capability
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}		40V
$R_{DS(on)}$	typ.	3.8mΩ
	max.	4.9mΩ
I_{D} (Silicon Limited)		122A①
I_{D} (Package Limited)		56A



D²Pak
AUIRLS3114Z

G	D	S
Gate	Drain	Source

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRLS3114Z	D²-Pak	Tube	50	AUIRLS3114Z
		Tape and Reel Left	800	AUIRLS3114ZTRL

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	122①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	86①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wirebond Limited)	56	
I_{DM}	Pulsed Drain Current ②	488	
P_D @T_C = 25°C	Maximum Power Dissipation	143	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ③	168	mJ
$E_{AS\ (Tested)}$	Single Pulse Avalanche Energy (Tested)	518	
I_{AR}	Avalanche Current ②	See Fig.15,16, 12a, 12b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ
dv/dt	Peak Diode Recovery ④	2.3	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	——	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑦	——	40	

HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

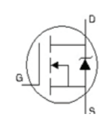
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.03	——	V/°C	Reference to 25°C, I_D = 1mA ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	3.8	4.9	mΩ	V_{GS} = 10V, I_D = 56A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	1.0	1.7	2.5	V	V_{DS} = V_{GS}, I_D = 100μA
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	——	-6.6	——	mV/°C	
gfs	Forward Trans conductance	103	——	——	S	V_{DS} = 10V, I_D = 56A
$R_{G(Int)}$	Internal Gate Resistance	——	0.8	——	Ω	
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	250		V_{DS} = 40V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -16V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q_g	Total Gate Charge	——	35	53	nC	I_D = 56A
Q_{gs}	Gate-to-Source Charge	——	11	——		V_{DS} = 20V
Q_{gd}	Gate-to-Drain Charge	——	16	——		V_{GS} = 4.5V⑤
$t_{d(on)}$	Turn-On Delay Time	——	28	——	ns	V_{DD} = 20V
t_r	Rise Time	——	271	——		I_D = 56A
$t_{d(off)}$	Turn-Off Delay Time	——	43	——		R_G= 3.7Ω
t_f	Fall Time	——	60	——		V_{GS} = 4.5V⑤
C_{iss}	Input Capacitance	——	3617	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	633	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	345	——		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	2378	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	570	——		V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz
$C_{oss\ eff.}$	Effective Output Capacitance	——	875	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	122①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	488		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C,I_S = 56A,V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	——	33	50	ns	T_J = 25°C ,I_F = 56A, V_{DD} = 20V
Q_{rr}	Reverse Recovery Charge	——	32	48	nC	di/dt = 100A/μs ⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
② Repetitive rating; pulse width limited by max. junction temperature.
③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.107mH, R_G = 50Ω, I_{AS} = 56A, V_{GS} =10V. Part not recommended for use above this value.
④ $I_{SD} \le$ 56A, di/dt $\le$ 263A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 175°C.
⑤ Pulse width $\le$ 1.0ms; duty cycle $\le$ 2%.
⑥ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
⑧ R_θ is measured at T_J approximately 90°C.

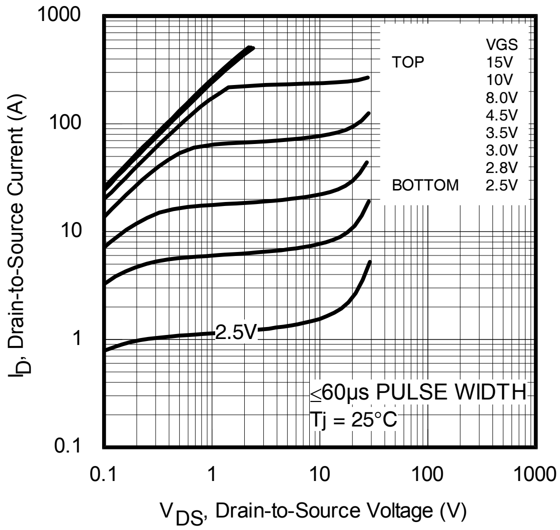


Fig. 1 Typical Output Characteristics

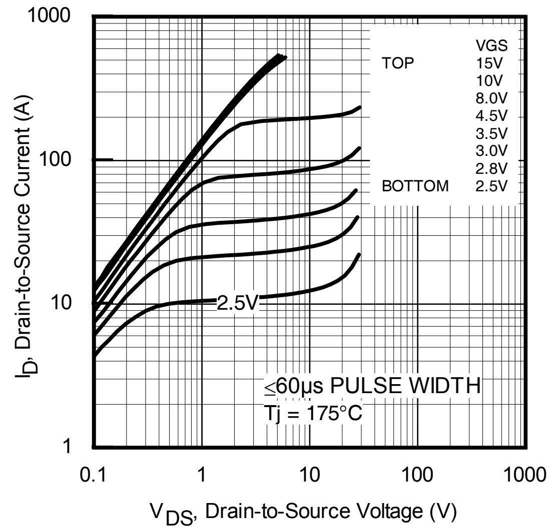


Fig. 2 Typical Output Characteristics

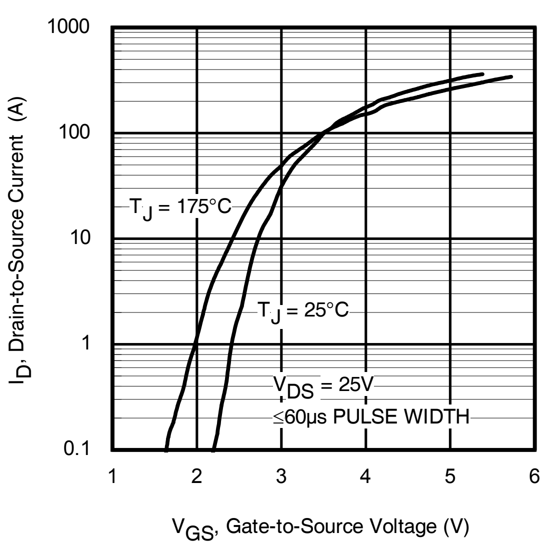


Fig. 3 Typical Transfer Characteristics

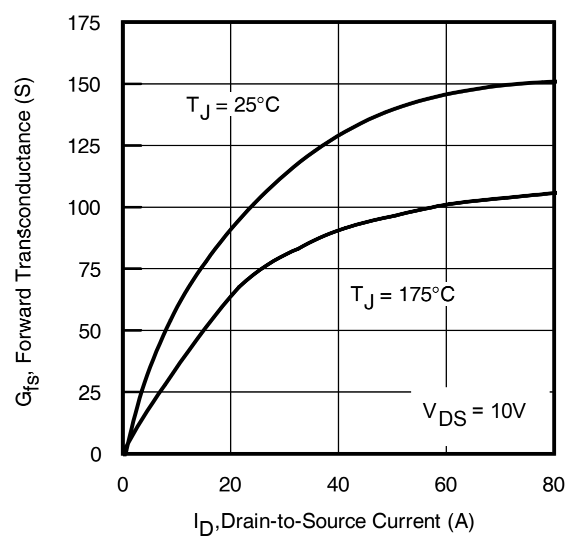


Fig. 4 Typical Forward Trans conductance vs. Drain Current

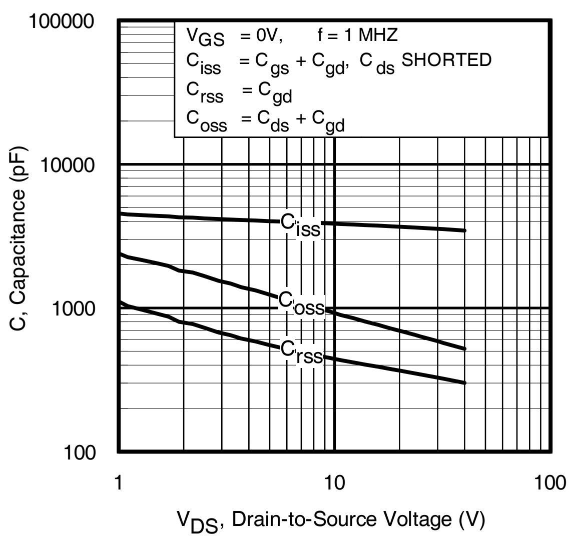


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

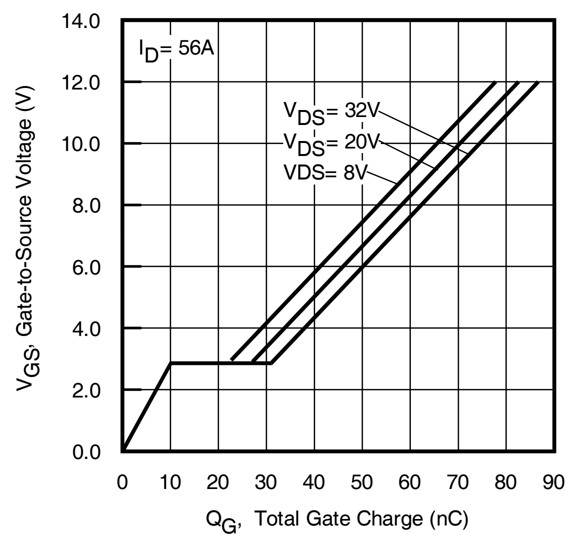


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

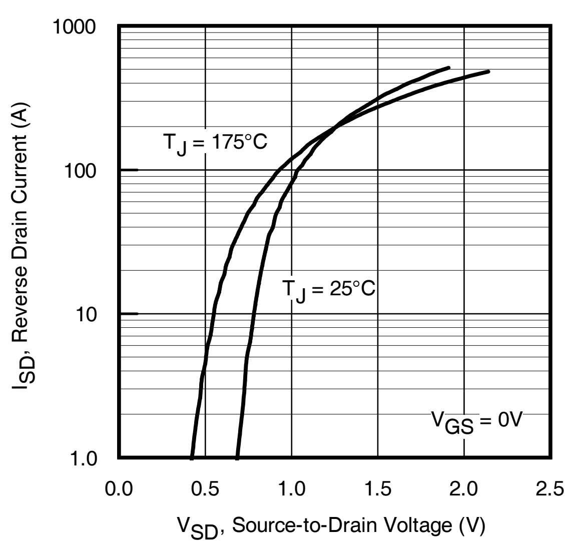


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

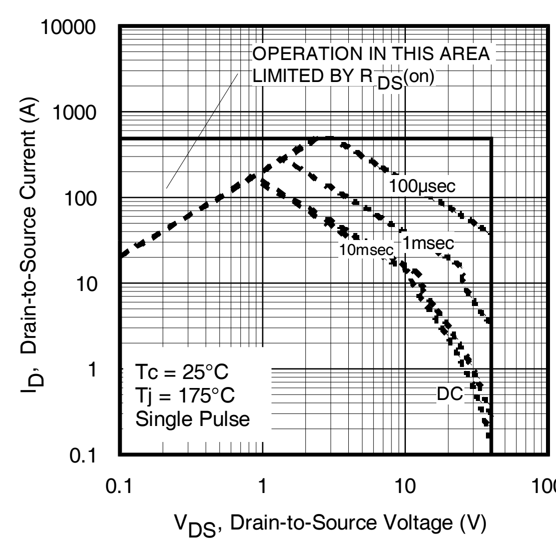
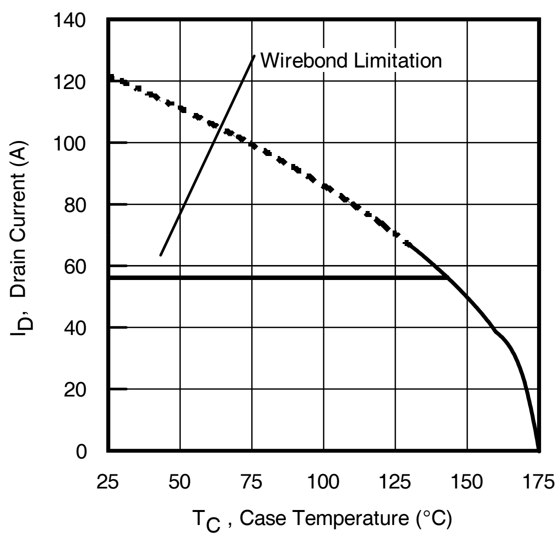


Fig 8. Maximum Safe Operating Area



Fg 9. Maximum Drain Current vs. Case Temperature

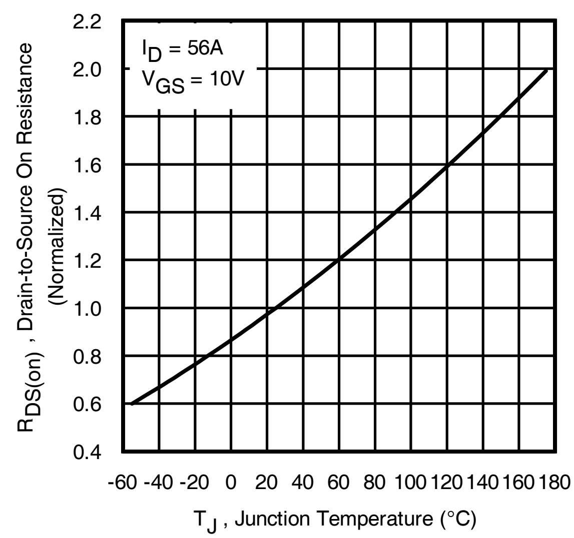


Fig 10. Normalized On-Resistance vs. Temperature

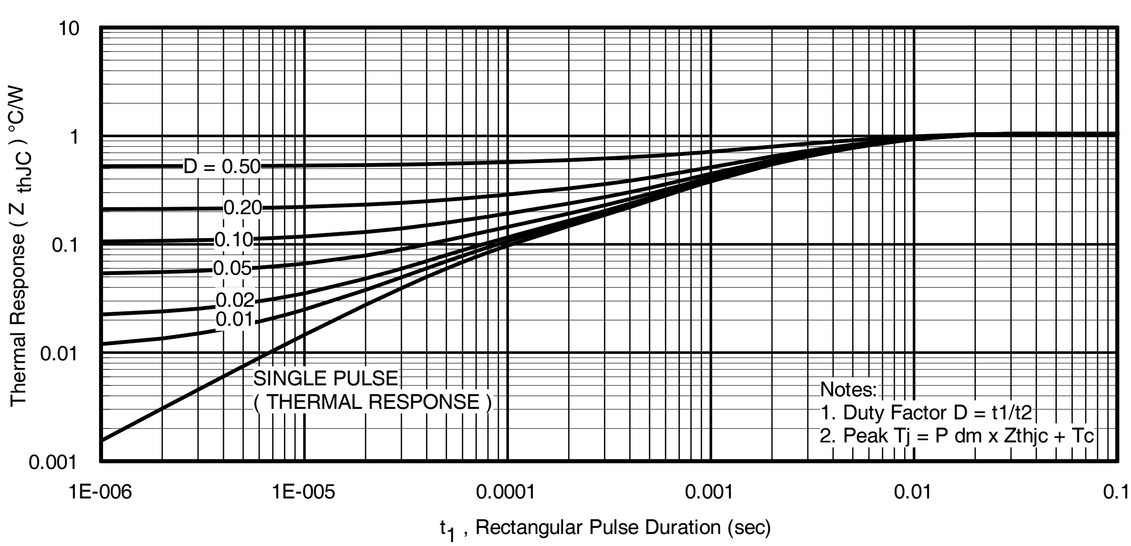


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

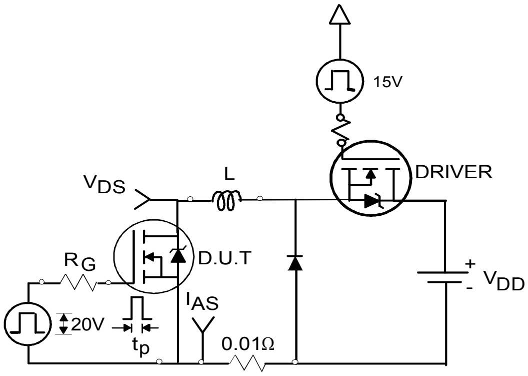


Fig 12a. Unclamped Inductive Test Circuit

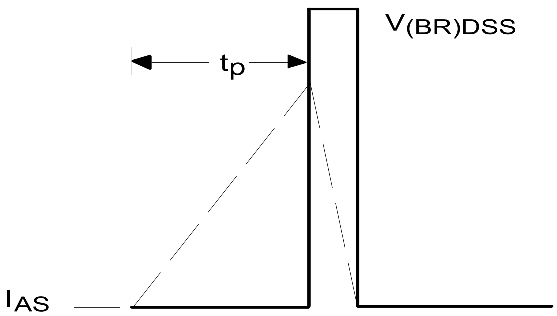


Fig 12b. Unclamped Inductive Waveforms

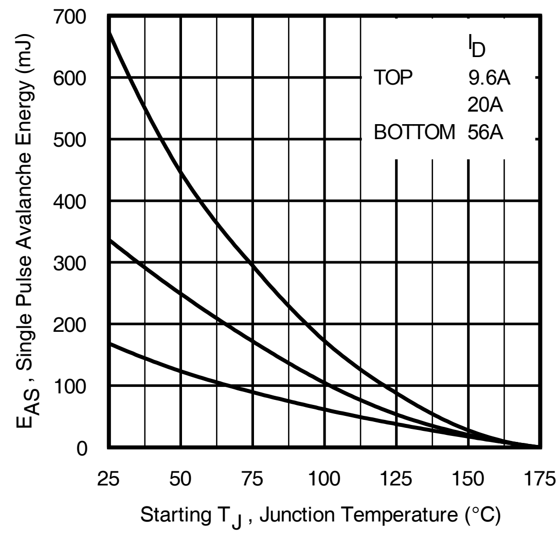


Fig 12c. Maximum Avalanche Energy vs. Drain Current

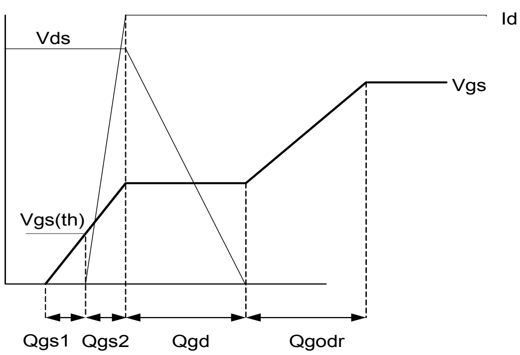


Fig 13a. Gate Charge Waveform

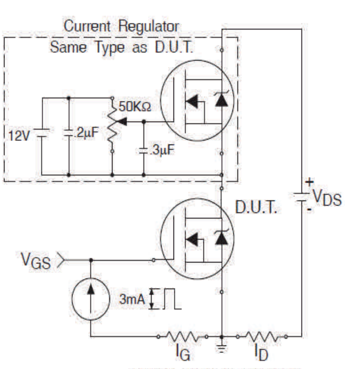


Fig 13b. Gate Charge Test Circuit

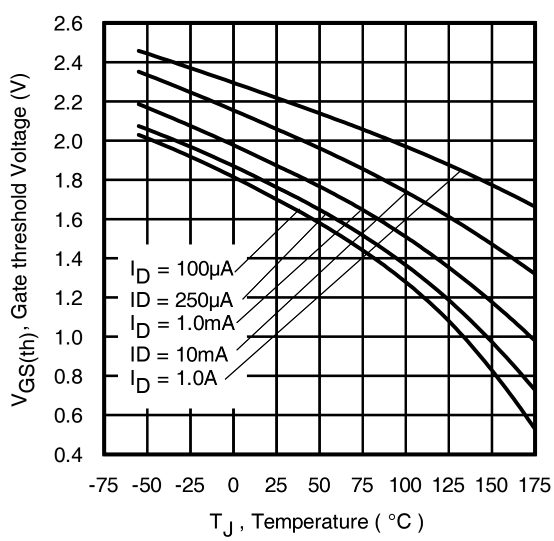


Fig. 14 - Threshold Voltage vs. Temperature

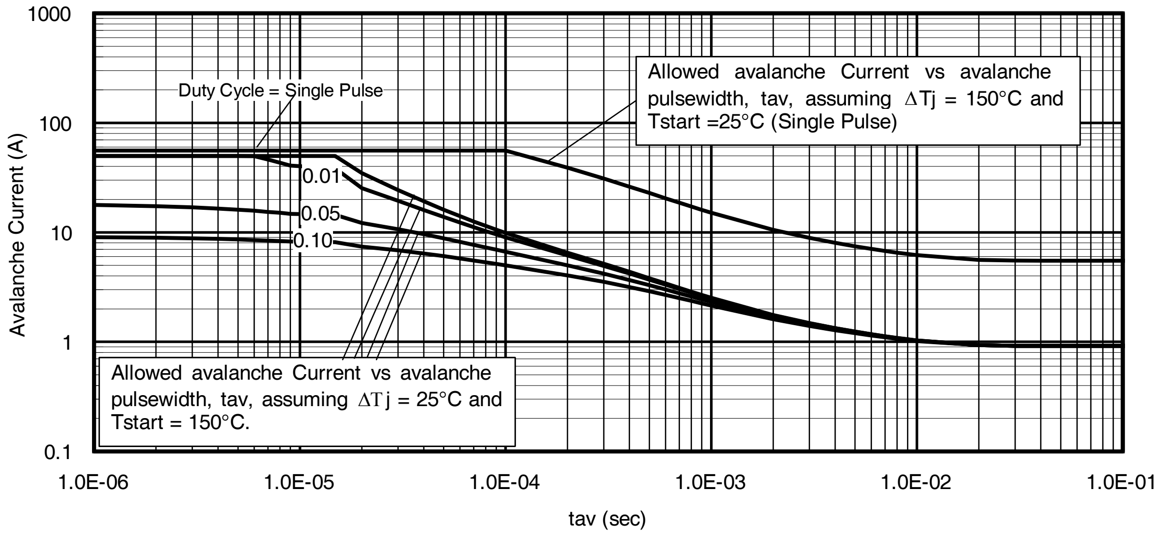


Fig 15. Avalanche Current vs. Pulse width

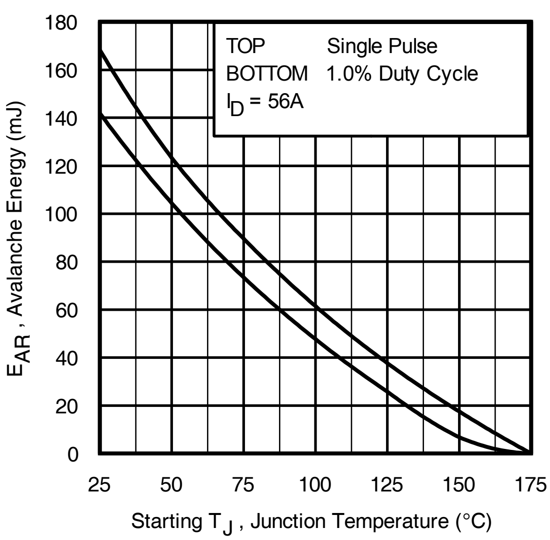


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 11, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

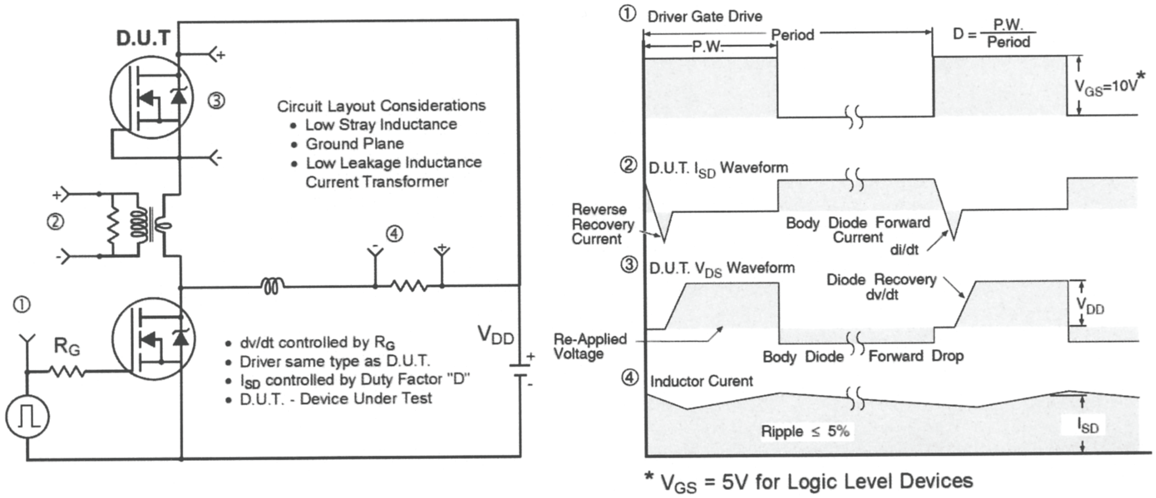


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

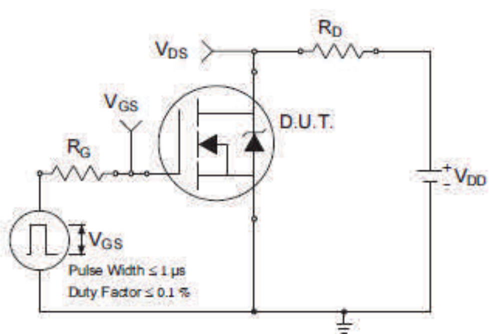


Fig 18a. Switching Time Test Circuit

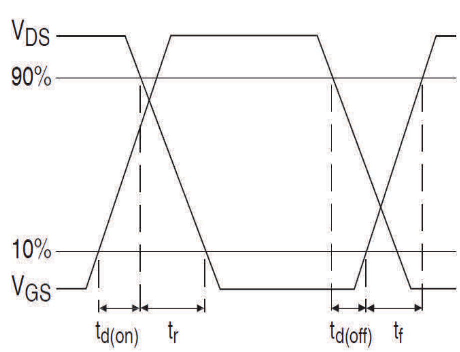
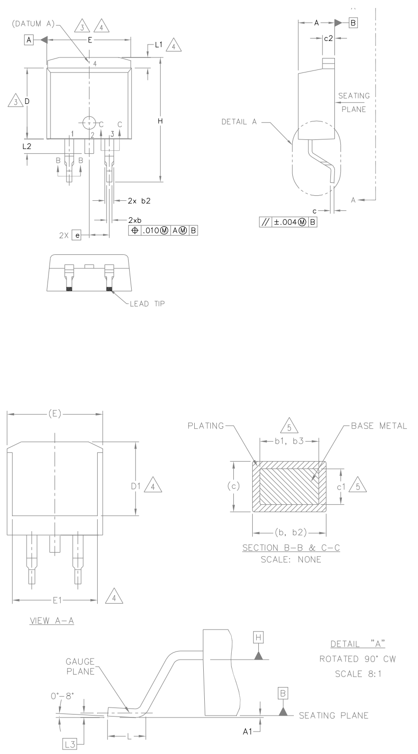


Fig 18b. Switching Time Waveforms

D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. (△3) DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. (△4) THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. (△5) DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245	–	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

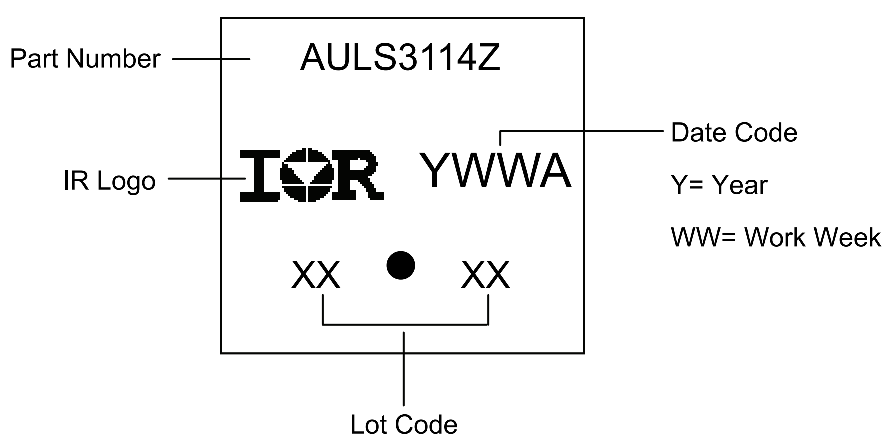
LEAD ASSIGNMENTS

DIODES
1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

HEXFET
1.– GATE
2, 4.– DRAIN
3.– SOURCE

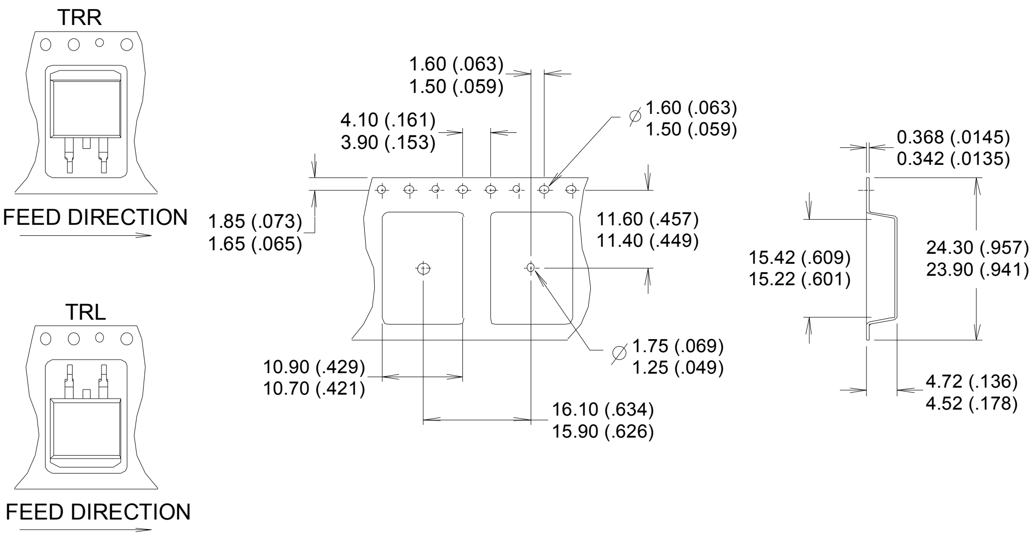
IGBTs, CoPACK
1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

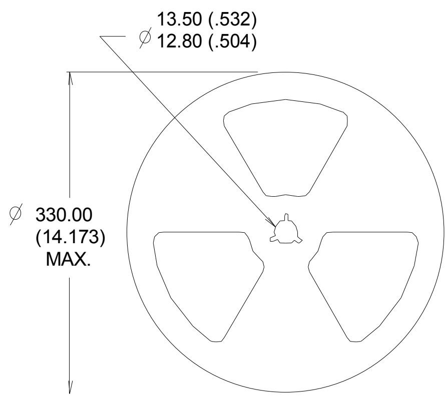
D²Pak (TO-263AB) Part Marking Information

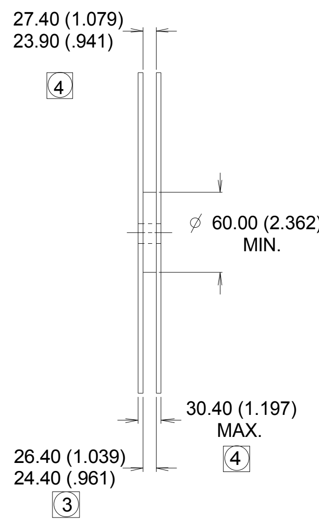


Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))







NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D^2-Pak	MSL1
ESD	Machine Model	Class M4 (+/- 600V)† AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000V)† AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V)† AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
3/3/2014	• Added "Logic Level Gate Drive" bullet in the features section on page 1 • Updated data sheet with new IR corporate template
11/6/2015	• Updated datasheet with corporate template • Corrected ordering table on page 1.

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[>>Infineon Technologies(英飞凌)]