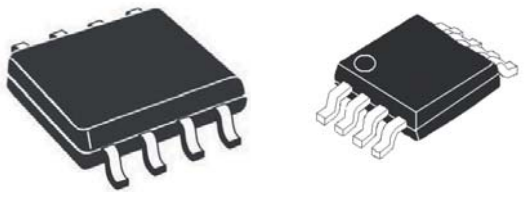
PM8834

4 A dual low-side MOSFET driver

Datasheet - production data



SO8 MSOP 8L-EP

Features

- Dual independent low-side MOSFET driver with 4 A sink and source capability
- Independent enable for each driver
- Driver output parallelability to support higher driving capability
- Matched propagation delays
- CMOS/TTL-compatible input levels
- Wide input supply voltage range: 5 V to 18 V
- Embedded drivers with anti cross conduction protection
- Low bias switching current
- Short propagation delays
- Wide operative temperature range: -40 °C to 105 °C
- Industry standard SO8 package and MSOP8 with exposed pad

Applications

- SMPS
- DC-DC converters
- Motor controllers
- Line drivers
- Class-D switching amplifiers

Description

The PM8834 is a flexible, high-frequency dual low-side driver specifically designed to work with high capacitive MOSFETs and IGBTs.

Both PM8834 outputs can sink and source 4 A independently. A higher driving current can be obtained by connecting the two PWM outputs in parallel.

The PM8834 provides two enable pins which can be used to enable the operation of one or both of the output lines.

The PM8834 works with a CMOS/TTL-compatible PWM signal.

The device is available in an SO8 or an MSOP8 package with an exposed pad.

Table 1. Device summary

Order code	Temp range	Package	Packing
PM8834	-40 °C - 105 °C	SO8	Tube
PM8834TR			Tape and reel
PM8834M		MSOP 8L-EP	Tube
PM8834MTR			Tape and reel

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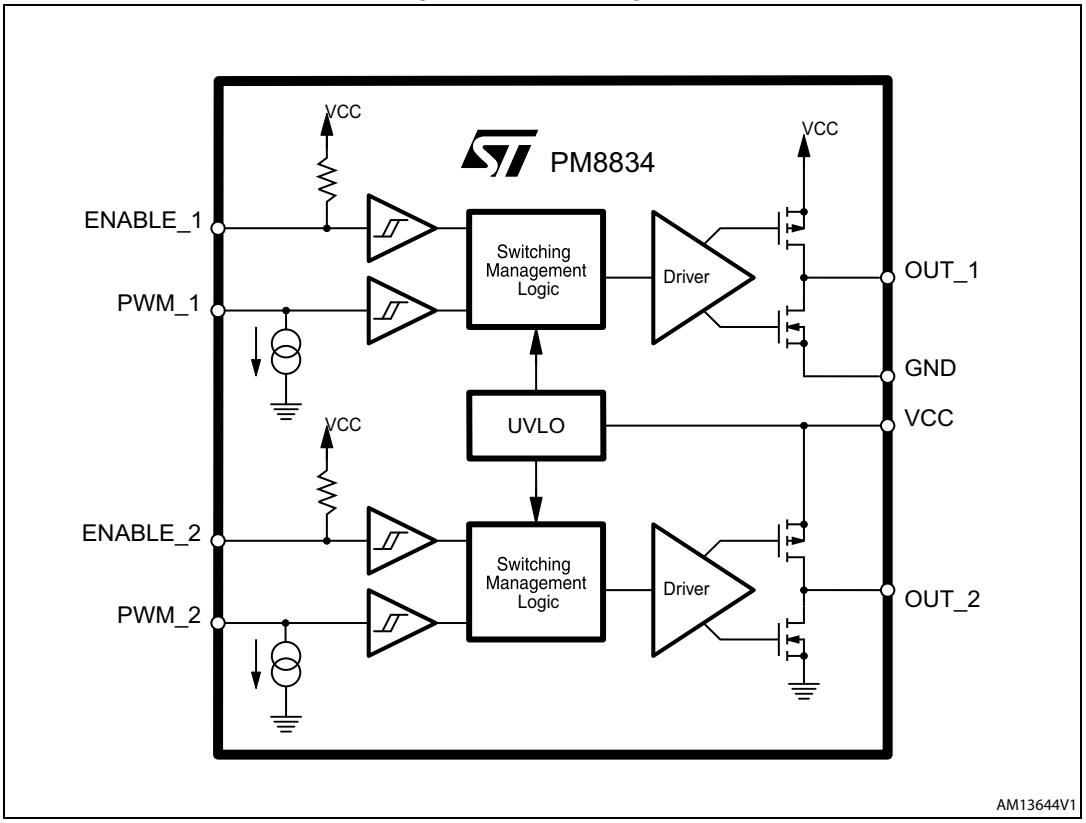
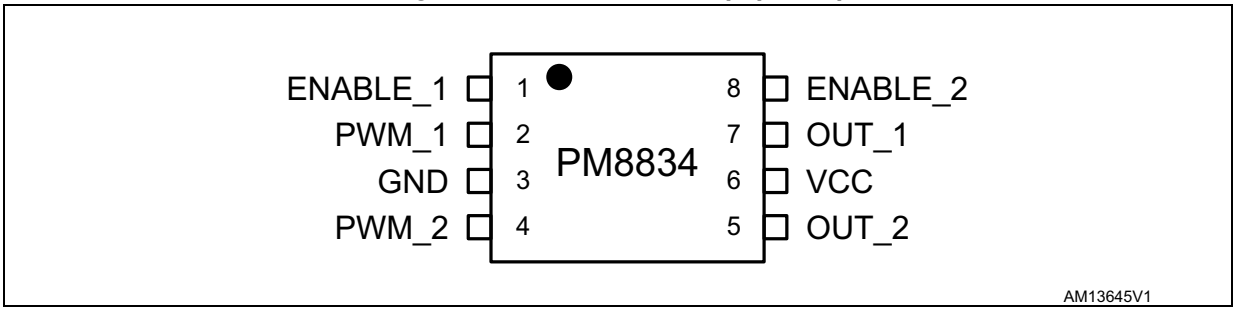
1 Block diagram

Figure 1. Block diagram



2 Pin description and connections

Figure 2. Pin connections (top view)



2.1 Pin description

Table 2. Pin description

Pin no.	Name	Function
1	ENABLE_1	Enable input for Driver 1. Pull low to disable Driver 1 (OUT1 will be low, PWM1 will be ignored). Even though internally pulled up to VCC with a typ. 100 kΩ internal resistor, it is recommended to pull high up directly to VCC externally to enable the section. Enable pin is a device state control pin and must be set before to apply the PWM signal. The pin features TTL/CMOS-compatible thresholds.
2	PWM_1	PWM input signal for Driver 1 featuring TTL/CMOS-compatible threshold and hysteresis. Even though internally pulled down to GND with a 10 µA current generator, it is recommended to pull-down to GND with an external 100 kΩ resistor.
3	GND	All internal references, logic and drivers are referenced to this pin. Connect to the PCB ground plane.
4	PWM_2	PWM input signal for Driver 2 featuring TTL/CMOS-compatible threshold and hysteresis. Even though internally pulled down to GND with a 10 µA current generator, it is recommended to pull-down to GND with an external 100 kΩ resistor.
5	OUT_2	Driver 2 output. The output stage is capable of providing up to 4 A drive current to the gate of a power MOSFET. IGBTs are supported as well. A low ohmic value series resistor can be useful to reduce dissipated power.
6	VCC	PM8834 supply voltage. Bypass with low ESR MLCC capacitor to GND.
7	OUT_1	Driver 1 output. The output stage is capable of providing up to 4 A drive current to the gate of a power MOSFET. IGBTs are supported as well. A low ohmic value series resistor can be useful to reduce dissipated power.
8	ENABLE_2	Enable input for Driver 2. Pull low to disable Driver 2 (OUT2 will be low, PWM2 will be ignored). Even though internally pulled up to VCC with a typ. 100 kΩ internal resistor, it is recommended to pull high up directly to VCC externally to enable the section. Enable pin is a device state control pin and must be set before to apply the PWM signal. The pin features TTL/CMOS compatible thresholds.
PM8834M only		
	EXP PAD	The thermal pad connects the silicon substrate and makes good thermal contact with the PCB. Use multiple vias to connect it to the GND plane.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	-40 to 150	°C
T_J	Junction temperature range	-40 to 150	°C
T_A	Operating ambient temperature range	-40 to 105	°C
SO8			
R_{THJA}	Thermal resistance junction to ambient (device soldered on 2s2p PC board - 67 mm x 67 mm)	85	°C/W
R_{THJC}	Thermal resistance junction to case	40	°C/W
P_{TOT}	Maximum power dissipation at 70 °C (device soldered on 2s2p PC board - 67 mm x 67 mm)	0.65	W
DF	Derating factor above 70 °C	12	mW/°C
MSOP8			
R_{THJA}	Thermal resistance junction to ambient (device soldered on 2s2p PC board - 67 mm x 67 mm)	50	°C/W
R_{THJC}	Thermal resistance junction to case	10	°C/W
P_{TOT}	Maximum power dissipation at 70 °C (device soldered on 2s2p PC board - 67 mm x 67 mm)	1.1	W
DF	Derating factor above 70 °C	20	mW/°C

Note: Maximum power dissipation and derating factor are estimated assuming 125 °C as maximum operating junction temperature.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
All pins	to GND	-0.3 to 19	V
I_{OUTx}	DC output current	500	mA
V_{HBM}	ESD capability, human body model	2	kV

3.2 Electrical characteristics

Table 5. Electrical characteristics [V_{CC} = 5 V to 18 V, Tj = -40 °C to 105 °C unless otherwise specified(1)]

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current	OUT_1, OUT_2 = OPEN VCC = 10 V; T_J = 25 °C		3.5		mA
$UVLO_{VCC}$	VCC turn-ON	VCC rising		4.4	4.6	V
	VCC turn-OFF	VCC falling	3.6	3.8		V
Input threshold						
PWM_x, ENABLE_x	Input high - V_{IH}	Rising threshold		2.2	2.5	V
	Input low - V_{IL}	Falling threshold	0.8	1.1		V
Drivers (OUT_1, OUT_2)						
R_{DSON_H}	Source resistance	VCC = 10 V; IOUT = 100 mA; T_J = 25 °C		1	1.3	Ω
		VCC = 10 V; IOUT = 100 mA; full temp. range			1.5	Ω
I_{SOURCE}	Source current(2)	VCC = 10 V; C_{OUT} to GND = 10 nF		4		A
I_{SINK}	Sink current(2)	VCC = 10 V; C_{OUT} to GND = 10 nF		5		A
R_{DSON_L}	Sink resistance	VCC = 10 V; IOUT = 100 mA; T_J = 25 °C		0.7	1	Ω
		VCC = 10 V; IOUT = 100 mA; full temp. range			1.3	Ω
	Max OUT_x in OFF state	VCC rising with slope > 2 V/ms			1.5	V
Switching time (PWM_1,PWM_2)						
t_R	Rise time	VCC = 10 V; C_{OUT} to GND = 2.5 nF		10	20	ns
		VCC = 10 V; C_{OUT} to GND = 14 nF		45	75	ns
t_F	Fall time	VCC = 10 V; C_{OUT} to GND = 2.5 nF		10	20	ns
		VCC = 10 V; C_{OUT} to GND = 14 nF		35	75	ns

Table 5. Electrical characteristics (continued) [V_{CC} = 5 V to 18 V, Tj = -40 °C to 105 °C unless otherwise specified[(1)]]

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Propagation delay						
t_{D_LH}	Delay - low to high	C_{OUT} to GND = 2.5 nF	15	25	35	ns
t_{D_HL}	Delay - high to low	C_{OUT} to GND = 2.5 nF	20	30	40	ns
	Matching between propagation delays		-5		5	ns

1. Limits guaranteed by design and statistical analysis, not production tested. Production test is done at T = 25 °C.
2. Parameter guaranteed by designed, not fully tested in production.

4 Device description and operation

The PM8834 is a dual low-side driver suitable for charging and discharging large capacitive loads like MOSFETs or IGBTs used in power supplies and DC-DC modules. The PM8834 can sink and source 4 A on both low-side driver branches but a higher driving current can be obtained by paralleling its outputs.

Even though this device has been designed to function with loads requiring high peak current and fast switching time, the ultimate driving capability depends on the power dissipation in the device which must be kept below the power dissipation capability of the package. This aspect will be discussed in *Section 5.2 on page 13*.

For enhanced control of operations the PM8834 has been designed with dual independent active-high enable pins (ENABLE_1 and ENABLE_2). Connecting these pins to the GND pin will disable the corresponding low-side driver.

The PM8834 uses the VCC pin for supply and the GND pin for return.

The dual low-side driver has been designed to work with supply voltage in the range of 5 to 18 V.

For VCC voltages greater than the UVLO threshold ($UVLO_{VCC}$), the PWM input keeps the control of the driver operations, provided that the corresponding enable pin is active. Both PWM_1 and PWM_2 are internally pulled down so, if left floating, the corresponding output pins are discharged.

The PM8834, during VCC startup, keeps both low-side MOSFETs in an OFF state until the UVLO threshold is reached.

The input pins (PWM_1, PWM_2, ENABLE_1 and ENABLE_2) are CMOS/TTL-compatible and can also operate with voltages up to VCC.

The voltage level of the input pins is not allowed to be higher than VCC under any operating condition.

4.1 Input stage

4.1.1 PWM inputs

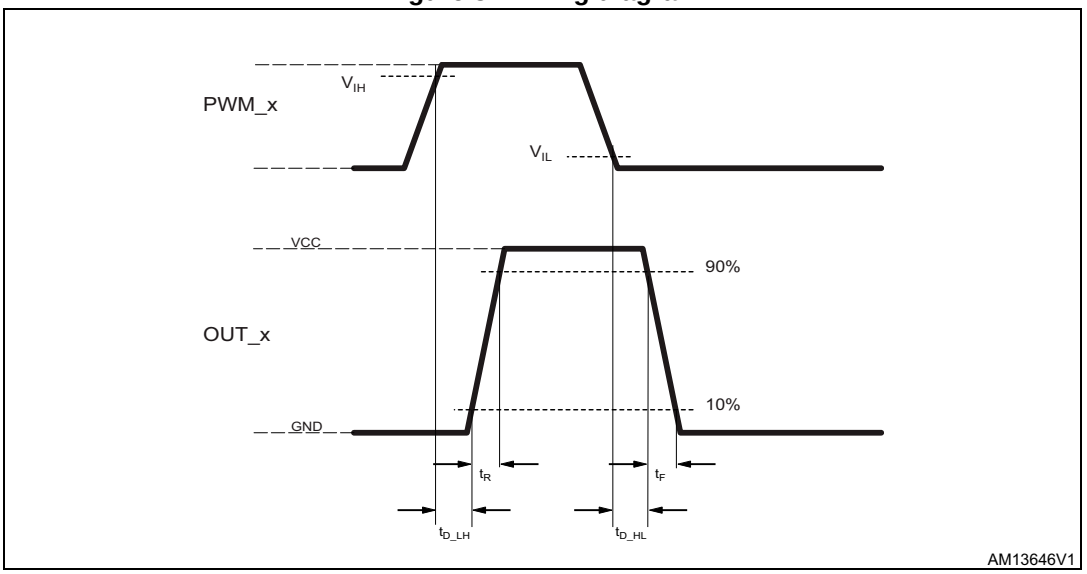
The inputs of the PM8834 dual low-side driver are compatible to CMOS/TTL levels with the capability to be pulled up to VCC.

The relationship between the input pins (PWM_1, PWM_2) and the corresponding PWM output pins (OUT_1, OUT_2) is depicted in *Figure 3*. In the worst case, input levels above 2.5 V are recognized as high voltage and values below 0.8 V are recognized as low logic values. Propagation delays for high-low (t_{D_HL}) and low-high (t_{D_LH}) and rise (t_R) and fall (t_R) times have been designed to ensure operation in a fast-switching environment.

Matched propagation delay in the two branches of the PM8834 ensures symmetry in operation and allows parallel output functionality.

Each PWM input features a 10 µA pull-down to turn off (default state) the external MOSFET / IGBT.

Figure 3. Timing diagram



4.1.2 Enable pins

The PM8834 features two independent enable signals, ENABLE_1 and ENABLE_2, to control the operation of each low-side driver. Both enable pins are internally pulled up to VCC with a typ. 100 kΩ resistance and are active high. In applications where ENABLE_1 and ENABLE_2 are not in use, it is strongly recommended to connect these pins to VCC directly or with a pull-up resistor. ENABLE_1 and ENABLE_2 are compatible to CMOS/TTL levels and can be directly pulled up to VCC. By default, because of the internal pull-up, both drivers are enabled. It is possible to disable one or both low-side drivers, connecting the corresponding enable signal to GND.

The enable pins cannot be used as input driving pins, but only as device control pins; they must be set before to apply the PWM signals; high to low transition on enable pins cannot be simultaneous with transition edges on the PWM inputs.

The enable pins are not designed and tested in terms of matched propagation delay time and maximum operating frequency.

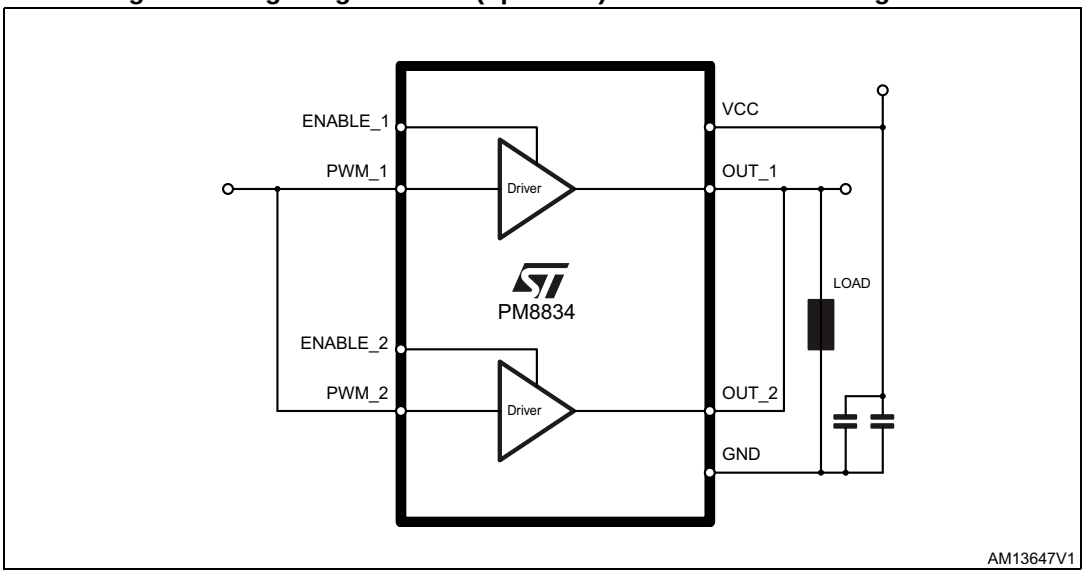
4.2 Output stage

The output stage of the PM8834 makes use of ST's proprietary lateral DMOS. Both N-DMOS and P-DMOS have been sized to exhibit high driving peak current as well as low ON-resistance. Typical peak current is 4 A while output resistances are 1 Ω and 0.7 Ω for P-DMOS and N-DMOS resistance respectively. The device features adaptive anti cross conduction protection. The PM8834 continuously monitors the status of the internal N-DMOS and P-DMOS. During a PWM transition, before switching on the desired DMOS, the device waits until the other DMOS is completely turned off. No static current will then flow from VCC to GND. During VCC startup, the internal N-DMOS is kept in an OFF state: with typical VCC rise time, with slope >2 V/ms, the OUT pins are maintained at low level under any operating condition. For VCC startup with very smooth rising edge, with slope < 2 V/ms, the OUT pins can track the VCC rising edge until the UVLO threshold is reached, but the voltage reached is maintained under 1.5 V under any operating condition.

4.3 Parallel output operation

For applications demanding high driving current capability (in excess of the 4 A provided by the single section), the PM8834 allows paralleling the operation of the two drivers in order to reach higher current, up to 8 A. This configuration is depicted in *Figure 4* where both PWM_1 and PWM_2 and OUT_1 and OUT_2 are tied together. The matching of internal propagation delays guarantees that the two drivers are switched on and off simultaneously.

Figure 4. Single high-current (up to 8 A) low-side driver configuration



4.4 Gate driver voltage flexibility

The PM8834 allows the user to freely select the gate drive voltage in order to optimize the efficiency of the application. The low-side MOSFET driving voltage depends on the voltage applied to VCC and can range between 5 V to 18 V.

5 Design guidelines

5.1 Output series resistance

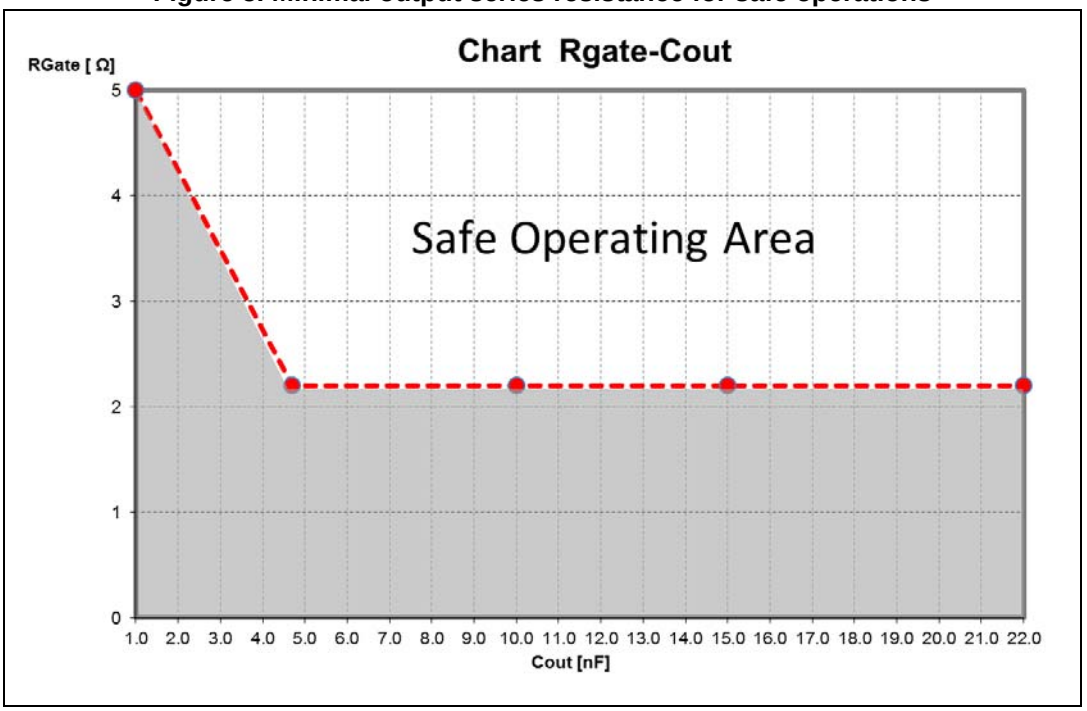
An output resistance is generally introduced to allow high-frequency operation without exceeding the maximum power dissipation of the driver package.

The value of the output resistance can be obtained as described in *Section 5.2*. For applications with supply voltages (VCC) greater than 15 V, with low capacitive loads (C_G<10 nF), exercise caution when designing with the PM8834.

In these circumstances, due to its high peak current capability, severe undervoltage on the output pins may occur, which, if not limited in some way, can violate the safe operating area of the output stage of the device. To avoid this phenomenon it is mandatory to add a gate resistor of at least 2.2Ω.

For applications with low capacitive loads (< 4.7 nF), exercise further caution when designing with the PM8834. Indication of the required minimum gate resistor vs. the capacitive load capable to assure safe operation of the PM8834 in a typical application is shown in *Figure 5*.

Figure 5. Minimal output series resistance for safe operations



Applications where the MOSFETs are placed away from the PM8834, or where the layout cannot foresee a wide copper plane of GND, an alternative way to clamp the undervoltage is to add externally a Schottky diode, with an anode connected to GND and a cathode to the driver output.

5.2 Power dissipation

The PM8834 embeds two high-current low-side drivers that can be used to drive high capacitive MOSFETs. This section estimates the power dissipated inside the device in normal applications.

Two main terms contribute to the device's power dissipation: bias power and the power of the driver.

- Bias power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply obtained as follows:

Equation 1

$$P_{DC} = V_{CC} \cdot I_{CC}$$

- The power of the driver is defined as the power needed by the driver to continuously switch ON and OFF the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs is dissipated by three main factors: external gate resistance, intrinsic MOSFET resistance and intrinsic driver resistance. This last term has to be determined to calculate the device power dissipation. The total power dissipated by each section to switch an external MOSFETs with gate charge Q_G is:

Equation 2

$$P_{SW} = F_{SW} \cdot (Q_G \cdot V_{CC})$$

When designing an application based on the PM8834 it is recommended to take into consideration the effect of the external gate resistors on the power dissipated by the driver. External gate resistors help the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor, resulting in a general cooling of the device.

Referring to *Figure 6*, a typical MOSFET driver can be represented by a push-pull output stage with two different MOSFETs: P-DMOS to drive the external gate high and N-DMOS to drive the external gate low (with their own Rds_{ON}: R_{hi}, R_{lo}). The external power MOSFET can be represented in this case as a capacitance (C_G) that stores the gate-charge (Q_G) required by the external power MOSFET to reach the driving voltage (V_{CC}). This capacitance is charged and discharged at the driver switching frequency F_{SW}.The total power P_{SW} is dissipated among the resistive components distributed along the driving path. According to the external gate resistance and the power MOSFET intrinsic gate resistance, the driver dissipates only a portion of P_{SW} (per section) as follows:

Equation 3

$$P_{SW} = \frac{1}{2} \cdot C_G \cdot (V_{CC})^2 \cdot F_{SW} \cdot \left(\frac{R_{hi}}{R_{hi} + R_{Gate} + R_i} + \frac{R_{lo}}{R_{lo} + R_{Gate} + R_i} \right)$$

The total power dissipated from the driver can then be determined as follows:

Equation 4

$$P = P_{DC} + 2 \cdot P_{SW}$$

Figure 6. Equivalent circuit for MOSFET driver

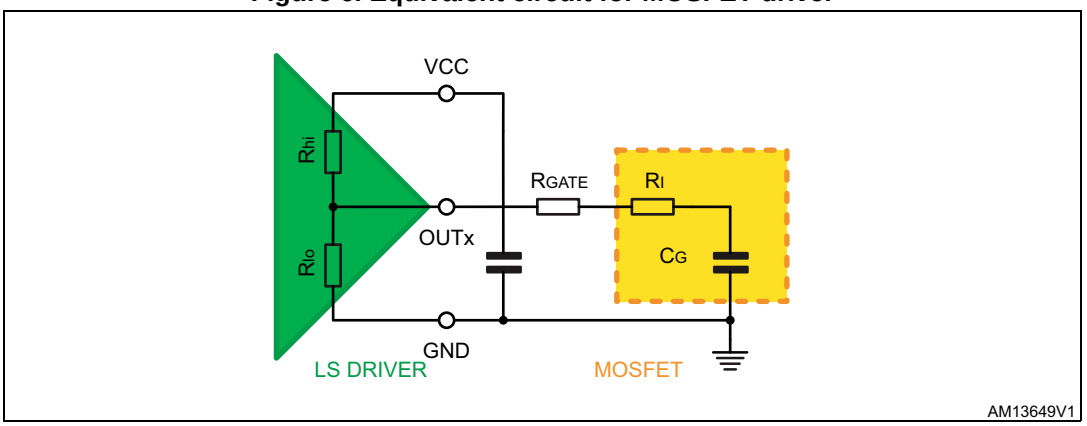


Figure 7. Power dissipation with load of 10 nF and 2.2 Ω gate resistor

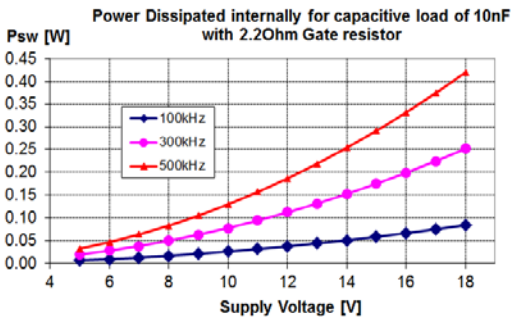
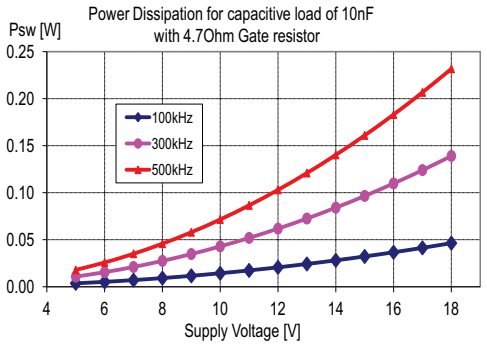


Figure 8. Power dissipation for capacitive load of 10 nF with 4.7 Ω gate resistor



5.3 Layout guidelines

The first priority when placing components for these applications has to be reserved to the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (also EMI and losses) power connections must be part of a power plane and must consist of wide and thick copper traces: the loop must be minimized.

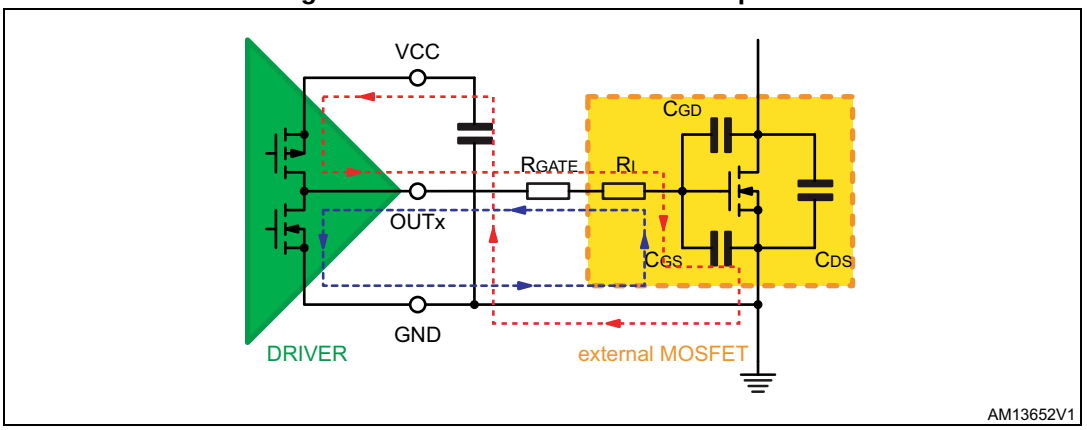
Traces between the driver and the MOSFETs should be short and wide to minimize the inductance of the traces, thus minimizing ringing in the driving signals. Moreover, the number of vias needs to be minimized in order to reduce the related parasitic effect.

Small signal components and connections to critical nodes of the application as well as bypass capacitors for the device supply are also important. Locate the bypass capacitor (V_{CC} capacitors) close to the device with the shortest possible loop and use wide copper traces to minimize parasitic inductance.

To improve heat dissipation, place a copper area under the IC. This copper area may be connected with other layers (if available) through vias to improve the thermal conductivity.

The combination of a copper pad, copper plane and vias under the driver allows the device to reach its best thermal performance.

Figure 9. Driver turn-on and turn-off paths



Traces between the driver and the MOSFETs should be short and wide to minimize the inductance of the traces, thus minimizing ringing in the driving signals. Moreover, the number of vias needs to be minimized in order to reduce the related parasitic effect.

As a general rule, place the driver no more than 1 inch away from its load (a rough estimation for the inductance of a PCB trace 1” long is about 20 nH).

Small signal components and connections to critical nodes of the application as well as bypass capacitors for the device supply are also important. Locate the bypass capacitor close to the device with the shortest possible loop and use wide copper traces to minimize the parasitic inductance. The use of low inductance SMD components such as ceramic chip capacitors is recommended.

It is suggested to maintain separated power traces and signal traces (output and input signals) in order to minimize the noise coupling and use star point grounding, with the source of the MOSFET as a star point.

Use (if available) a ground plane to provide noise shielding. Connect also the ground plane to the source of the MOSFET with a single point: the ground plane cannot be used as a path for any power loop.

In noisy environments, it is suggested to tie enable inputs of the driver to VCC in order to ensure that the output is enabled and to prevent coupling noise from causing malfunction in the output.

To improve heat dissipation, place a copper area under the IC. This copper area may be connected with other layers (if available) through vias to improve the thermal conductivity.

The combination of a copper pad, copper plane and vias under the driver allows the device to reach its best thermal performance.

Figure 10. Example of placement of external components - SO8 package

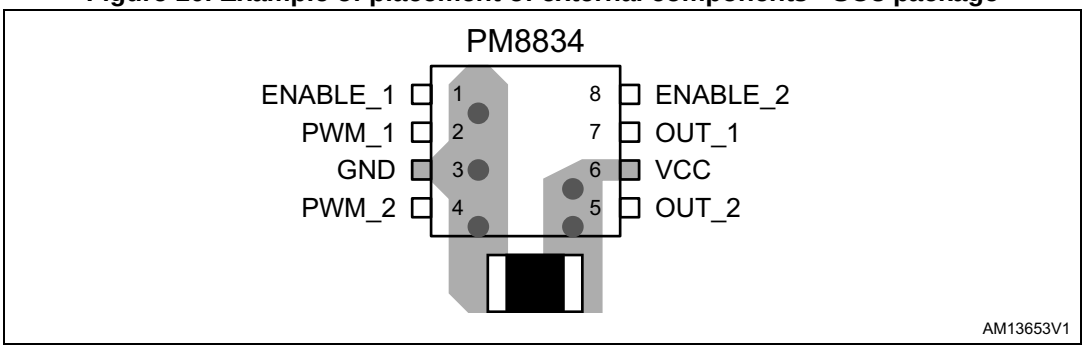
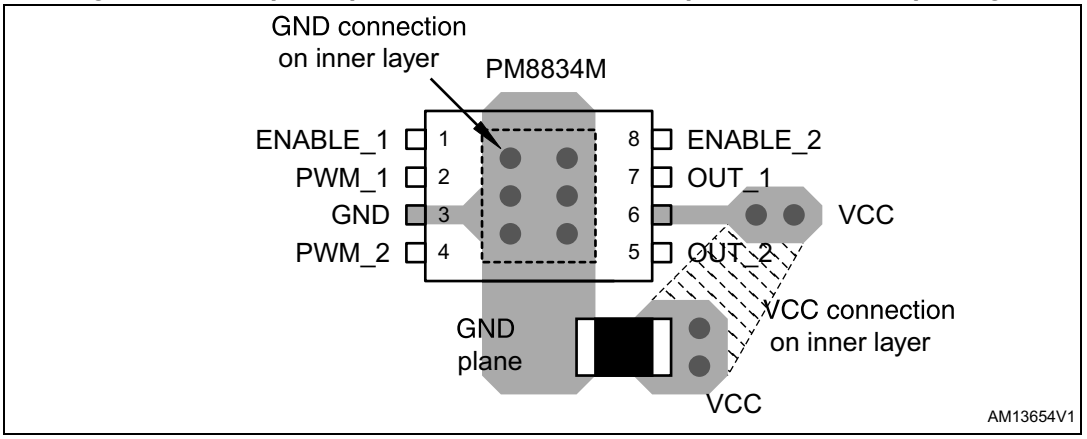


Figure 11. Example of placement of external components - MSOP8 package



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 12. SO-8 package outline

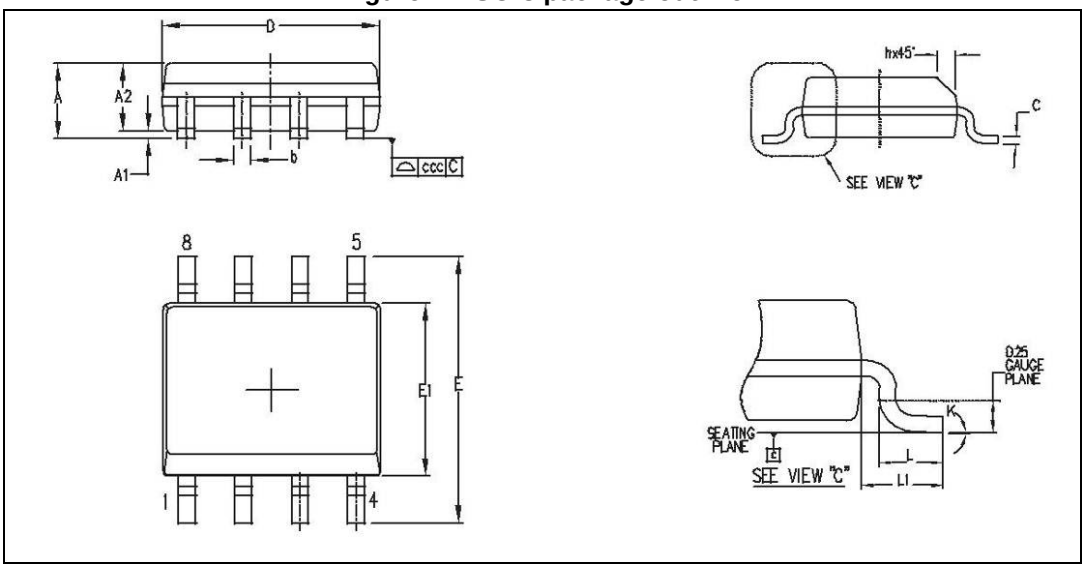


Table 6. SO-8 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

Figure 13. MSOP-8 package outline

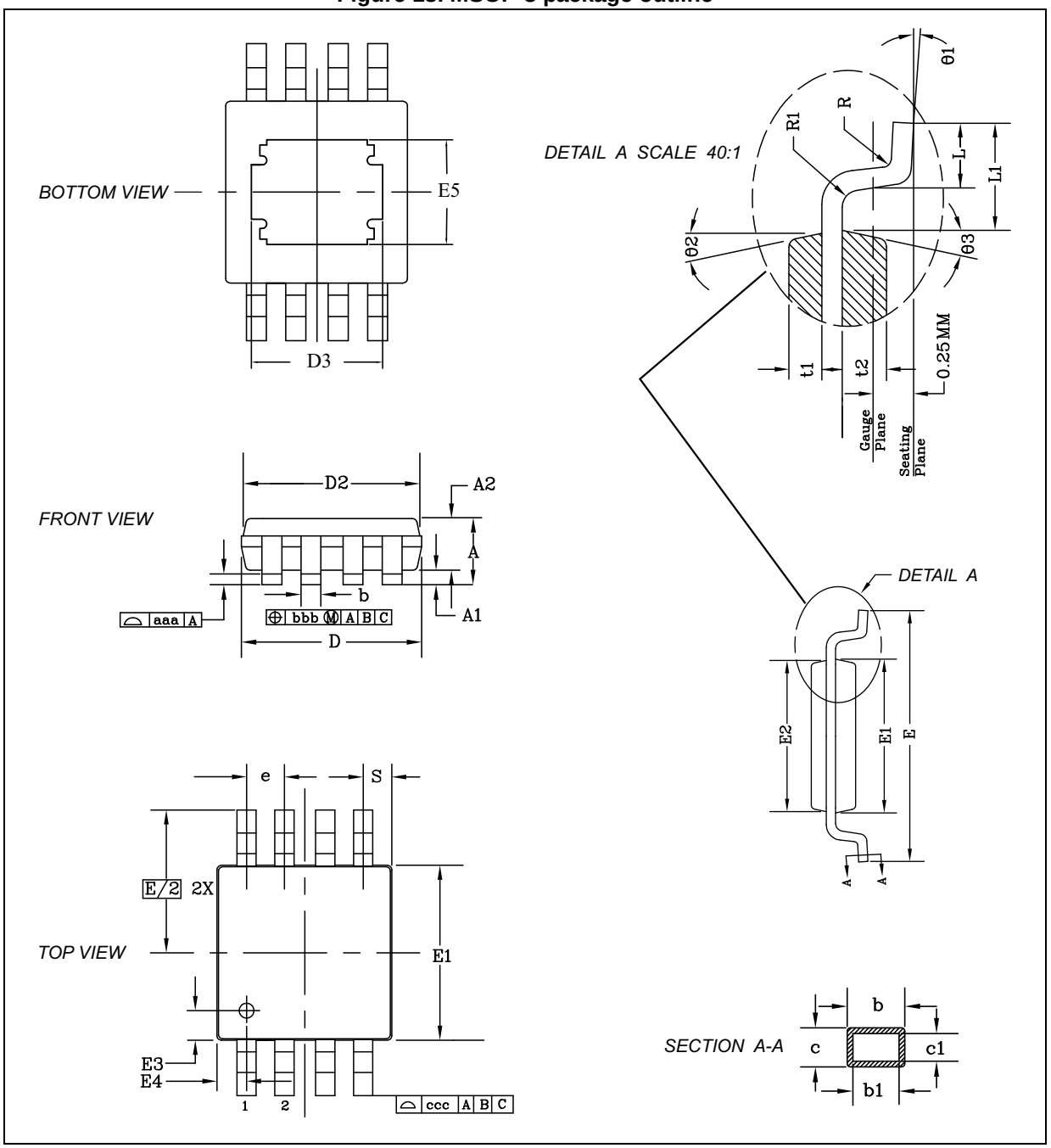
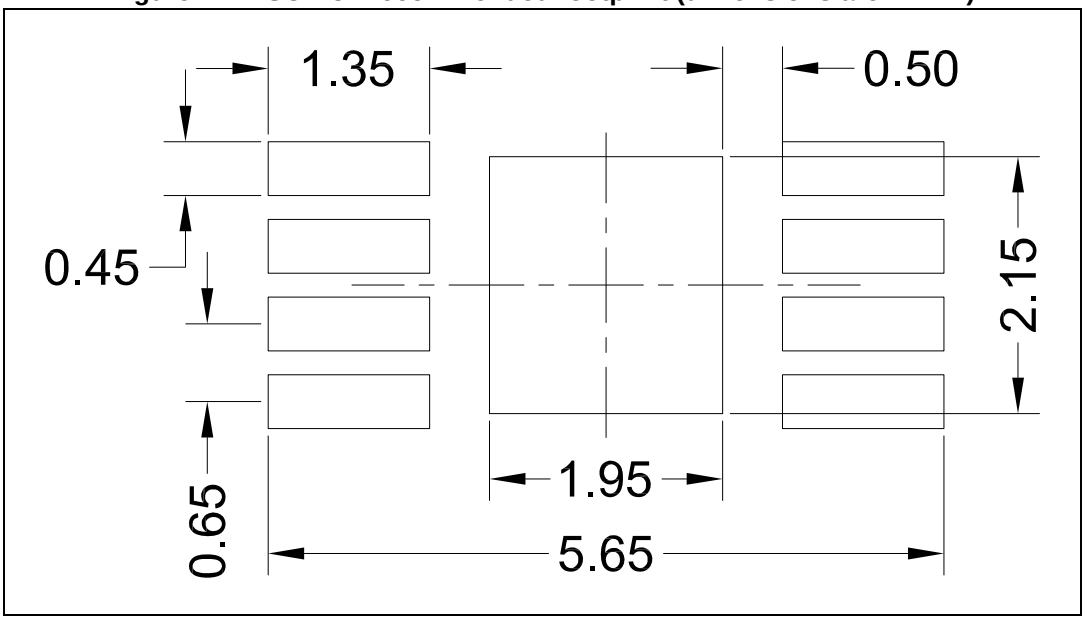


Table 7. MSOP-8L with exposed pad package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
Θ1	0°	3°	6°
Θ2	9°	12°	15°
Θ3	9°	12°	15°
A		1.10	
A1	0.05	0.10	0.15
A2	0.78	0.86	0.94
D	2.9	3.00	3.10
D2	2.85	2.95	3.05
E	4.75	4.90	5.05
e	0.65BSC		
S	0.525BSC		
D3	2.08	2.18	2.28
E5	1.63	1.73	1.73
E1	2.9	3.0	3.10
E2	2.85	2.95	3.05
E3	0.38	0.51	0.64
E4	0.38	0.51	0.64
R	0.07	0.15	0.3
R1	0.07	0.15	0.3
t1	0.23	0.31	0.39
t2	0.33	0.41	0.49
b	0.25	0.33	0.7
b1	0.25	0.30	0.35
c	0.13	0.18	0.23
c1	0.13	0.15	0.18
L	0.4	0.55	0.7
aaa	0.10		
bbb	0.08		
ccc	0.25		

1. Dimension “D” and “D2” does not include mold flash protrusion or gate burrs.
2. Dimension “E1” and “E2” does not include interlead flash or protrusion.
3. Package outline exclusive of metal burr dimensions.
4. Dimension for “D2” and “E2” are for top package and “D” and “E1” are for bottom package.
5. Cross section A-A to be determined at 0.13 to 0.25mm from the lead tip.

Figure 14. MSOP-8L recommended footprint (dimensions are in mm)



7 Revision history

Table 8. Document revision history

Date	Revision	Changes
13-Oct-2008	1	Initial release.
21-Oct-2009	2	Updated *Figure 1*, *Table 2*, *Table 5* and *Section 4.1.2*
30-Jul-2013	3	Modified *Table 1*, *Table 4*, *Section 4* and *Section 6: Package information*. Minor textual changes.
21-Oct-2014	4	Updated *Table 2 on page 5* (updated ENABLE_1, PWM_1, PWM_2, and ENABLE_2 pin functions). Updated *Section 4.1.2: Enable pins on page 10*. Updated *Section 5.1: Output series resistance on page 12* (updated entire section and *Figure 5* - updated title and replaced by new figure). Updated *Section 5.2: Power dissipation on page 13* and *Figure 7 on page 14* (updated title and replaced by new figure, minor text modifications). Updated *Section 5.3: Layout guidelines on page 15*. Updated *Section 6: Package information on page 17* (updated titles, reversed order of *Figure 12* and *Table 6*, *Figure 13* and *Table 7*, updated titles and headers of *Table 6* and *Table 7*). Minor modifications throughout document.
24-Jul-2015	5	Updated *Table 7: MSOP-8L with exposed pad package mechanical data* and corresponding package outline drawings in *Figure 13*. Added *Figure 14*. Minor text edits.