

**Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

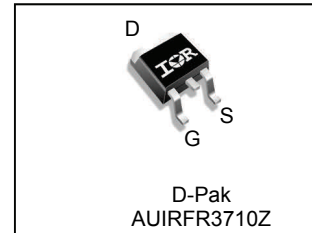
HEXFET® Power MOSFET



$V_{DSS}$		<b>100V</b>
$R_{DS(on)}$	<b>max.</b>	<b>18mΩ</b>
$I_D$ (Silicon Limited)		<b>56A</b>
$I_D$ (Package Limited)		<b>42A</b>

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFR3710Z	D-Pak	Tube	75	AUIRFR3710Z
		Tape and Reel Left	3000	AUIRFR3710ZTRL

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	56	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	39	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	42	
$I_{DM}$	Pulsed Drain Current ①	220	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	150	mJ
$E_{AS}$ (Tested)	Single Pulse Avalanche Energy Tested Value ③	200	
$I_{AR}$	Avalanche Current ④	See Fig.15,16, 12a, 12b	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	1.05	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mount) ⑦	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

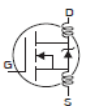
HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

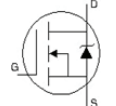
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.088	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	15	18	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 33A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Trans conductance	39	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 33A ③
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Q <sub>g</sub>	Total Gate Charge	—	69	100	nC	I <sub>D</sub> = 33A
Q <sub>gs</sub>	Gate-to-Source Charge	—	15	—		V <sub>DS</sub> = 80V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	25	—		V <sub>GS</sub> = 10V ③
t <sub>d(on)</sub>	Turn-On Delay Time	—	14	—	ns	V <sub>DD</sub> = 50V
t <sub>r</sub>	Rise Time	—	43	—		I <sub>D</sub> = 33A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	53	—		R <sub>G</sub> = 6.8Ω
t <sub>f</sub>	Fall Time	—	42	—		V <sub>GS</sub> = 10V ③
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	2930	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	290	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	180	—		f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1200	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	180	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 80V f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	430	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V ④

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	56	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	220		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 33A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	35	53	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 33A, V <sub>DD</sub> = 50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	41	62	nC	di/dt = 100A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.28mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 33A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ④ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>
- ⑤ Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, starting T<sub>J</sub> = 25°C, L = 0.28mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 33A, V<sub>GS</sub> = 10V.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.

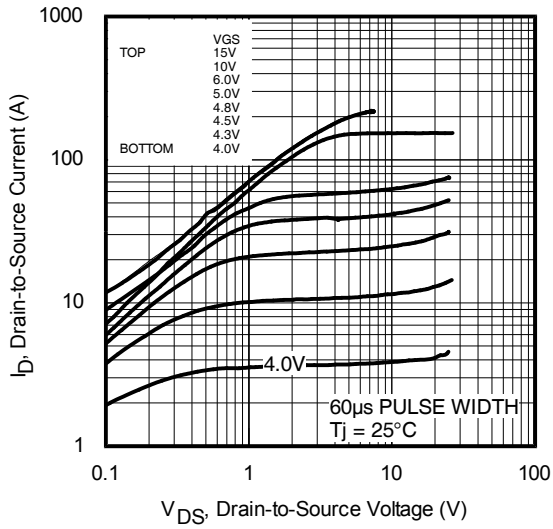


Fig. 1 Typical Output Characteristics

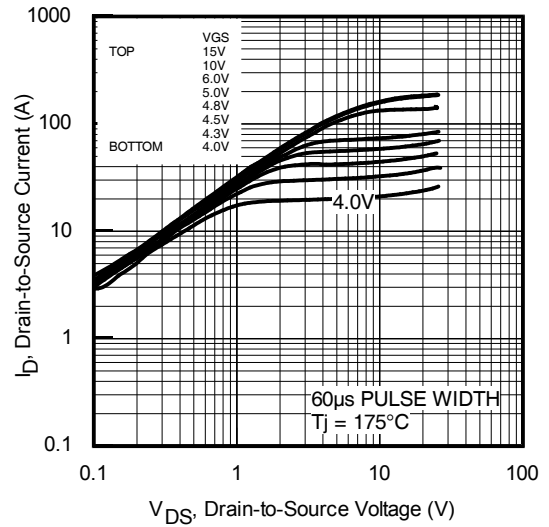


Fig. 2 Typical Output Characteristics

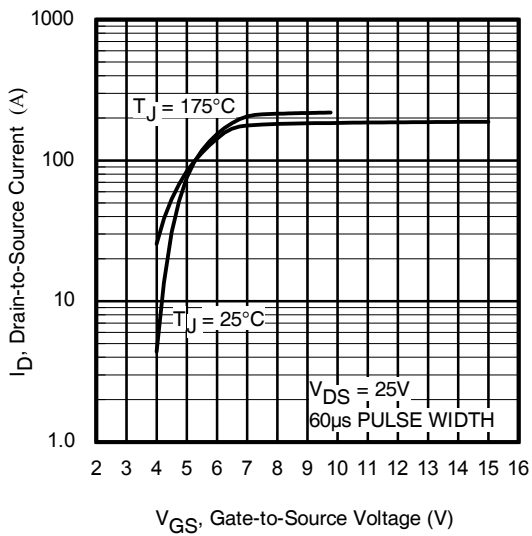


Fig. 3 Typical Transfer Characteristics

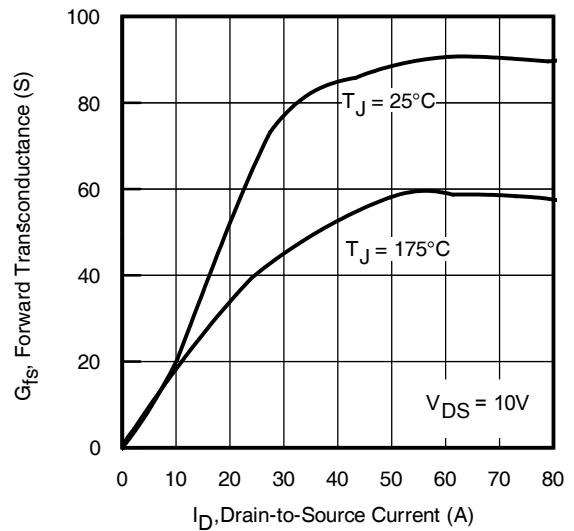
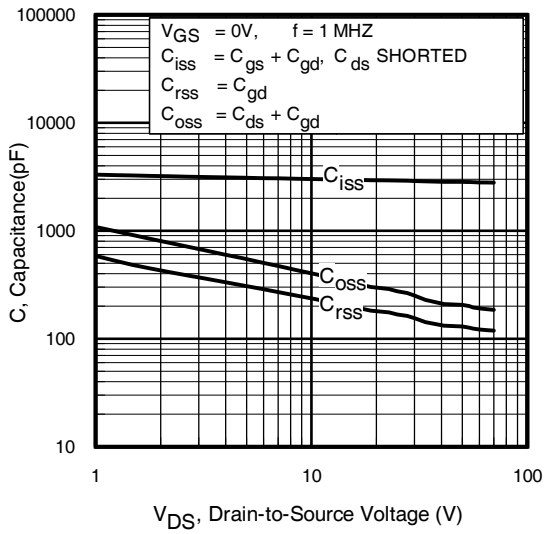
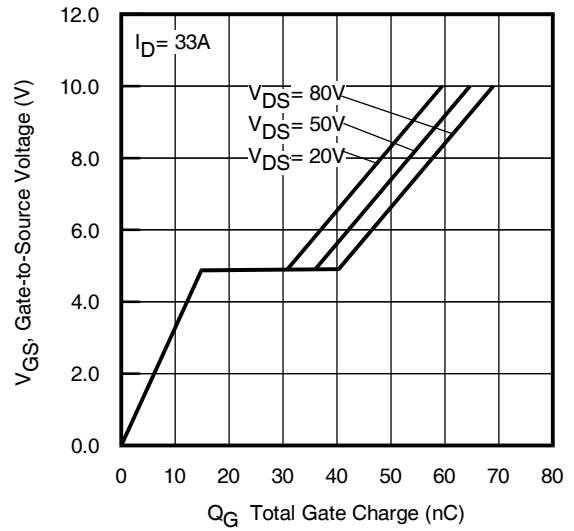


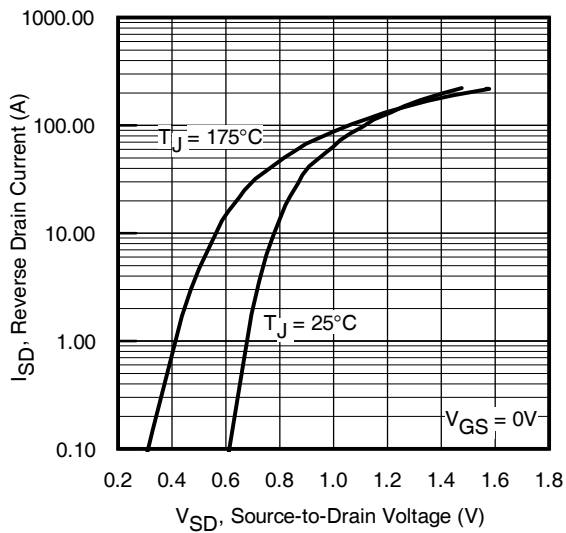
Fig. 4 Typical Forward Trans conductance Vs. Drain Current



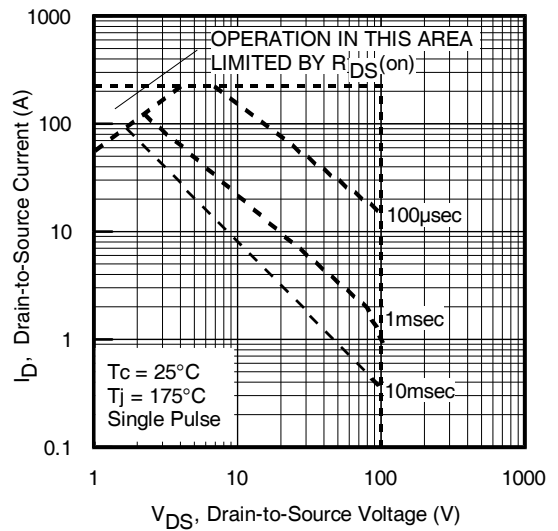
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



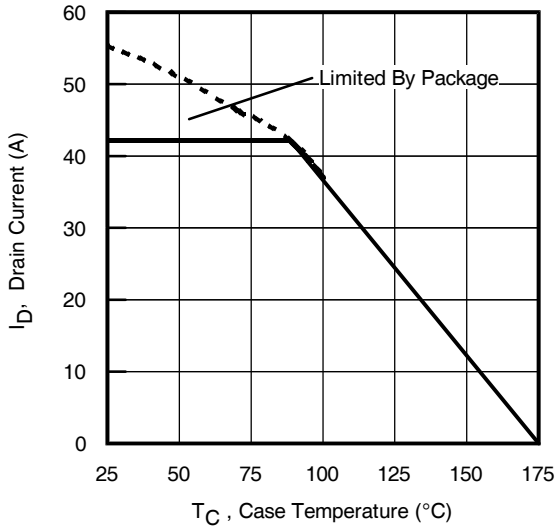
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



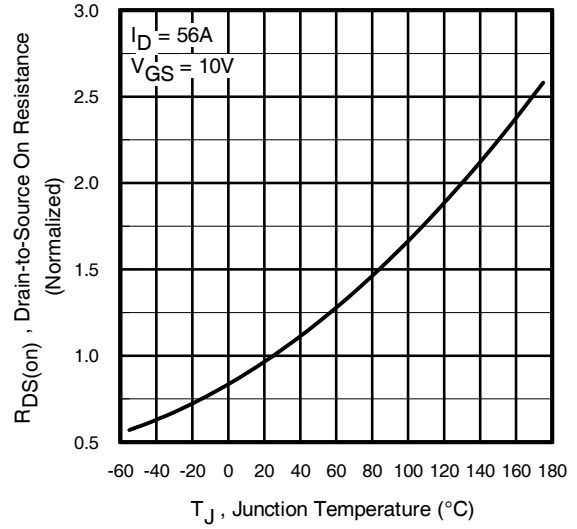
**Fig 7.** Typical Source-to-Drain Diode Forward Voltage



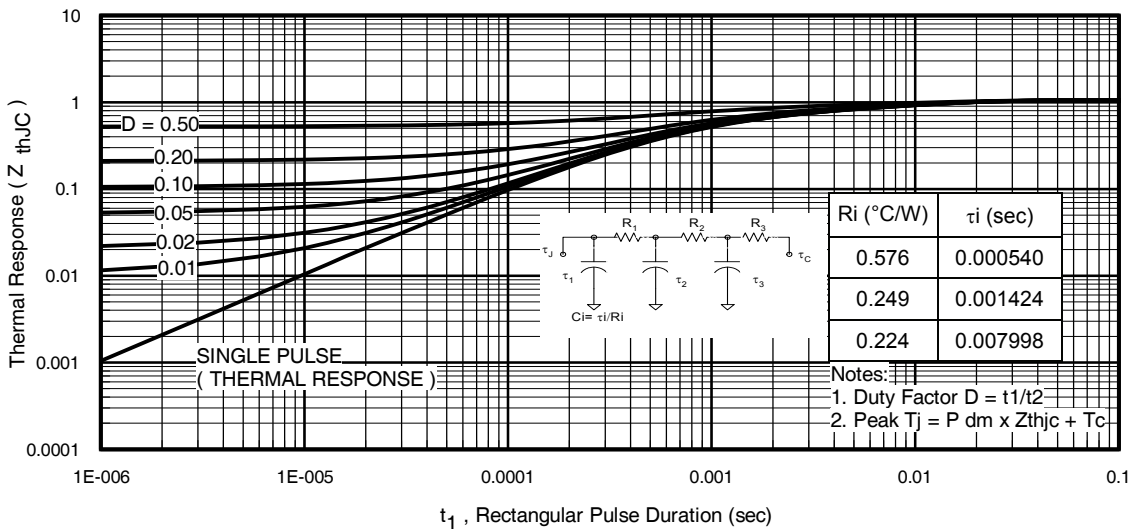
**Fig 8.** Maximum Safe Operating Area



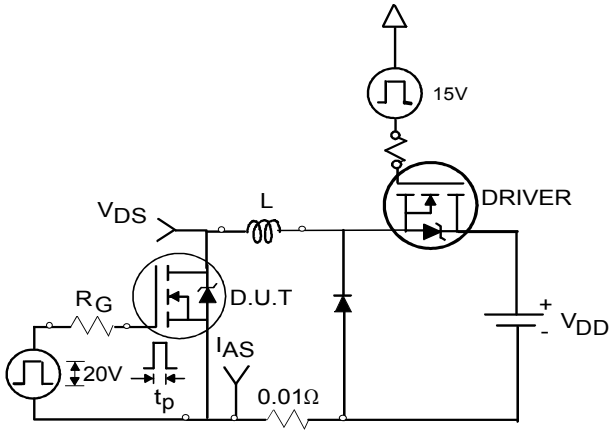
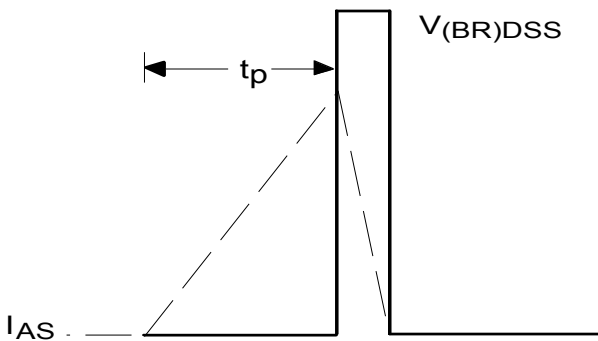
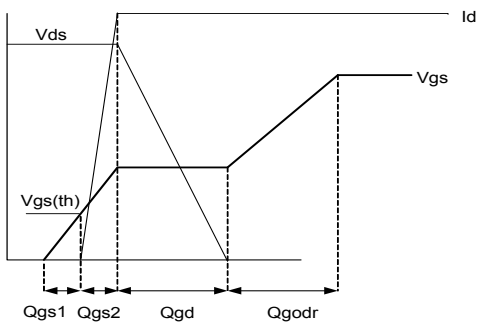
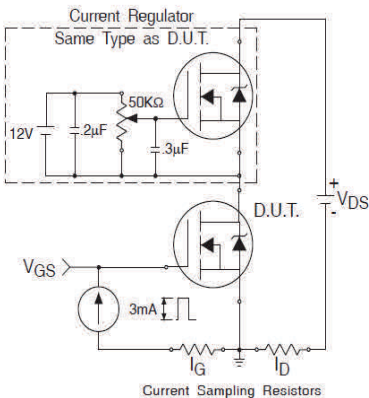
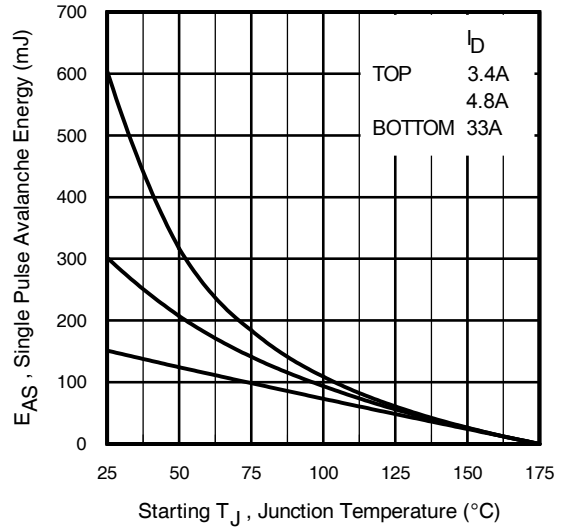
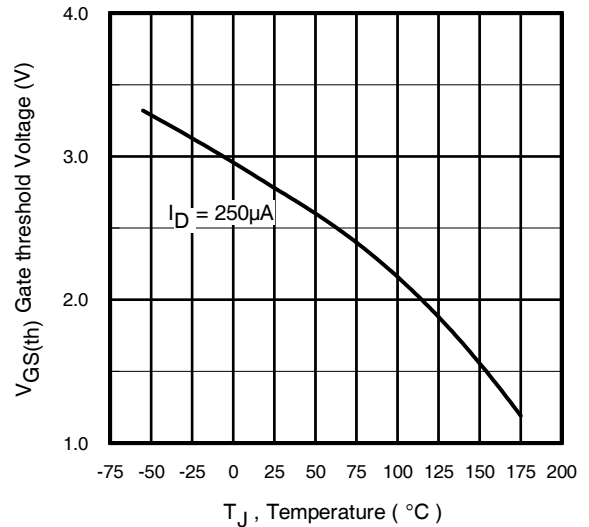
**Fig 9.** Maximum Drain Current Vs. Case Temperature

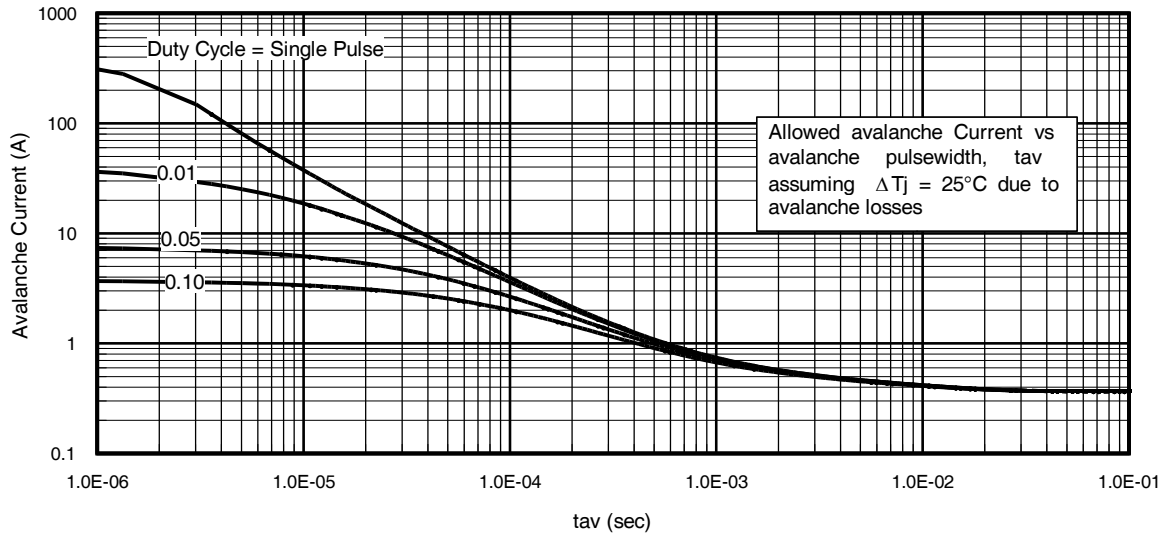
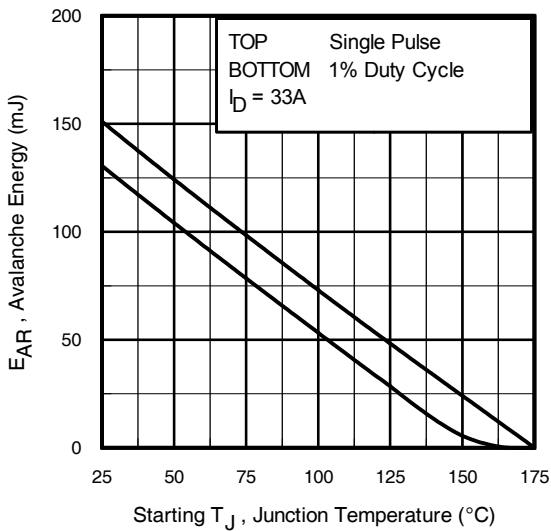


**Fig 10.** Normalized On-Resistance Vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12a. Unclamped Inductive Test Circuit**

**Fig 12b. Unclamped Inductive Waveforms**

**Fig 13a. Gate Charge Waveform**

**Fig 13b. Gate Charge Test Circuit**

**Fig 12c. Maximum Avalanche Energy vs. Drain Current**

**Fig 14. Threshold Voltage Vs. Temperature**

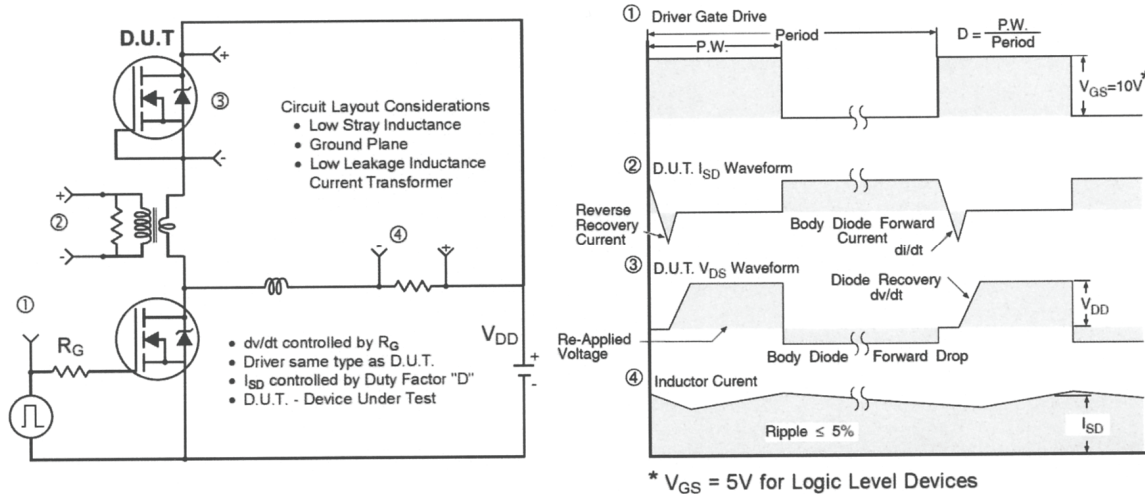

**Fig 15. Typical Avalanche Current Vs. Pulse width**

**Fig 16. Maximum Avalanche Energy Vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**
**(For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

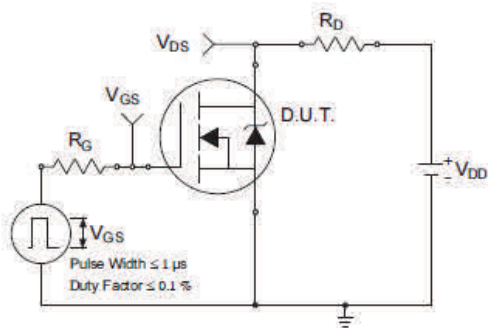
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

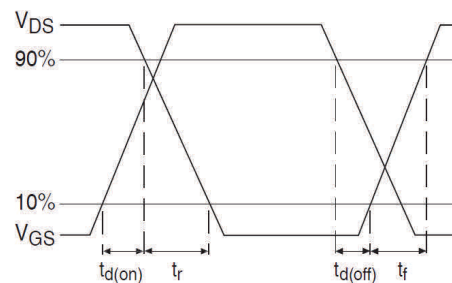
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms



**D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
- △ LEAD DIMENSION UNCONTROLLED IN L5.
- △ DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- △ DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- △ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

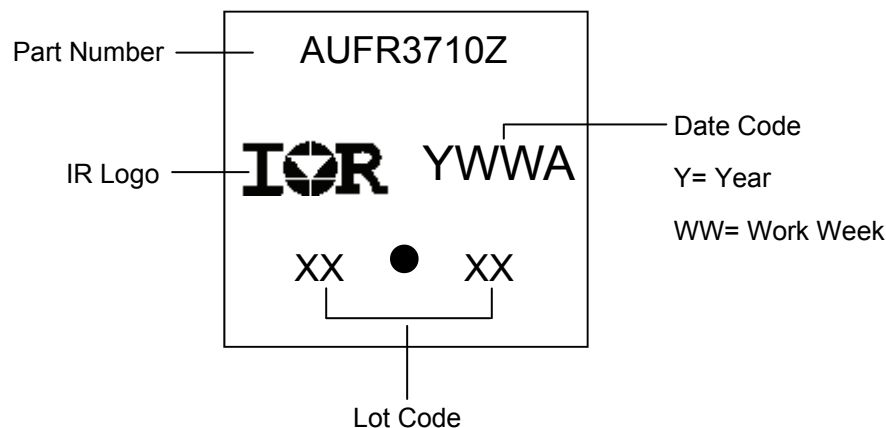
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
φ	0"	10"	0"	10"	
φ1	0"	15"	0"	15"	
φ2	25"	35"	25"	35"	

**LEAD ASSIGNMENTS**
**HEXFET**

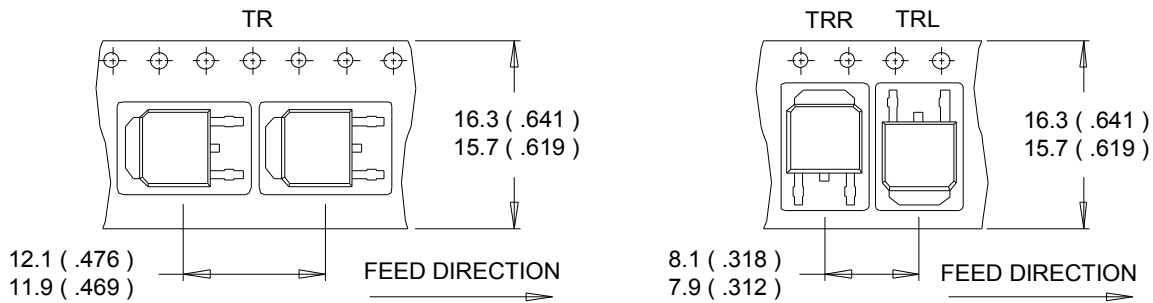
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBT & CoPAK**

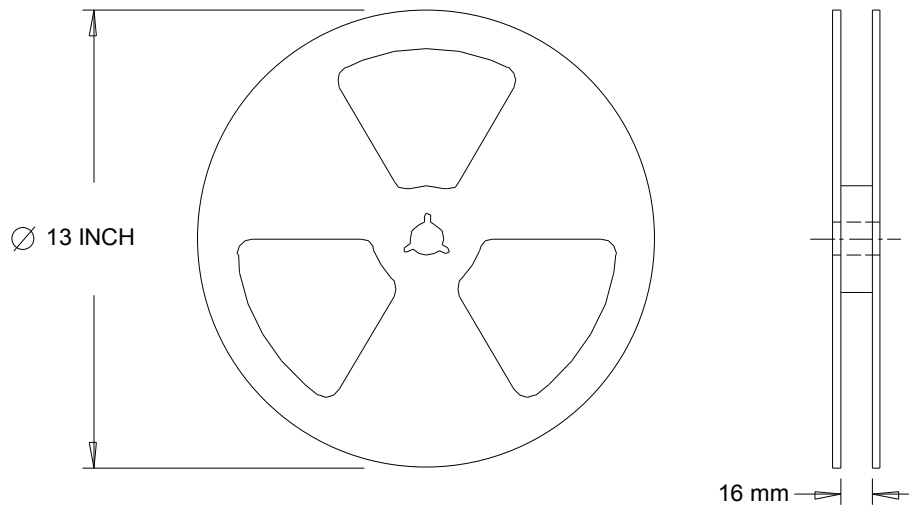
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

**D-Pak (TO-252AA) Part Marking Information**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))**

**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		D-Pak	MSL1
<b>ESD</b>	Machine Model	Class M4 <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H1C <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C3 <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
11/23/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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