

# AUIRLR3915

HEXFET® Power MOSFET

### **Features**

- Advanced Plannar Technology
- Logic-Level Gate Drive
- Low On-Resistance
- 175°C Operating Temperature
- Fast Switching

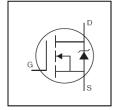
Description

applications.

- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other

- · Lead-Free, RoHS Compliant
- Automotive Qualified \*



V <sub>DSS</sub>		55V
R <sub>DS(on)</sub>	typ.	12mΩ
	max.	14mΩ
D (Silicon Lim	nited)	61A
D (Package Li	imited)	30A

# D S G D-Pak AUIRLR3915

G	D	S
Gate	Drain	Source

G	D		S		
	D-Pak AUIRLR3915				
	S G	<b>№</b> 3			

Page part number   Backage Tune		Standard Pack		Orderable Part Number	
Base part number	Package Type	Form	Quantity	Orderable Part Number	
VIIIDI DOME	D. Dok	Tube	75	AUIRLR3915	
AUIRLR3915	D-Pak	Tape and Reel Left	3000	AUIRLR3915TRL	

## **Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	61	
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	43	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	30	Α
I <sub>DM</sub>	Pulsed Drain Current ①	240	
P <sub>D</sub> @T <sub>C</sub> = 25°C	Maximum Power Dissipation	120	W
	Linear Derating Factor	0.77	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 16	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②	200	
E <sub>AS</sub> (Tested)	Single Pulse Avalanche Energy Tested Value ⑦	600	- mJ
I <sub>AR</sub>	Avalanche Current ①	See Fig.15,16, 12a, 12b	Α
E <sub>AR</sub>	Repetitive Avalanche Energy ®		mJ
TJ	Operating Junction and	-55 to + 175	
T <sub>STG</sub>	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

### Thermal Resistance

Symbol Parameter		Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case		1.3	
$R_{ heta JA}$	Junction-to-Ambient ( PCB Mount) ®		50	°C/W
$R_{\theta JA}$	Junction-to-Ambient		110	

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<sup>\*</sup>Qualification standards can be found at www.infineon.com



# Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.057		V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
D	Statia Drain to Source On Begintance		12	14		$V_{GS} = 10V, I_D = 30A $ ④
$R_{DS(on)}$	Static Drain-to-Source On-Resistance		14	17	mΩ	$V_{GS} = 5.0V, I_D = 26A $ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0		3.0	٧	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
gfs	Forward Trans conductance	42			S	$V_{DS} = 25V, I_{D} = 30A \oplus$
ı	Drain to Source Leakage Current			20	μA	$V_{DS} = 55V, V_{GS} = 0V$
IDSS	Drain-to-Source Leakage Current			250	μΑ	$V_{DS} = 55V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
ı	Gate-to-Source Forward Leakage			200	nA	V <sub>GS</sub> = 16V
I <sub>GSS</sub>	Gate-to-Source Reverse Leakage			-200	IIA	V <sub>GS</sub> = -16V

# Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

Total Gate Charge		61	92		I <sub>D</sub> = 30A
Gate-to-Source Charge		9.0	14	nC	$V_{DS} = 44V$
Gate-to-Drain Charge		17	25		V <sub>GS</sub> = 10V ④
Turn-On Delay Time		7.4			$V_{DD} = 28V$
Rise Time		51		20	$I_D = 30A$
Turn-Off Delay Time		83		115	$R_G = 8.5\Omega$
Fall Time		100			V <sub>GS</sub> = 10V4
Internal Drain Inductance		4.5			Between lead, 6mm (0.25in.)
Internal Source Inductance		7.5			from package and center of die contact
Input Capacitance		1870			$V_{GS} = 0V$
Output Capacitance		390			$V_{DS} = 25V$
Reverse Transfer Capacitance		74		nΕ	f = 1.0MHz, See Fig. 5
Output Capacitance		2380		рΓ	$V_{GS} = 0V$ , $V_{DS} = 1.0V$ $f = 1.0MHz$
Output Capacitance		290			$V_{GS} = 0V$ , $V_{DS} = 44V$ $f = 1.0MHz$
Effective Output Capacitance ©		540			$V_{GS} = 0V, V_{DS} = 0V \text{ to } 44V$
	Gate-to-Source Charge Gate-to-Drain Charge Turn-On Delay Time Rise Time Turn-Off Delay Time Fall Time Internal Drain Inductance Internal Source Inductance Input Capacitance Output Capacitance Reverse Transfer Capacitance Output Capacitance Output Capacitance Output Capacitance Output Capacitance Output Capacitance	Gate-to-Source Charge —— Gate-to-Drain Charge —— Turn-On Delay Time —— Rise Time —— Turn-Off Delay Time —— Fall Time —— Internal Drain Inductance —— Internal Source Inductance —— Input Capacitance —— Output Capacitance —— Reverse Transfer Capacitance —— Output Capacitance ——	Gate-to-Source Charge         —         9.0           Gate-to-Drain Charge         —         17           Turn-On Delay Time         —         7.4           Rise Time         —         51           Turn-Off Delay Time         —         83           Fall Time         —         100           Internal Drain Inductance         —         4.5           Internal Source Inductance         —         7.5           Input Capacitance         —         390           Reverse Transfer Capacitance         —         74           Output Capacitance         —         2380           Output Capacitance         —         290	Gate-to-Source Charge         —         9.0         14           Gate-to-Drain Charge         —         17         25           Turn-On Delay Time         —         7.4         —           Rise Time         —         51         —           Turn-Off Delay Time         —         83         —           Fall Time         —         100         —           Internal Drain Inductance         —         4.5         —           Internal Source Inductance         —         7.5         —           Input Capacitance         —         390         —           Output Capacitance         —         74         —           Output Capacitance         —         2380         —           Output Capacitance         —         290         —	Gate-to-Source Charge         —         9.0         14         nC           Gate-to-Drain Charge         —         17         25           Turn-On Delay Time         —         7.4         —           Rise Time         —         51         —           Turn-Off Delay Time         —         83         —           Fall Time         —         100         —           Internal Drain Inductance         —         4.5         —           Internal Source Inductance         —         7.5         —           Input Capacitance         —         390         —           Output Capacitance         —         74         —           Output Capacitance         —         2380         —           Output Capacitance         —         290         —

### **Diode Characteristics**

	Parameter	Min.	Тур.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)			61		MOSFET symbol showing the
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①			240		integral reverse p-n junction diode.
$V_{SD}$	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S = 30A, V_{GS} = 0V $
t <sub>rr</sub>	Reverse Recovery Time		62	93	ns	$T_J = 25^{\circ}C$ , $I_F = 30A$ , $V_{DD} = 25V$
$Q_{rr}$	Reverse Recovery Charge		110	170	nC	di/dt = 100A/µs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsio	turn-or	time is	negligil	ole (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )

# Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- $\odot$  Limited by  $T_{Jmax}$ , starting  $T_J$  = 25°C, L = 0.45mH,  $R_G$  = 25 $\Omega$ ,  $I_{AS}$  = 30A,  $V_{GS}$  =10V. Part not recommended for use above this value.
- $\label{eq:local_local_local_local} \ensuremath{\Im} \quad I_{SD} \leq 30 \mbox{A, di/dt} \leq 280 \mbox{A/} \mu \mbox{s, } V_{DD} \leq V_{(BR)DSS}, \ T_J \leq 175 \mbox{°C}.$
- ④ Pulse width  $\leq$  1.0ms; duty cycle  $\leq$  2%.
- $\circ$  Coss eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- © Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- $\odot$  This value determined from sample failure population, starting T<sub>J</sub> = 25°C, L = 0.45mH, R<sub>G</sub> = 25 $\Omega$ , I<sub>AS</sub> = 30A, V<sub>GS</sub> =10V.
- When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- <sup>®</sup> R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.



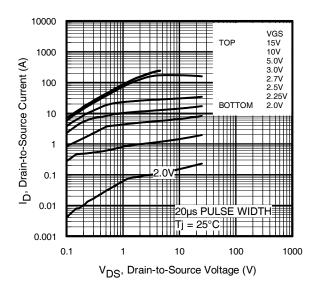


Fig. 1 Typical Output Characteristics

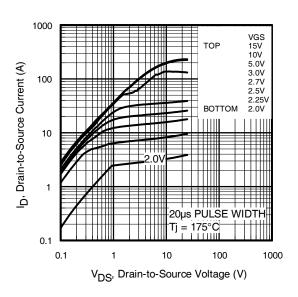


Fig. 2 Typical Output Characteristics

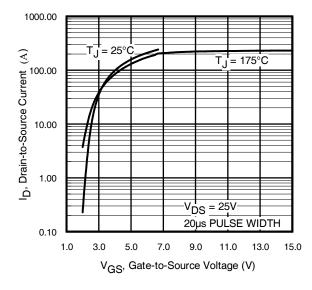
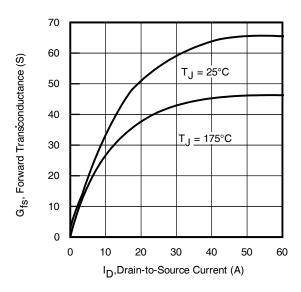
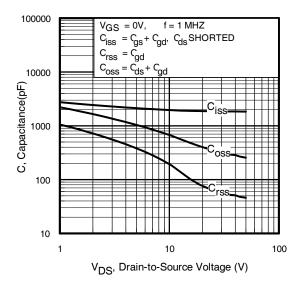


Fig. 3 Typical Transfer Characteristics

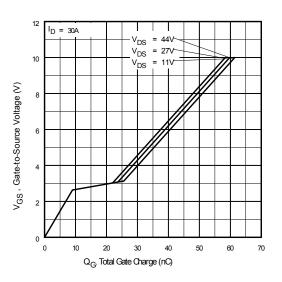


**Fig. 4** Typical Forward Trans conductance Vs. Drain Current





**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

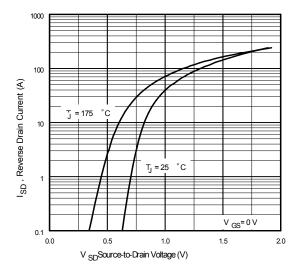


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

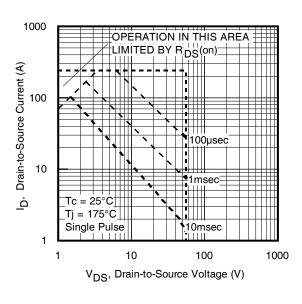
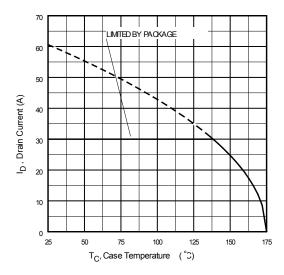
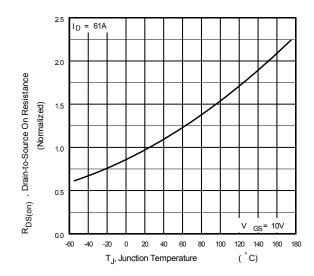


Fig 8. Maximum Safe Operating Area







**Fig 9.** Maximum Drain Current Vs. Case Temperature

**Fig 10.** Normalized On-Resistance Vs. Temperature

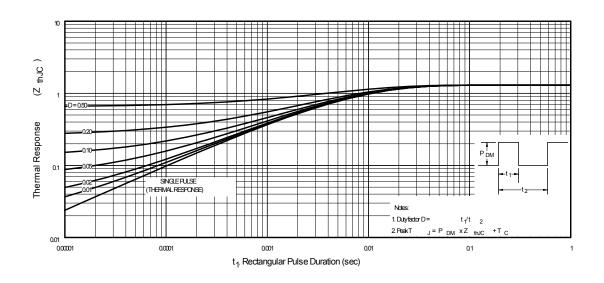


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



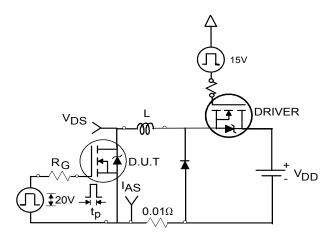


Fig 12a. Unclamped Inductive Test Circuit

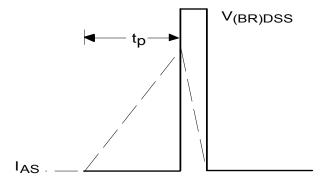


Fig 12b. Unclamped Inductive Waveforms

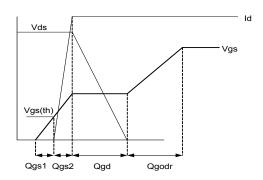


Fig 13a. Gate Charge Waveform

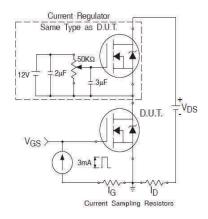
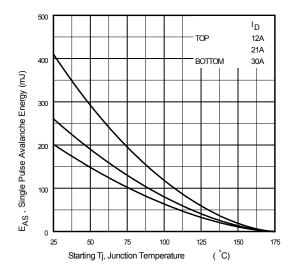


Fig 13b. Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

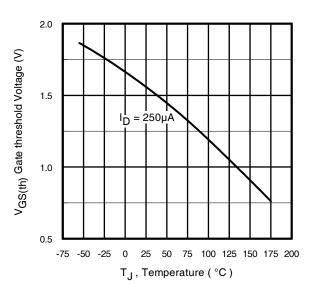


Fig 14. Threshold Voltage Vs. Temperature



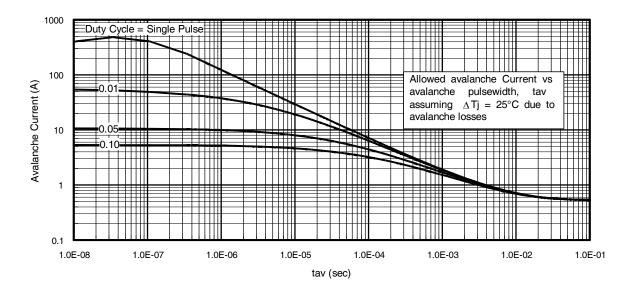
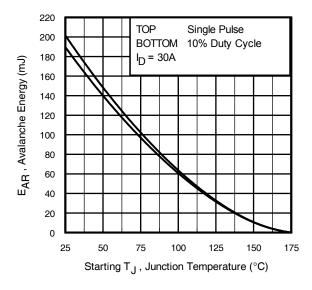


Fig 15. Typical Avalanche Current Vs. Pulse width



**Fig 16.** Maximum Avalanche Energy Vs. Temperature

### Notes on Repetitive Avalanche Curves, Figures 15, 16:

# (For further info, see AN-1005 at www.infineon.com)

- Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T<sub>imax</sub>. This is validated for every part type.
- 2. Safe operation in Avalanche is allowed as long as T<sub>jmax</sub> is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
- 4. PD (ave) = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. lav = Allowable avalanche current.
- 7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).

tav = Average time in avalanche.

D = Duty cycle in avalanche =  $t_{av} \cdot f$ 

ZthJC(D, tav) = Transient thermal resistance, see Figures 13)

$$\begin{split} P_{D \; (ave)} &= 1/2 \; (\; 1.3 \cdot BV \cdot I_{av}) = \Delta T / \; Z_{thJC} \\ I_{av} &= 2\Delta T / \; [1.3 \cdot BV \cdot Z_{th}] \\ E_{AS \; (AR)} &= P_{D \; (ave)} \cdot t_{av} \end{split}$$



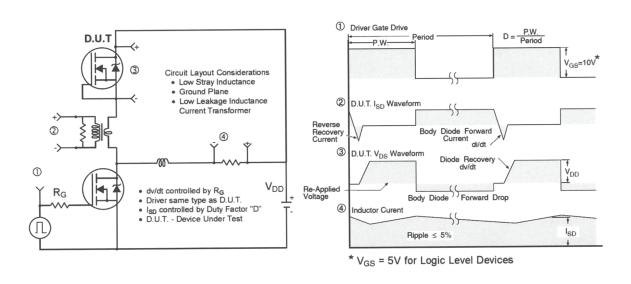


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

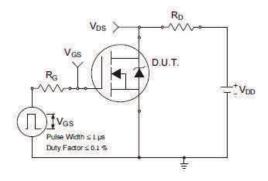


Fig 18a. Switching Time Test Circuit

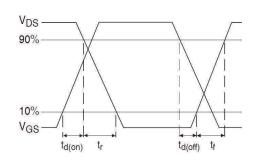
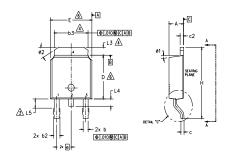


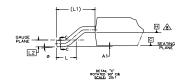
Fig 18b. Switching Time Waveforms

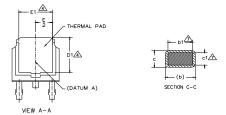


# D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))









#### NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 1 LEAD DIMENSION UNCONTROLLED IN L5.
- A- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.— SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- Limited Dimension D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- ⚠- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- ♠ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

S		DIMENSIONS				
M B O	MILLIM	ETERS	INC	HES	O T	
O L	MIN.	MAX.	MIN.	MAX.	E S	
Α	2.18	2.39	.086	.094		
A1	-	0.13	-	.005		
b	0.64	0.89	.025	.035		
ь1	0.65	0.79	.025	.031	7	
b2	0.76	1.14	.030	.045		
b3	4.95	5.46	.195	.215	4	
С	0.46	0.61	.018	.024		
c1	0.41	0.56	.016	.022	7	
c2	0.46	0.89	.018	.035		
D	5.97	6.22	.235	.245	6	
D1	5.21	-	.205	-	4	
Ε	6.35	6.73	.250	.265	6	
E1	4.32	-	.170	-	4	
е	2.29	BSC	.090	BSC		
Н	9.40	10.41	.370	.410		
L	1.40	1.78	.055	.070		
L1	2.74	BSC	.108	REF.		
L2	0.51	BSC	.020	BSC		
L3	0.89	1.27	.035	.050	4	
L4	-	1.02	_	.040		
L5	1.14	1.52	.045	.060	3	
ø	0.	10°	0,	10°		
ø1	0.	15*	0,	15*		
ø2	25*	35*	25*	35*		

#### LEAD ASSIGNMENTS

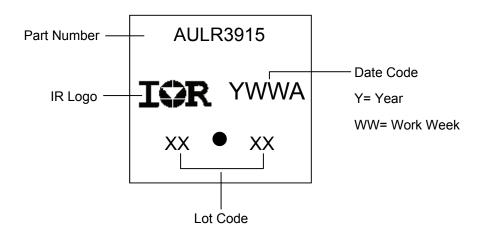
#### **HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE 4.- DRAIN
- 4. DIVAII

#### IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER 4.- COLLECTOR

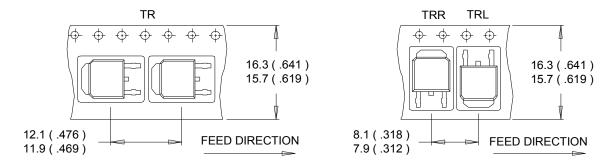
D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

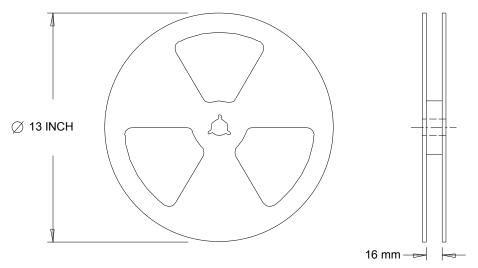


# D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))



#### NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



# NOTES:

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <a href="http://www.irf.com/package/">http://www.irf.com/package/</a>



#### **Qualification Information**

			Automotive (per AEC-Q101)				
Qualification Level		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.					
Moisture	Sensitivity Level	D-Pak	MSL1				
	Manakina Mandal	Class M2 (+/- 200V) <sup>†</sup>					
	Machine Model	AEC-Q101-002					
FOR	Livers on Dody Model	Class H1B (+/- 1000V) <sup>†</sup>					
ESD	Human Body Model	AEC-Q101-001					
	Olanova d Davis a Madal		Class C5 (+/- 2000V) <sup>†</sup>				
Charged Device Model		AEC-Q101-005					
RoHS Compliant		Yes					

† Highest passing voltage.

## **Revision History**

Date	Comments		
12/14/2015	Updated datasheet with corporate template		
12/14/2013	Corrected ordering table on page 1.		

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