TLE826xE/-2E

Universal System Basis Chip Family

Errata Sheet

Rev. 1.00, 2012-02-28

Automotive Power

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TLE826xE/-2E Family

Reference: Data Sheets Rev. 1.0

During SBC Family introduction datasheet deviations were observed.
These deviations are described in this document.

Products effected are as follows:

- TLE8261E
- TLE8261-2E
- TLE8262E
- TLE8262-2E
- TLE8263E
- TLE8263-2E
- TLE8264E
- TLE8264-2E

This document describes the errata in relation to the Data Sheet Rev. 1.0 of the respective above listed product.

Revision History: Previous Version:

Major Changes:

1 Overview

1.1 Unexpected Failure Detection

1.1.1 Possible Wake from SBC Sleep Mode

- **Occurrence: L**imp **H**ome (LH) output is activated and the device is sent to SBC Sleep Mode with LH active
- **Behavior:** device restart after ~4 min and unexpected SPI diagnosis bit settings
- **Impact:** transition to SBC Normal Mode thus resulting in an undesired SBC mode change
- **Workaround:** always disable LH outputs before going to SBC Sleep Mode

For details see **Chapter 2.1**.

1.1.2 Diagnosis Bits Setting after Transition to SBC Restart Mode

- **Occurrence:** wake from SBC Sleep or Fail-Safe Mode and transition to SBC Normal Mode (LH output was disabled before entering SBC Sleep Mode)
- **Behavior:** unexpected SPI diagnosis bit setting if device has been in SBC Sleep or Fail-Safe Mode for more than ~4 min No unexpected wake up will be triggered
- **Impact:** unexpected setting of certain SPI diagnosis bits
- **Workaround:** verification of other SPI diagnosis bits to detect actual device status

For details see **Chapter 2.2**.

1.2 Missing of Short Reset Delay Time after SBC Sleep or Fail-Safe Mode

- **Occurrence:** after wake-up from SBC Sleep or Fail-Safe Mode and depending on slope of $V_{cc1\_\mu C}$ ramp
- **Behavior:** under some conditions no reset delay time is present
- **Impact:** no t_{RD2} (if configured) but min. time of ~10 µs is ensured
- **Workaround:** configuration of long reset delay time t_{RD1}

For details see **Chapter 3**.

1.3 Application Hint: CAN & LIN Bus Interrupt Handling

The chapter describes the CAN and LIN Bus dominant time-out interrupt handling and SPI bit setting.

For details see **Chapter 4**.

2 Detailed Description for Unexpected Failure Detection

2.1 Possible Wake from SBC Sleep Mode

2.1.1 Occurrence

Only occurs when **L**imp **H**ome is active before entering SBC Sleep Mode

2.1.2 Occurrence Time

Approximately 4 min after entering SBC Sleep Mode

2.1.3 Behavior

- $V_{cc1\_\mu C}$ undervoltage (UV) comparator can generate the chip-internal signal “no Vcc1_UV” during SBC Sleep Mode
  after ~4 min
- Digital logic interprets $V_{cc1\_\mu C}$ is enabled and reset output RO is internally set to “HIGH” after reset delay time (only occurs when Limp Home is activated)
- RO driver is not supplied ($V_{cc1\_\mu C}$ is off in SBC Sleep Mode) → “Reset clamped low” (LH[2:0] = 110_B) detected

Note: This behavior will only occur in SBC Sleep Mode and not in SBC Fail-Safe Mode.

2.1.4 Impact

- SBC detects failure and changes to SBC Restart Mode and switches on $V_{cc1\_\mu C}$, leading to SBC Normal Mode
- LH[2:0] shows 110_B (“Reset clamped”) instead of 000_B
  MS[2:0] shows 001_B (coming from SBC Restart Mode) instead of 100_B (coming from SBC Sleep Mode)
  RM[1:0] shows 01_B (“Undervoltage on $V_{cc1\_\mu C}$”) instead of 00_B

2.1.5 How to Recognize the Behavior

- Unexpected device wake-up from SBC Sleep Mode after ~4 min without a wake source (CAN, LIN, WK) being set
- The same set of SPI responses could only be reached when a $V_{cc1\_\mu C}$ undervoltage occurs in SBC Normal or Stop Mode and a “reset clamped” appears during the following SBC Restart Mode

2.1.6 Recommended Workaround

- Do not activate LH before entering the SBC Sleep Mode (see also **Figure 1**)
- Ensure that LH is disabled before entering SBC Sleep Mode, e.g. after a failure:
  – Check if the LH bit (bit 12 in the SBC Configuration Register CS[2:0] = 100_B) is set
  – If the LH bit is set, then send a valid watchdog trigger. Otherwise the SBC can be sent to Sleep Mode immediately.
  – Disable the LH bit (*Note: this must be a separate SPI command*)

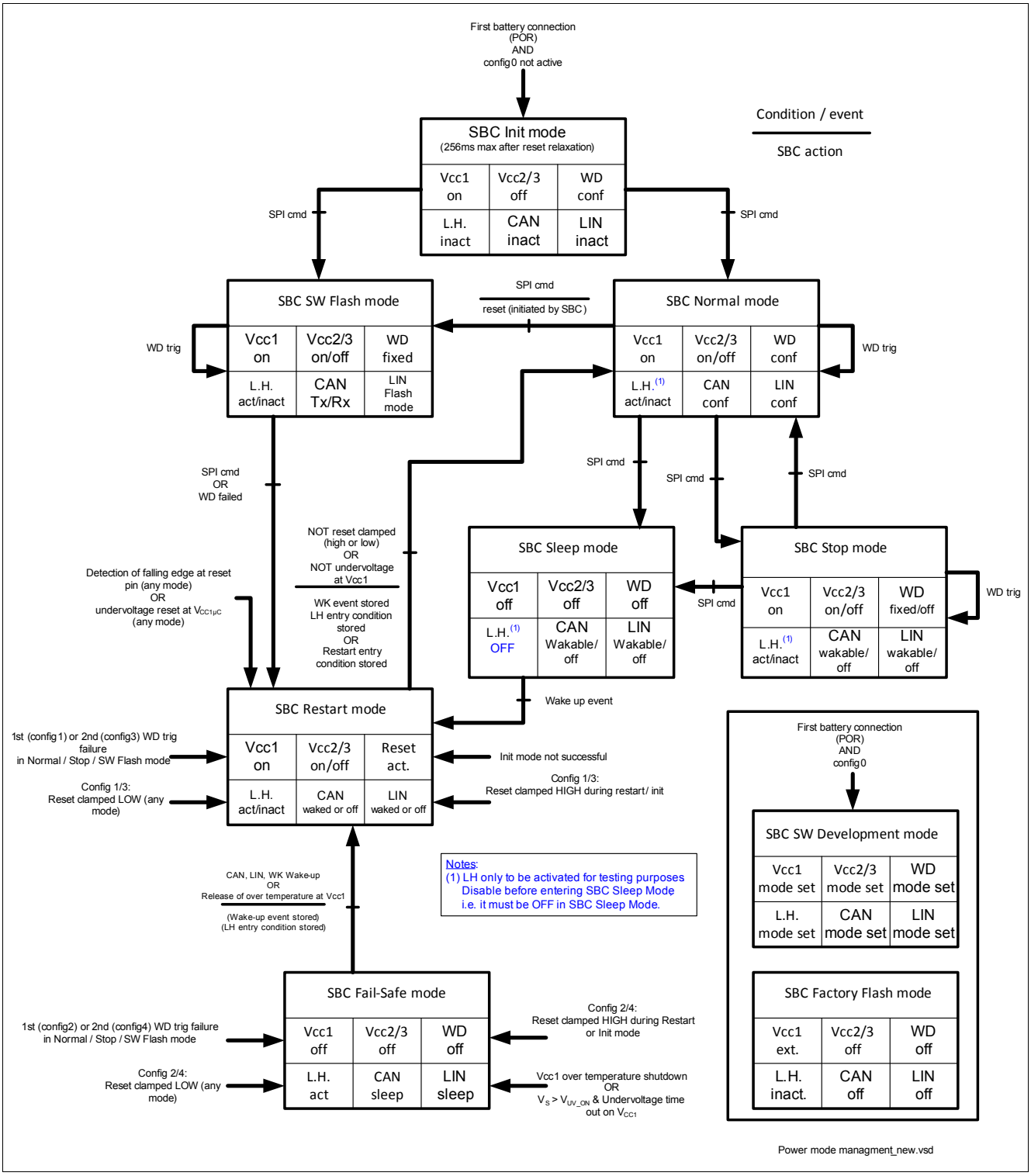

Figure 1 LH Activation during SBC Sleep Mode Not Permitted

Note: LH will be activated automatically due to a failure during the device operation and is not automatically disabled when entering SBC Normal Mode. Therefore, it must be ensured that LH is disabled before entering SBC Sleep Mode.

2.2 Diagnoses Bit Setting after Transition to SBC Restart Mode

2.2.1 Occurrence

After a wake up (via CAN, LIN, WK) when the device was in SBC Sleep or Fail-Safe Mode for more than ~4 min

2.2.2 Occurrence Time

Immediately after transition from SBC Sleep or Fail-Safe Mode to SBC Restart Mode leading to SBC Normal Mode. LH was not active before SBC Sleep or Fail-Safe Mode was entered.

2.2.3 Behavior

- $V_{cc1\_\mu C}$ undervoltage (UV) comparator generates the chip-internal signal “no Vcc1_UV” during SBC Sleep or Fail-Safe Mode (see also **Chapter 2.1**) but device will only wake up by an external wake-up event on CAN, LIN or WK as defined in the datasheet.
- At the SBC mode transition from SBC Sleep or Fail-Safe Mode to Restart Mode $V_{cc1\_\mu C}$ is enabled and $V_{cc1\_\mu C}$ UV comparator shows correct signal “Vcc1_UV”. This transition from “no Vcc1_UV” to “Vcc1_UV” causes an unexpected failure signaling and the SPI bits RM[1:0] set to 01_B .

2.2.4 Impact

Unexpected SPI diagnosis bit settings

- RM[1:0] set to 01_B (“Undervoltage on $V_{cc1\_\mu C}$”) instead of 00_B
- MS[2:0] shows 001_B (“Coming from Restart Mode”) instead of 100_B (“Coming from Sleep Mode”) or 110_B (“Coming from Fail-Safe Mode”) respectively

2.2.5 How to Recognize the Behavior

The same set of SPI responses can only be reached when $V_{cc1\_\mu C}$ undervoltage occurs in SBC Normal or SBC Stop Mode and the Wake register wasn’t cleared before.

See also **Figure 2** for a detailed detection tree

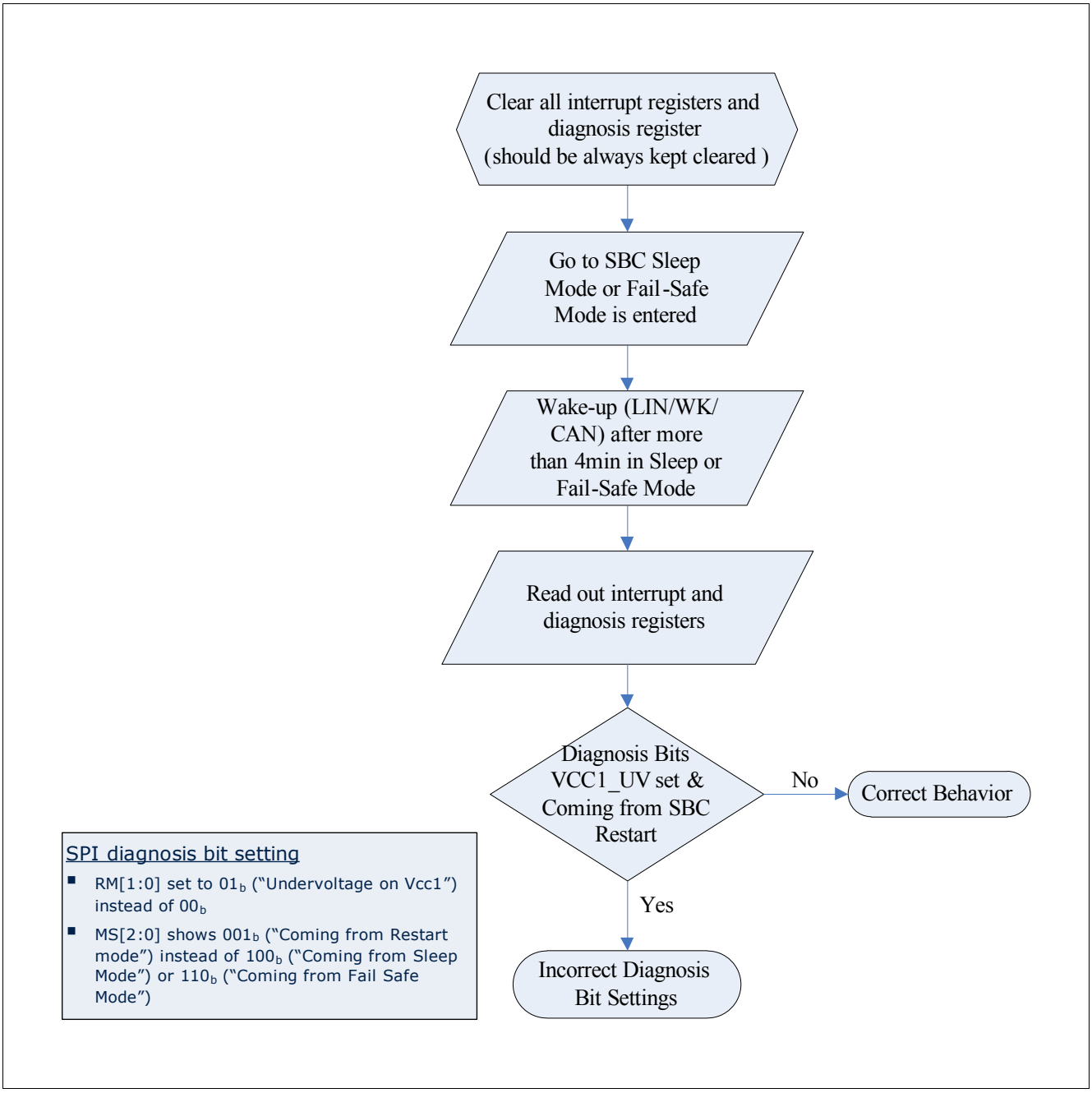

Figure 2 Verifying actual device status after coming from SBC Sleep or Fail-Safe Mode

2.3 Recommended Workaround

- Always clear interrupt and diagnosis (Limp Home) registers before entering SBC Sleep Mode
- Save last SBC State in microcontroller, e.g. SBC was sent to SBC Sleep Mode
- Read out interrupt and diagnosis (Limp Home) registers after wake-up (see **Figure 2**)

3 Detailed Description for Partially Missing Short Reset Delay Time after SBC Sleep or Fail-Safe Mode

3.1 Occurrence

- During the ramp-up phase of $V_{cc1\_\mu C}$ after a wake from SBC Sleep or Fail-Safe Mode at the transition from SBC Restart to SBC Normal Mode.
- The output voltage $V_{cc1\_\mu C}$ reaches the selected V_{RTx} during a certain time window t_{RDx} and t_{RDx} + 500 µs (because t_{RDx} is also used for the $V_{cc1\_\mu C\_UV\_TO}$ detection - see also **Figure 4**). The timer for t_{RDx} is initially started when SBC Restart Mode is entered.
- Depends on slope of $V_{cc1\_\mu C}$ during ramp-up, which is determined by external capacitor at $V_{cc1\_\mu C.}$

3.2 Behavior

- The expected behavior of the reset output RO is shown in **Figure 3**. When $V_{cc1\_\mu C}$ reaches the selected V_{RTx} threshold the selected reset delay time (t_{RDx}) is started. RO is released after t_{RDx}

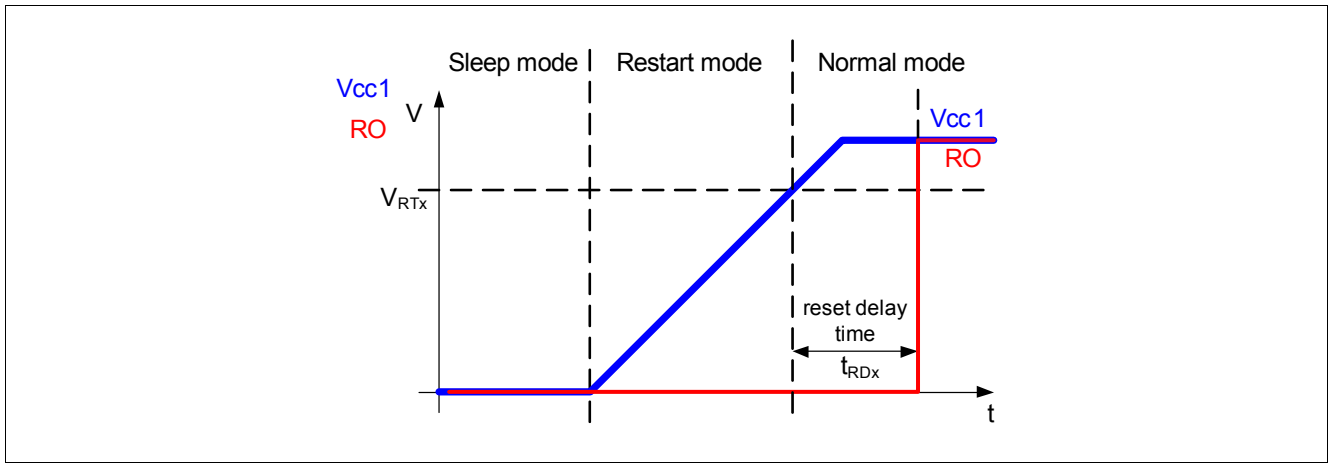

Figure 3 Expected behavior of RO output with reset delay time

- Under conditions as described in **Chapter 3.1** no reset delay time will be triggered. See also **Figure 4**
- When $V_{cc1\_\mu C}$ is ramping during SBC Restart Mode an internal counter starts running to test for the “Vcc1 undervoltage time-out” behavior. However, the same counter is used for the reset delay time t_{RDx}. See also **Chapter 3.3**

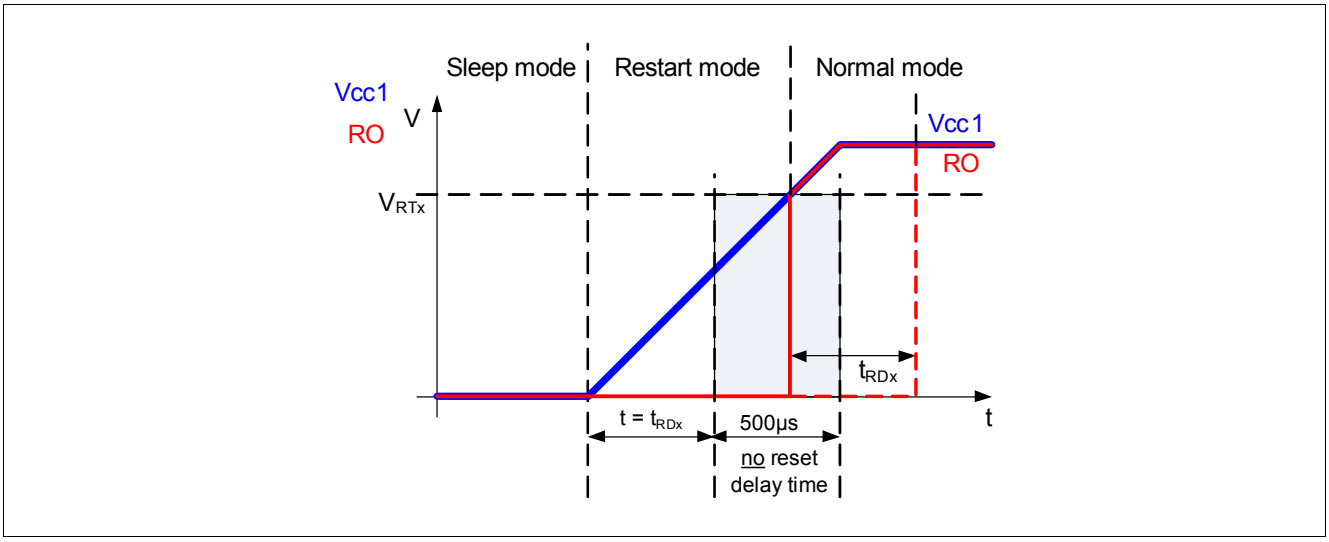

Figure 4 Missing reset delay time after coming from SBC Reset Mode

3.3 Impact

- When the counter content shows the end of the reset delay time when $V_{cc1\_\mu C}$ is crossing the V_{RTx} threshold, RO is set to “HIGH” already after 10µs (typ) instead of configured t_{RDx}

3.4 When does it occur?

- The critical range in time (see **Figure 4**) is the period between t_{RDx} and t_{RDx} + 500 µs
- When $V_{cc1\_\mu C}$ exceeds V_{RTx} during that time, the reset delay time is skipped and RO is release already after 10µs (typ.)
- The critical range for the external capacitor at $V_{cc1\_\mu C}$ and t_{RD2} selected can be calculated (assuming the capacitor is discharged):
  $I_{cc1,max} \times t_{RDx} / V_{RT} < \boldsymbol{C_{crit}} < I_{cc1,max} \times (t_{RDx} + 500\ \mu s) / V_{RT}$
  – Typ. example ($I_{cc1,max}$ = 300 mA, t_{RD2} = 500 µs, V_{RT} = 4.7 V):
  32 µF < C_{crit} < 64 µF
  – Worst case ($I_{cc1,max}$ = 200...500 mA, t_{RD2} = 450...550 µs, V_{RT} = 3.3...4.85 V):
  18.5 µF < C_{crit} < 167 µF

3.5 Recommended Workaround

- Select the long (default) reset delay time t_{RD1} (in that case C_{crit} > 185 µF). Changing the reset delay time does not affect any other behavior of the SBC.
- The selected reset threshold V_{RTx} has a small influence only

4 Application Hint: CAN & LIN Bus Interrupt Handling

The chapter describes the CAN and LIN Bus dominant time-out interrupt behavior, which should be considered in the user software.

The provided information should be a guideline to ensure a proper operation within the application (ECU).

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

4.1 Introduction

The TLE826xE/-2E devices trigger interrupts (pin INT pulled LOW) due to various events. The INT output is set LOW as soon as an interrupt condition occurs.

The INT pin is released after a SPI interrupt buffer read out that is performed with a Read Only command (111) to register (000) or latest after the time t_{INTTO} (typ. 6ms).

One of the interrupt sources are the CAN and LIN Bus dominant time-out detection. Bus pulses exceeding t_{BUS_TO} will trigger a time-out by switching the respective transceiver into Receive Only Mode. For this case it could be possible that under certain circumstances an interrupt is triggered without a SPI interrupt bit being set.

Definition of Ghost Interrupts

Ghost interrupts are defined as follows:

The INT pin is pulled LOW. However when the SPI status registers are read out, no SPI flags are set, i.e. all interrupt bits are read as “0”.
This behavior could occur if two interrupt routines are started in the microcontroller because of two consecutive interrupts triggered by the SBC and the first interrupt routine cleared already all interrupt bits.
The user software should consider this behavior in order to ensure reliable operation.

4.2 Ghost Interrupts caused by a CAN or LIN Bus Dominant Time-Out

A special kind of ghost interrupt could be caused by a bus dominant time-out event on the LIN or CAN bus.
The bus dominant time-out durations for CAN and LIN are specified as shown in **Table 1** and **Table 2** respectively.

Table 1 Dominant Time-Out Parameters for HS-CAN

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
TxD Permanent Dominant Time-out	t_{TxD_TO}	0.3	0.6	1.0	ms	CAN Normal Mode
Bus Dominant Time-out	t_{BUS_TO}	0.3	0.6	1.0	ms	CAN Normal Mode

Table 2 Dominant Time-Out Parameters for LIN

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
TxD Permanent Dominant Time-out	t_{TxD_TO}	6	12	20	ms	LIN Normal Mode
Bus Dominant Time-out	t_{BUS_TO}	6	12	20	ms	LIN Normal Mode

The expected behavior for both CAN or LIN bus dominant time-out would be:

- INT is pulled to LOW.
- The transceiver is switched from Normal Mode to Receive Only Mode.
- The bus failure bits are set to “01” in the SPI register.

Under certain circumstances, a different behavior can be observed:

- When recognizing a bus dominant time-out the INT pin is triggered correctly
- The transceiver mode is also changed to Receive Only Mode correctly.
- However, depending on the pulse width of the dominant bus pulse, the SPI failure bits are not always set, resulting in an unexpected behavior.

The respective transceiver always detects a bus dominant time-out correctly by triggering the INT pin and switching the transceiver into Receive Only mode.

The SPI bus failure bits are set accordingly if the detected time-out condition is valid for a sufficient time (>2 clock cycles ≡ 8µs). As shown in **Figure 5**, this is the case if the dominant time-out condition is valid longer than the maximum time-out detection period t_{BUS_TO}.

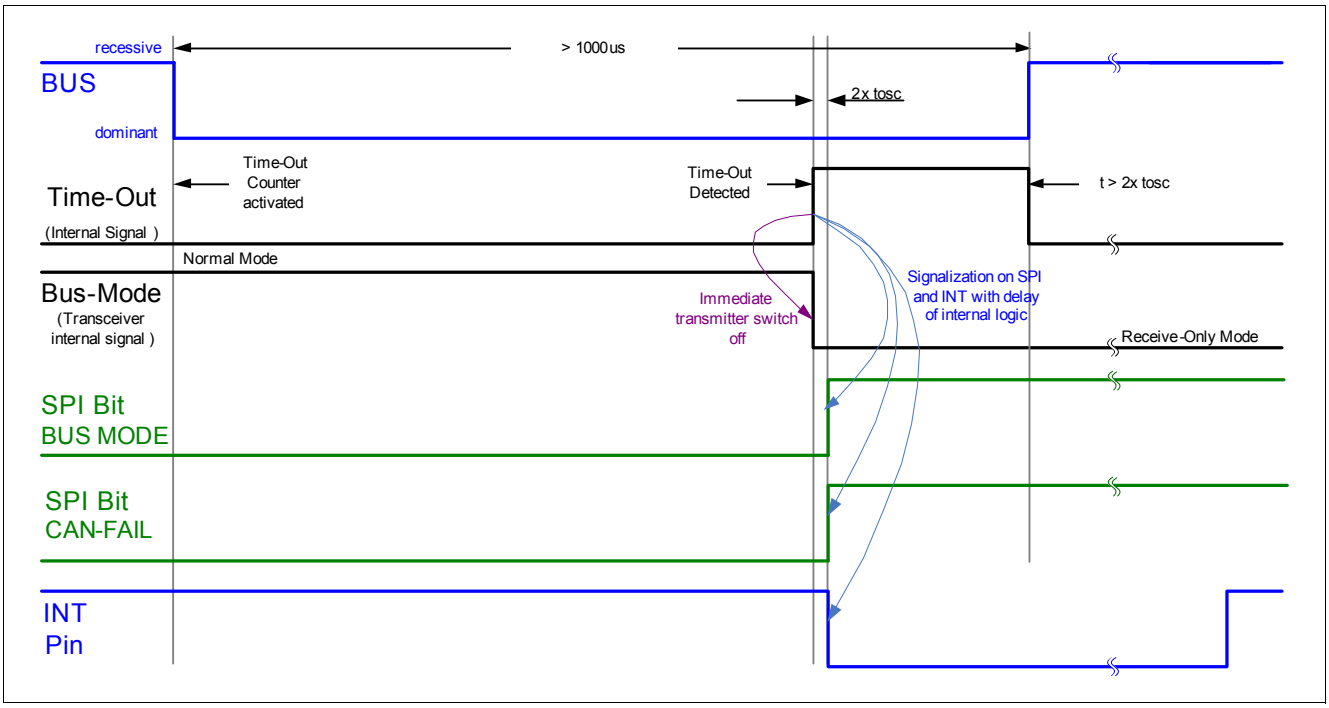

Figure 5 Simplified timing diagram (not to scale) of a dominant CAN bus signal longer than $t_{BUS\_TO, max}$ The SPI CAN Fail Bit is set

The mode change of the transceiver to Receive-Only Mode is done immediately once the time-out condition is detected. Signalization of the transceiver mode change and bus failure in the SPI register as well as setting the INT pin LOW is done at the same time after an internal delay. This applies for the CAN as well as for the LIN transceiver.

However, it could occur that a CAN or LIN dominant time-out failure[1)] is not always set in the respective SPI register for pulses shorter than the maximum time-out detection period t_{BUS_TO}.

If the time-out condition disappears shortly after the detection (1-2 clock cycles) it is possible that the SBC will capture the time-out event but not set the corresponding SPI flag. The INT pin is properly toggled, the transceiver is properly set into Receive Only Mode. However the SPI flag is not set. This behavior will occur for dominant CAN signals within the range of 300µs and 600µs (for LIN signals between 10ms and 14ms). A timing diagram showing this behavior is shown in **Figure 6**.

1) caused by transceiver failures as described in chapter 15.5.2.3 in theTLE8264 datasheet (TxD shorted to GND / bus dominant clamped, RxD shorted to $V_{cc1\_\mu C}$, TxD shorted to RxD)

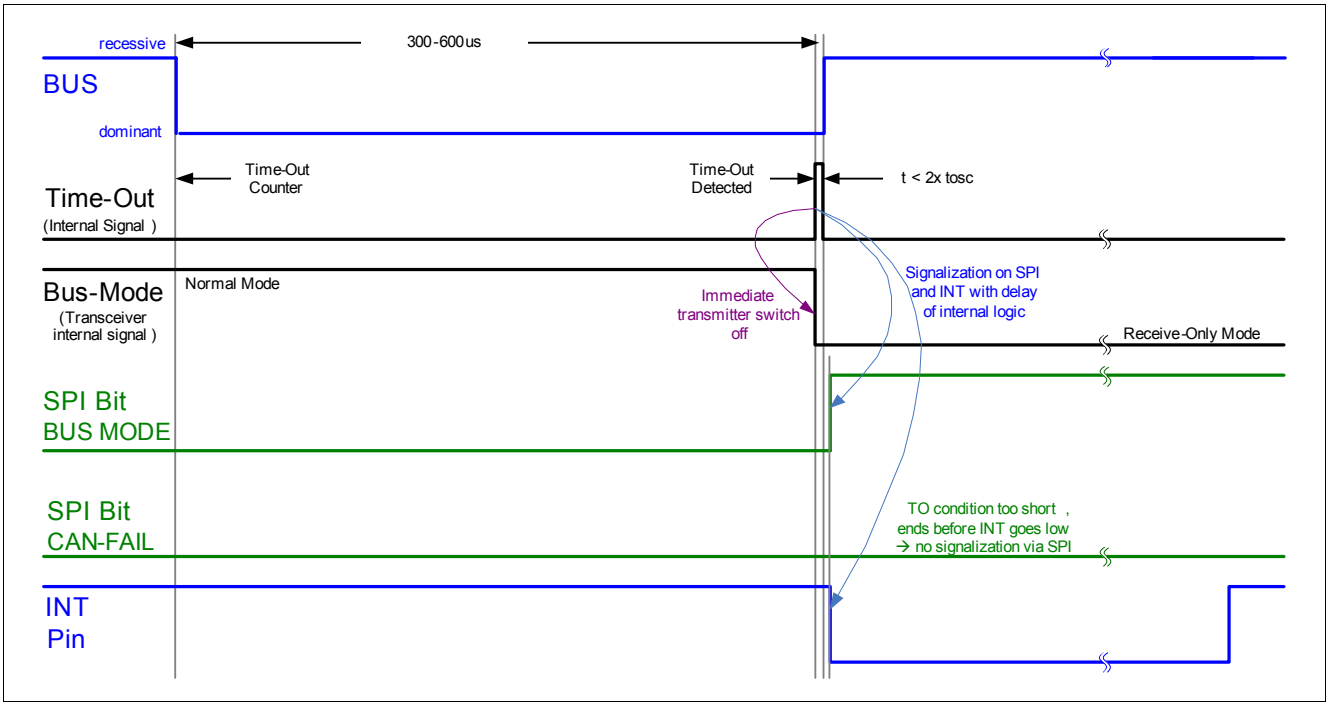

Figure 6 Simplified timing diagram (not to scale) of a dominant CAN bus signal in the range of 300 -600us. No SPI CAN fail bit is set

This behavior will also be seen when the transceiver is switched again to Normal Mode (from Receive Only Mode) during the dominant pulse and when the remaining dominant period falls within the above mentioned range.

4.3 Conclusion for LIN and CAN dominant time-out behavior

4.3.1 Summary

In case the bus failure period is smaller than the max. t_{BUS_TO}, it could occur that INT is pulled LOW but the bus failure bits are not set in the SPI. This is valid for LIN as well as CAN. Reliable detection of CAN / LIN dominant time-out is possible for dominant time outs ≥ max. t_{bus_TO}. This behavior applies for CAN and for LIN transceivers.

4.3.2 Proposal for handling interrupts when no SPI interrupt bit is set

The µC can not differentiate when no interrupt flag was set in the SPI registers. Therefore, the software must consider the above described behavior. Please consider the following proposals.When an interrupt is triggered and no SPI interrupt bit is set:

- Read the status of the communication setup register (101) to check if the transceivers have changed modes (i.e. from Normal to Receive Only Mode).
- If this is the case, then a bus failure has occurred and the microcontroller must switch the transceiver back to normal mode if applicable.
- If the mode of the transceivers is unchanged, then another ghost interrupt has occurred caused by a register read out while INT was HIGH (not a bus dominant time-out). If the interrupt registers are all ‘0’, then the INT trigger should be ignored by the software.

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