

Data Sheet

iMOTION™ Motion Controller Module for PM AC Fan

Quality Requirement Category: Industry

Features

- Complete 250V - 500V 3-phase inverter system in one chip
- Permanent Magnet Sinusoidal Motors Control by Hall sensors
- High efficiency control by quadratic phase advance curve
- Internal clock based on external RC
- 15V single power supply
3.3V Integrated Voltage Regulator
- Integrated protection features:
Dynamic overcurrent , Overtemperature ,
Overspeed, Rotor lock, Undervoltage lockout
- Full Three Phase Gate Driver
- Integrated Bootstrap Diodes
- No heatsink required
- 12x12 mm² PQFN package

Applications

- PM fan motor control

Description

IRDM982-025MB, IRDM982-035MB are the complete PM motor controller including six power MOSFET, high voltage integrated circuit, high precision analog circuit and integrated digital control algorithm. The controller implements a Hall sensor based control algorithm for 3-phase sinusoidal permanent magnet motor fan applications.

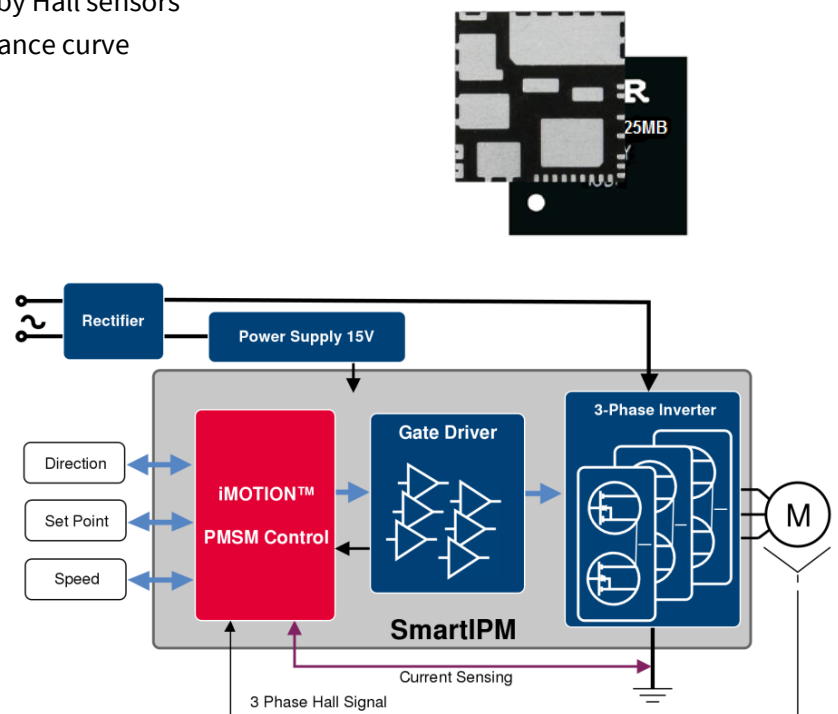
The integrated digital controller does not require any programming.

Instead there are 16 load curves stored in the internal ROM that can be selected via two resistor pairs.

The IRDM982 is packaged in the 12 x 12 PQFN package and designed to dissipate the power loss through a PCB without the use of an external heatsink.

There are two products available depending on the power rating of the internal high voltage MOSFETs:

- 1) IRDM982-025MB – employs six MOSFETs 500V 2A and 600V high voltage IC
- 2) IRDM982-035MB – employs six MOSFETs 500V 3A and 600V high voltage IC



**IRDM982 Series - IRDM982-025MB, IRDM982-035MB
Complete Motion Controller Module for PM AC fan**

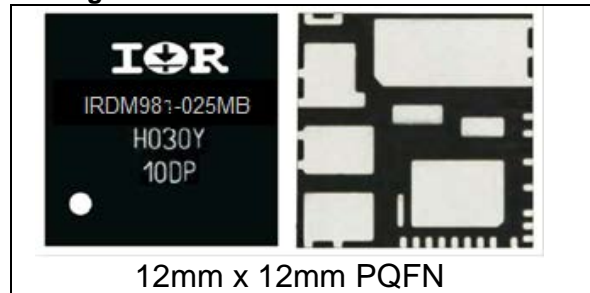
Features

- Complete 250V - 500V 3-phase inverter system in one chip
- No heatsink required
- Permanent Magnet Sinusoidal Motors Control by Hall sensors
- Selectable 4 or 12 pulse output per revolution¹⁾
- High efficiency control by quadratic phase advance curve
- Internal clock based on external RC
- 15V single power supply
- 3.3V Integrated Voltage Regulator
- Dynamic overcurrent limit per temperature
- Overtemperature control
- Overspeed protection
- Rotor lock detection/protection
- Full Three Phase Gate Driver
- Integrated Bootstrap Diodes
- Undervoltage lockout

Product Summary

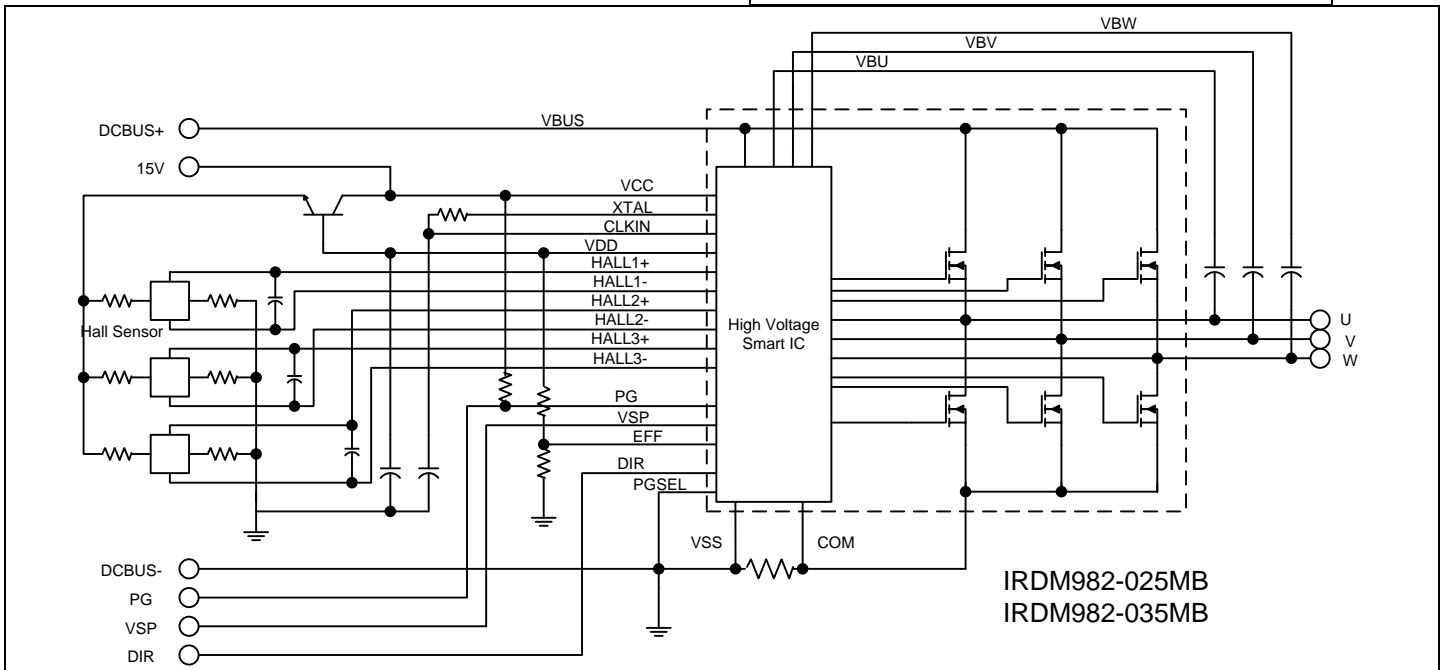
| | |
|---------------------|--|
| Topology | 3 Phase AC |
| V _{OFFSET} | ≤ 500 V for IRDM982-025MB, IRDM982-035MB |
| Control | Phase Advancement control |
| Feedback | DC Bus shunt, 3 Hall sensor |
| Temperature sensor | Integrated |

Package



Typical Applications

- Fan motor control



1) When used with 8 poles motor. In general it is 1 pulse / 3 pulses per electrical revolution.

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Introduction

IRDM982-025MB, IRDM982-035MB are the complete PM motor controller including six power MOSFET, high voltage integrated circuit, high precision analog circuit and digital control algorithm. There are three products depending on power rating of internal high voltage MOSFET listed below:

- 1) IRDM982-025MB – employs six MOSFET 500V 2A and 600V high voltage IC
- 2) IRDM982-035MB – employs six MOSFET 500V 3A and 600V high voltage IC

All two products are packaged in the 12 x 12 PQFN package and designed to dissipate the power loss through a mating PCB without an external heatsink. All two products contain exactly same control algorithm and analog functions. The controller implements a Hall sensor based control algorithm for 3-phase sinusoidal permanent magnet motor fan applications. The control also employs high efficiency PM motor control algorithm based on a quadratic load curve stored in internal ROM. 16 possible curves are selectable.

All devices have an on-chip voltage regulator to derive the 3.3V, required by the digital logic, from the 15V (VCC) supply. The 3.3VDC regulated voltage pin is available externally for connection to Hall-effect sensors. The IC provides low power standby (less than 7mW) mode of operation that 3.3V power is cut off when VSP (Voltage Input) becomes less than 1.15V to provide further power efficient operation.

An integrated A/D Converter is used to acquire EFF load curve selection, temperature (internal temp sensing), and the VSP input that sets the voltage applied to the motor. An internal temperature sensor is interfaced to the ADC and resulting digital conversion data is used to control the dynamic overcurrent setpoints as well as max overtemperature limit.

The protection functions include a supply under-voltage lockout (3.3V and 15VDC), over-speed protection, over-temperature limit and Over-current limitation protections. The reset circuitry includes a Power-On reset block and a reset input.

All devices do not require any programming. Default coefficients and system parameters are stored in internal ROM. The EFF input pin, used to adapt to specific motor and load to improve efficiency, can be used by means of two resistor pairs to choose one of 16 pre-stored load curves in ROM. DIR is a digital input pins which specify the motor direction command (CW or CCW).

All devices have an on-chip PLL to generate internal clocks. The PLL requires an external low frequency reference clock (32,768 Hz). The clock can be provided through an RC network connected to CLKIN and XTAL pins.

The IRDM982-025MB, IRDM982-035MB integrate high and low side gate drivers for applications up to 500V, it includes integrated Bootstrap FET that emulate bootstrap diode function and six power MOSFETs. The simplified block diagram is shown in Figure 1 in terms of hardware elements.

Simplified Block Diagram

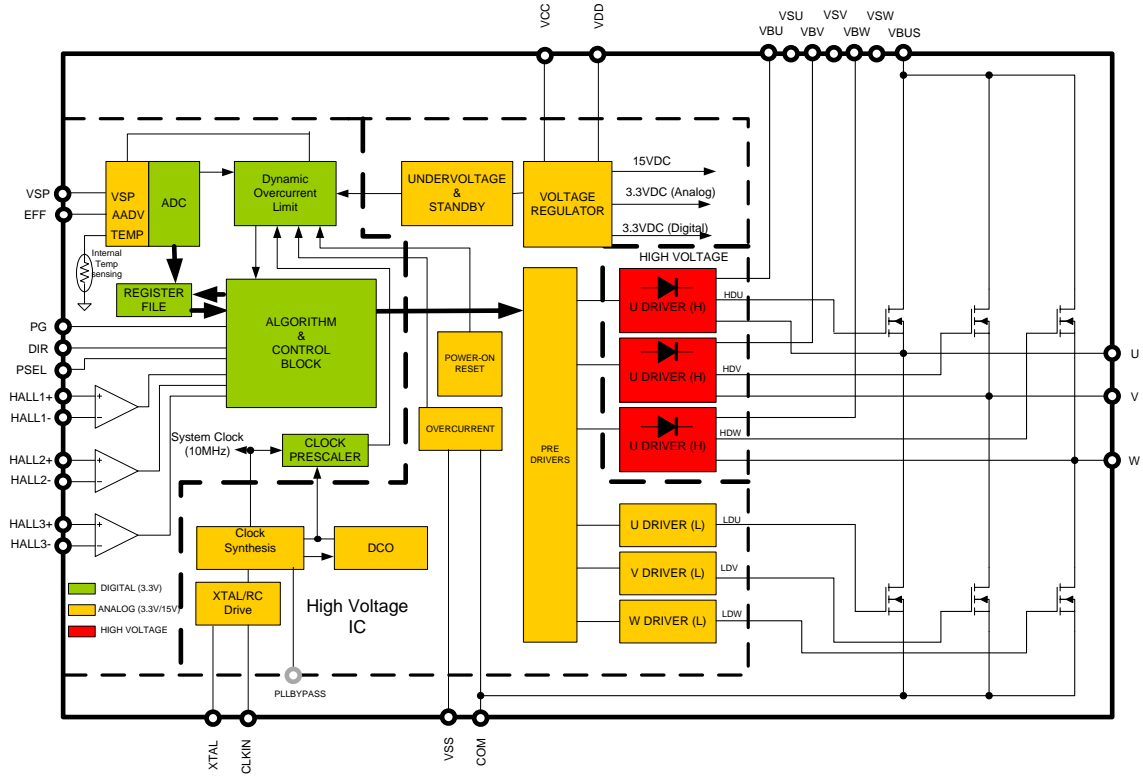


Figure 1 Simplified Block Diagram

Qualification Information

| | | |
|----------------------------|----------------------|---|
| Qualification Level | | Industrial ^{††} (per JEDEC JESD 47) Stress Test ; Preconditioning, Temp Cycle, Autoclave, THB, HTSL, LTSL, IOL, |
| Moisture Sensitivity Level | | PQFN MSL3 ^{†††} (per IPC/JEDEC J-STD-020) Floor Life Time ; 168 hours Conditions ; <30°C/60% RH Bake conditions ; 125 +5/-0°C, 24 hours minimum |
| ESD | Machine Model | Class B (per JEDEC Standard JESD22-A115) R1=0Ω, C1=200pF+/-10% Any part that passes after exposure to an ESD pulse of 200V, but fails after exposure to an ESD pulse of 400V. |
| | Human Body Model | Class 2 (per EIA/JEDEC standard EIA/JESD22-A114) R1=1500Ω+/-1%, C1=100pF+/-10% Any part that passes after exposure to an ESD pulse of 2000V, but fails after exposure to an ESD pulse of 4000V. |
| | Charged Device Model | Class IV (per JEDEC standard JESD22-C101 >1000V |
| IC Latch-Up Test | | Class I, Level A (per JESD78) Testing performed at room temperature ambient. The failure criteria as defined in table 1. |
| RoHS Compliant | | Yes |

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

| CLASS | TEST TYPE | TRIGGER POLARITY | CONDITION OF UNTESTED INPUTS | TEST TEMPERATURE ($\pm 2^\circ\text{C}$) | V_{supply} CONDITION | TRIGGER TEST CONDITIONS [6] | FAILURE CRITERIA | |
|-------|---------------------------------------|---------------------------|------------------------------|--|---|---|--|---|
| I | I-TEST | POSITIVE see FIGURE | Max. Logic High [1] | Room temperature | Maximum operating voltage for each V_{supply} pin group per device specification | +($I_{\text{nom}} + 100\text{ mA}$) or $1.5 \times I_{\text{nom}}$, whichever is greater [3] | 1.4 X I_{nom} or $I_{\text{nom}} + 10\text{ mA}$ whichever is greater [5] | |
| | | | Min. Logic Low [1] | | | | | |
| | | NEGATIVE see FIGURE | Max. Logic High [1] | | | | | -100 mA or $-0.5 \times I_{\text{nom}}$, whichever is greater in magnitude [4] |
| | | | Min. Logic Low [1] | | | | | |
| | V_{supply} OVER-VOLTAGE TEST | see FIGURE | Max. Logic High [1] | | | 1.5 X max V_{supply} [2] | | |
| | | | Min. Logic Low [1] | | | | | |
| II | I-TEST | POSITIVE see FIGURE | Max. Logic High [1] | Maximum ambient operating temperature | Maximum operating voltage for each V_{supply} pin group per device specification | +($I_{\text{nom}} + 100\text{ mA}$) or $1.5 \times I_{\text{nom}}$, whichever is greater [3] | 1.4 X I_{nom} or $I_{\text{nom}} + 10\text{ mA}$ whichever is greater [5] | |
| | | | Min. Logic Low [1] | | | | | |
| | | NEGATIVE see FIGURE | Max. Logic High [1] | | | | | -100 mA or $-0.5 \times I_{\text{nom}}$, whichever is greater in magnitude [4] |
| | | | Min. Logic Low [1] | | | | | |
| | V_{supply} OVER-VOLTAGE TEST | see FIGURE | Max. Logic High [1] | | | 1.5 X max V_{supply} [2] | | |
| | | | Min. Logic Low [1] | | | | | |

Table 1.

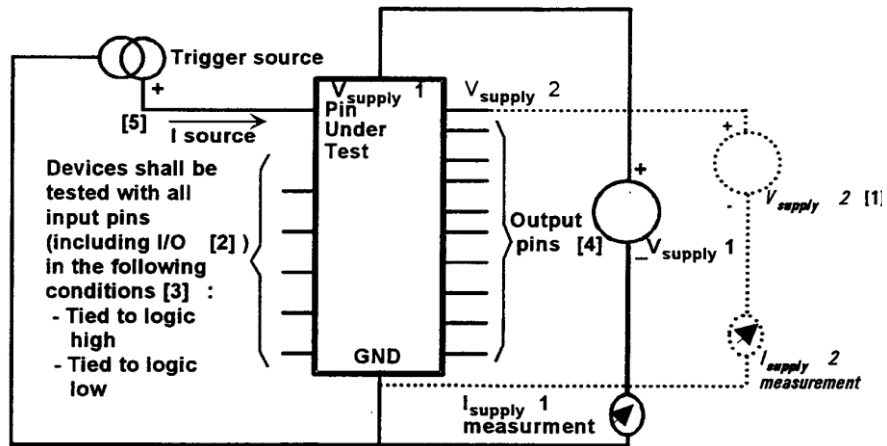


Figure 2.

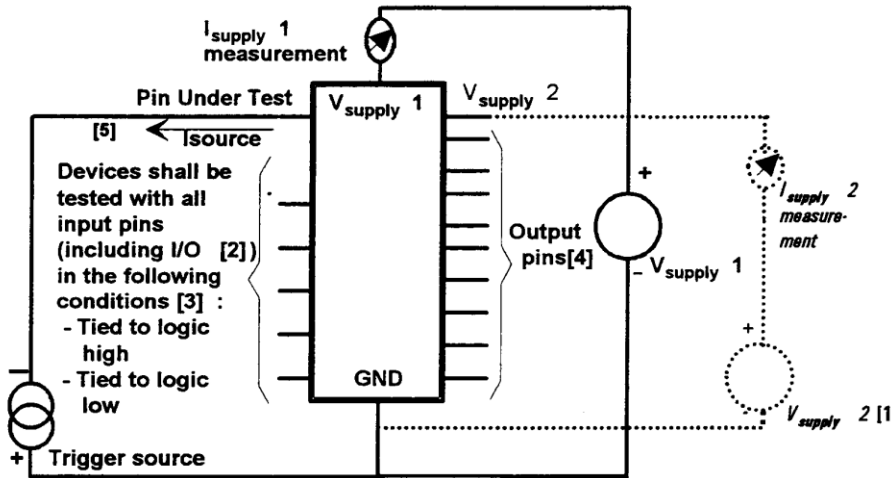


Figure 3.

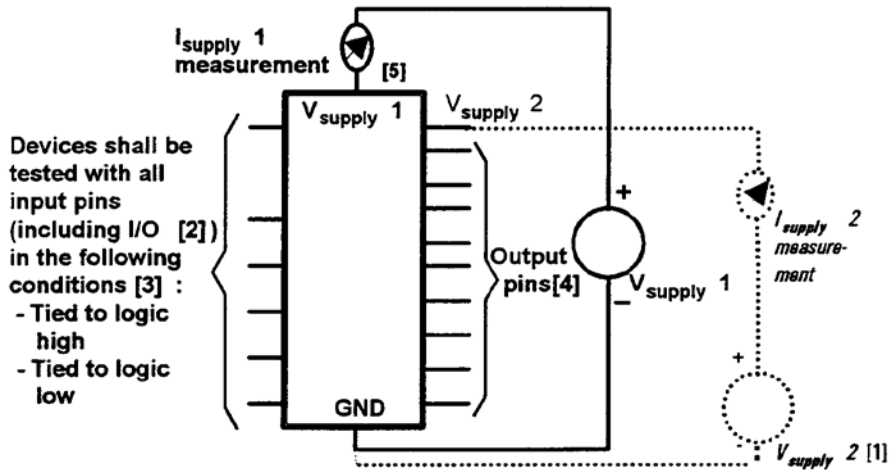


Figure 4.

IRDM982-025MB/-035MB Electrical Characteristics

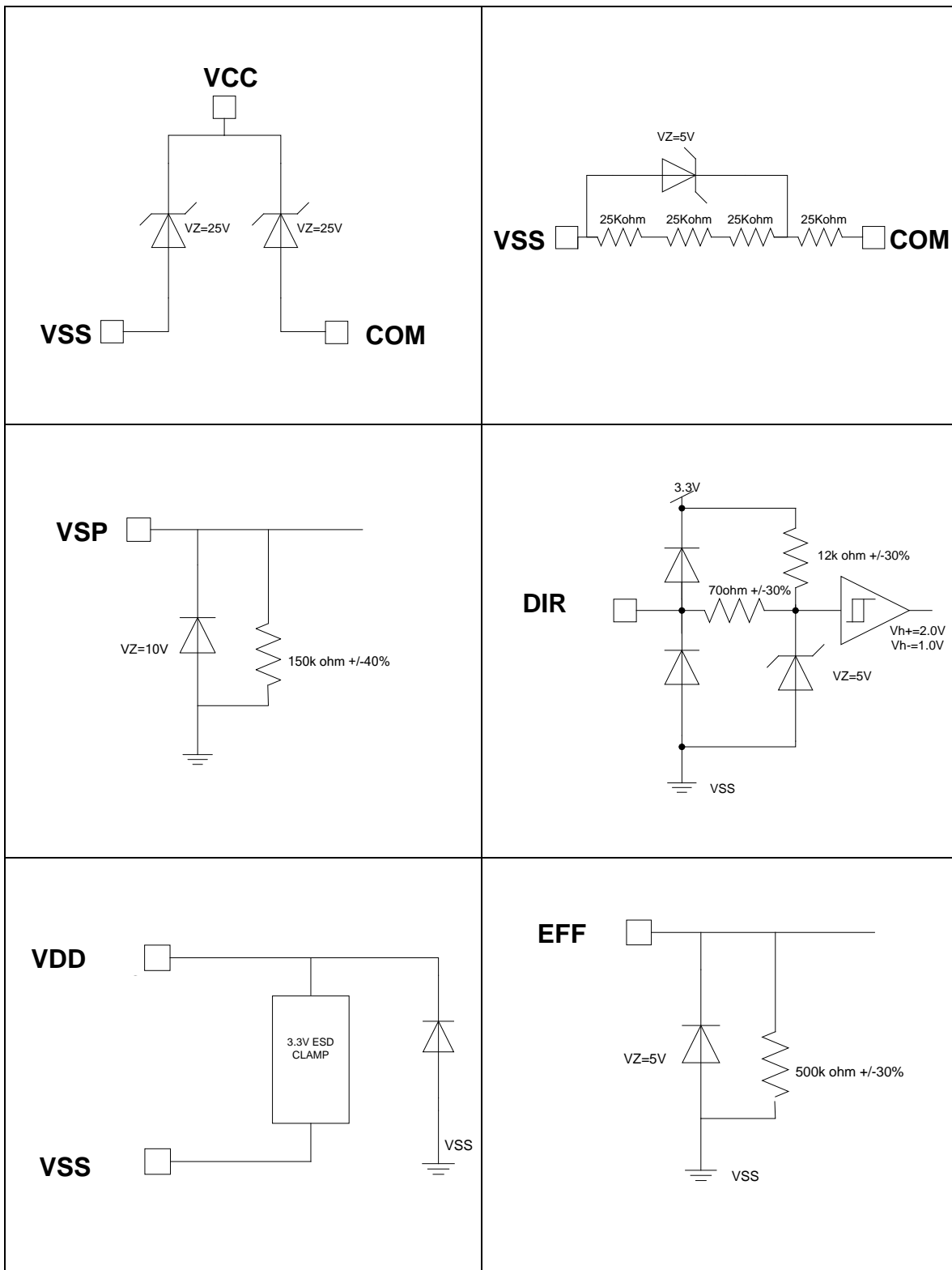
Absolute Maximum Ratings

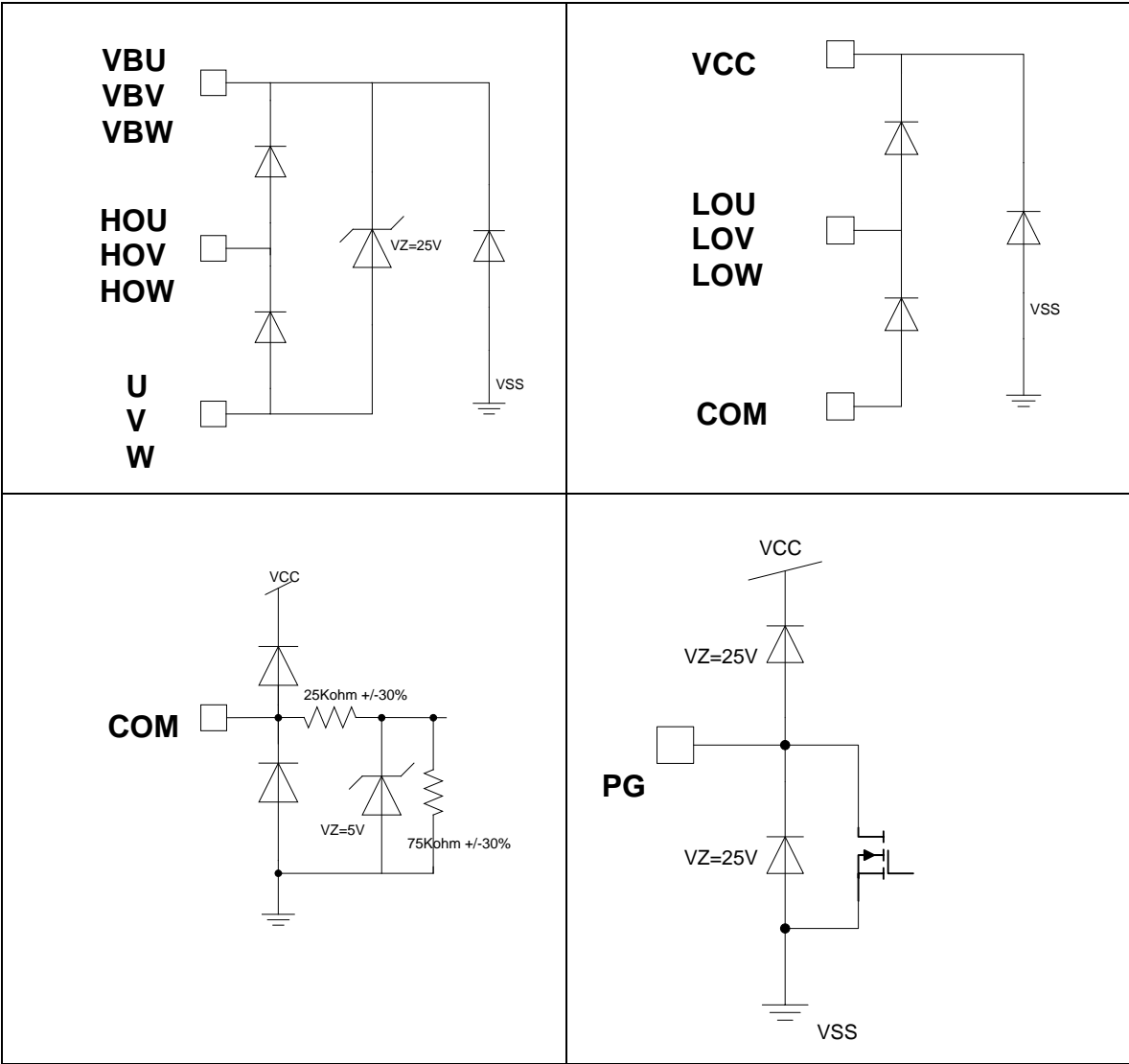
Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to **VSS** unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ta=25°C, unless otherwise stated.

| Symbol | Definition | Min. | Max. | Units | Condition |
|--|--|----------|-----------|-------|--|
| V _{ISO} | Isolation voltage | 1500 | - | Vrms | AC 1 minute |
| | | 1800 | - | | AC 1 second |
| DCBUS | DC bus voltage | - | 500 | V | IRDM982-025MB IRDM982-035MB |
| | | - | 630 | | IRDM982-025MB IRDM982-035MB 10usec ¹⁾ |
| DCBUS _{STAT} | DC bus voltage for PWM off ¹⁾ | - | 900 | V | IRDM982-025MB IRDM982-035MB VSP=0V, 1 minute, CO1=CO2 ²⁾ |
| VBU, VB _V , VBW | High-side floating absolute voltage | -0.3 | 525 | | |
| V _{SU} , V _{SV} , V _{SW} | High-side floating supply offset voltage | VB - 25 | VB + 0.3 | | |
| VCC | Low side power supply absolute voltage | -0.3 | 24 | | |
| | Drain current, IRDM982-035MB | - | 3.9 | A | Tc=25°C, Rth=2C/W |
| | Drain current, IRDM982-025MB | - | 2.6 | | Tc=25°C, Rth=3C/W |
| I _{VDD} | VDD current capability | - | 2 | mA | TW=1ms |
| I _{VSP} | VSP input current | - | 5 | | |
| COM | Power Ground | VCC - 24 | VCC + 0.3 | V | |
| V _{HCOM} | Hall Sensor input common mode voltage | -0.3 | VDD | | |
| V _{PG} | Open drain output motor evolution pulse | -0.3 | VCC+0.3 | | |
| V _{VSP} | Analog input voltage VSP | -0.3 | 10.0 | | |
| V _{DIR} V _{EFF} | Direction, Efficiency curve pins input voltage | -0.3 | VDD+0.3 | | |
| VDD | 3.3V voltage regulator output | -0.3 | 3.6 | | No short to ground |
| PD | Package power dissipation @ Tc ≤ +100 °C ¹⁾ | - | 5 | | W |
| TJ | Junction temperature ¹⁾ | - | 150 | °C | |
| TS | Storage temperature ¹⁾ | -55 | 150 | | |
| TL | Lead temperature (soldering, 10 seconds) ¹⁾ | - | 260 | | |

1) Guarantee by design, not tested at manufacturing

2) Output capacitance between VB-VS and VS-COM are same within +/-1%

ESD structure




Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to **VSS** unless otherwise stated in the table.

The input/output logic timing diagram is shown in Fig. 1.

The VS and VSS offset rating are tested with all supplies biased at a 15 V (VCC) differential / 3.3V (VDD).

Power up and down sequences are not dependent on the order of VCC, DCBUS, and VSP for proper operation to start or stop.

| Symbol | Definition | Min. | Typ | Max. | Units | Condition | |
|--------------------|---|--------------------|--------------|--------------------|-------|--|--------|
| V_U, V_V, V_W | PWM output motor voltage ¹⁾ | 100 | 320 | 450 | V | IRDM982-025MB IRDM982-035MB | |
| V_{PWMTR} | Transient PWM output motor voltage † ¹⁾ | -50 -50 | 0 0 | 500 250 | | 50ns transient period | |
| P_o | Output power ¹⁾ | - | 50 | - | W | Fc=20kHz, DCBUS=300V, IO=140mArms, no heatsink, Ta=40C, IRDM982-025MB | |
| | | - | 60 | - | | Fc=20kHz, DCBUS=300V, IO=200mArms, no heatsink, Ta=40C, IRDM982-035MB | |
| VCC | Low side supply voltage | 13.5 ¹⁾ | 15 | 16.5 ¹⁾ | V | | |
| V_{COM} | COM-VSS voltage | -5 | 0 | 5 | | | |
| V_{HCOM} | Hall sensor input voltage COMMON MODE | 0.6 | - | 2.9 | | | |
| V_{DIR}, V_{EFF} | Direction, Efficiency curve selection input pin voltage | 0 | - | VDD | | | |
| V_{PG} | Open drain output motor evolution pulse | 0 | - | VCC | | | |
| V_{VSP} | VSP input voltage | 0 | - | 9.8 | | | |
| VDD | 3.3V voltage regulator output | 3.0 | - | 3.6 | | Io=2mA | |
| VDDstby | 3.3V voltage regulator output when in stand by ¹⁾ | 0 | - | 0.8 | | VSP<1,15V for more than 5 s, Cout=20pF | |
| I_{VDD} | VDD current capability | - | - | 2 | | mA | TW=1ms |
| C_{VDD} | Capacitor at VDD | 2.2 | - | 22 | | uF | |
| FCRmax | Carrier frequency | 23.3k | 23.9k | 24.5k | Hz | $R_{CLKIN}=57.6K\Omega, C_{CLKIN}=270pF$ $F_{CLKIN}=38.99kHz$ | |
| FCRtyp | Carrier frequency | 18.1k | 18.5k | 18.9k | | $R_{CLKIN}=75K\Omega, C_{CLKIN}=270pF$ $F_{CLKIN}=30.31kHz$ | |
| FCRmin | Carrier frequency | 14.5k | 14.7k | 15.0k | | $R_{CLKIN}=95.3K\Omega, C_{CLKIN}=270pF$ $F_{CLKIN}=24.07kHz$ | |
| R_{CLKIN} | Resistor for RC oscillator ²⁾ | - | 75K 39.2K | - | Ω | R=75kohm with C=270pF, C _{PCB} =0pF Fc=18.83kHz R=75kohm with C=270pF, C _{PCB} =5pF Fc=18.50kHz R=39.2kohm with C=470pF, C _{PCB} =0pF Fc=20.75kHz R=39.2kohm with C=470pF, C _{PCB} =5pF Fc=20.54kHz | |
| C_{CLKIN} | Capacitor for RC oscillator ²⁾ | - | 270 470 | - | pF | | |
| TA | Ambient temperature ¹⁾ | -40 | | 125 | °C | | |

†Operational for transient negative VS of - 50 V with a 50 ns pulse width is guaranteed by design. Refer to the Application Information section of this datasheet for more details.

1) Guarantee by design, not tested at manufacturing

2) Carrier Frequency is calculated by the following.

$$FC=1/(((R+50) \times (C+5 \times 10^{-12}+C_{PCB})+900 \times 10^{-9}) \times 2.466)$$

C_{PCB} : Board layout capacitance

Static Electrical Characteristics

($V_{CC-COM} = (V_B - V_S) = 15\text{ V}$). $T_A = 25^\circ\text{C}$ unless otherwise specified. The VSP and IIN parameters are referenced to V_{SS} and are applicable to all six channels. The VO and IO parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to V_{SS} . The V_{BSUV} parameters are referenced to V_S .

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions | |
|------------------------|---|------|------|-------------------|-------|-----------------|-------------------------------------|
| IDSS | DC bus to COM leakage current, IRDM982-035MB | - | 70 | 200 | uA | | |
| | DC bus to COM leakage current, IRDM982-025MB | - | 50 | 100 | | | |
| VF | MOSFET body diode voltage, IRDM982-025MB | - | | 1.0 ²⁾ | V | IF=1A | |
| | MOSFET body diode voltage, IRDM982-035MB | - | | 1.0 ²⁾ | | | |
| VDD | VDD voltage | 3.0 | 3.3 | 3.6 | | | Io=2mA |
| VIH | Logic "1" input voltage | 2.5 | - | - | | | |
| VIL | Logic "0" input voltage | - | - | 0.8 | | | |
| VSPstbylow | Active to Standby mode VSP input negative going thresholds | 1.05 | 1.15 | 1.25 | | | |
| VSPstbyhigh | Standby to Active mode VSP input positive going thresholds | 1.3 | 1.4 | 1.5 | | | |
| VSPstbyhys | Standby mode VSP hysteresis | 0.1 | 0.25 | 0.4 | | | |
| VSPmin | VSP 0%duty | 1.9 | 2.1 | 2.3 | | | |
| VSPmax | VSP 100%duty | 5.2 | 5.4 | 5.6 | | | |
| VSP6step enter | VSP voltage that ensures enter in 6 step mode | 8.0 | 8.8 | 9.68 | | | 500 ms continuously above threshold |
| VSP6step exit | VSP voltage that ensures exit from 6 step mode | 8.0 | 8.8 | 9.68 | | | 200 ms continuously below threshold |
| V _{HCOM} | Hall sensor input voltage COMMON MODE | 0.6 | 2 | 2.9 | | | |
| V _{HDIF} | Hall sensor input voltage DIFFERENTIAL MODE | 0.03 | 0.5 | 2.5 | | | |
| V _{NOG} | Hall sensor input OP amp open loop gain ¹⁾ | 60 | - | 80 | | dB | Ta=-40 – 125C |
| V _{HOO} | Hall sensor input OP amp offset ¹⁾ | - | 1 | - | | mV | |
| V _{IHSTH} | Hall sensor input Schmitt Trigger input buffer hysteresis ¹⁾ | - | 1 | - | | V | |
| V _{HST+} | Hall sensor input Digital Schmitt Trigger input buffer positive going voltage ¹⁾ | - | 2 | - | | | |
| V _{HST-} | Hall sensor input Digital Schmitt Trigger input buffer negative going voltage ¹⁾ | - | 1 | - | | | |
| V _{CLKIN,TH+} | CLKIN positive going threshold | 2.5 | - | - | | | |
| V _{CLKIN,TH-} | CLKIN negative going threshold | - | - | 0.8 | | | |
| V _{CC,UVTH+} | V _{CC} supply undervoltage positive going Threshold | 8 | 8.9 | 9.8 | | | |
| V _{CC,UVTH-} | V _{CC} supply undervoltage negative going Threshold | 7.4 | 8.2 | 9 | | | |
| V _{CC,UVHYS} | V _{CC} supply undervoltage hysteresis | 0.3 | 0.7 | - | | | |
| V _{BS,UVTH+} | V _{BS} supply undervoltage positive going Threshold | 8 | 8.9 | 9.8 | V | | |
| V _{BS,UVTH-} | V _{BS} supply undervoltage negative going Threshold | 7.4 | 8.2 | 9 | | | |
| V _{BS,UVHYS} | V _{BS} supply undervoltage hysteresis | 0.3 | 0.7 | - | | | |
| V _{LIM1} | Current Limit Input voltage 1 ³⁾ | 450 | 520 | 590 | mV | Tc<116C | |
| V _{LIM2} | Current Limit Input voltage 2 ³⁾ | 300 | 375 | 450 | | Tc=116<132C | |
| V _{LIM3} | Current Limit Input voltage 3 ³⁾ | 200 | 250 | 300 | | Tc=132-<140C | |

| | | | | | | |
|-----------------------|---|------|------|------|--------|--------------------------------------|
| V _{ROCKILIM} | Current Limit input voltage at Rotor Lock | 200 | 250 | 300 | °C | |
| V _{ILIMHYS} | Current Limit Input voltage hysteresis | - | 60 | - | | |
| T _{OT+} | Positive going overtemperature limit | 130 | 140 | 150 | | |
| T _{OT-} | Negative going overtemperature limit | 95 | 105 | 115 | | |
| TAC | Temp sensor absolute accuracy | 0 | - | 12 | | |
| TES | Temp sensor resolution ¹⁾ | 0 | - | 3.25 | | |
| ICC | Vcc current | - | 13 | 24 | mA | |
| ICC _{STDBY} | Vcc current at standby | - | 0.10 | 0.20 | | |
| I _{VDD} | 3.3V output current | - | - | 2 | | |
| C _{VDD} | External capacitor for VDD ¹⁾ | 2.2 | - | 22 | uF | |
| PWM _{RES} | PWM pulse width resolution | - | 500 | - | Counts | 100ns resolution |
| MOD _{RESINT} | Internal modulator amplitude resolution ¹⁾ | - | 1686 | - | kHz | |
| F _c | PWM carrier frequency | 19.6 | 20 | 20.4 | | CLKIN=32.768kHz |
| FXTAL | XTAL pin frequency ¹⁾ | 29.6 | 30.3 | 30.9 | | R=75kohm, C=270pF |
| | | 32.2 | 32.8 | 33.5 | | R=40.2kohm, C=470pF |
| RBS | Ron internal bootstrap diode | - | 220 | - | Ω | |
| PD _{STBY} | Standby power dissipation | - | 1.5 | 3.0 | mW | VSP<1.15V, DCBUS=0V |
| I _{DRV+} | Internal driver gate drive sourcing current ¹⁾ | | 6 | | mA | V _{DRV} =0 V, PW ≤10 μs |
| I _{DRV-} | Internal driver gate drive sinking current ¹⁾ | - | 160 | - | | V _{DRV} =15 V, PW ≤10 μs |
| RON _{SPDFBK} | Ron of SPDFBK pin | - | 50 | 100 | Ω | |
| R _{thj-c} | Thermal resistance, junction to case ¹⁾ | - | 3 | - | °C /W | IRDM982-025MB |
| | | - | 2 | - | | IRDM982-035MB |

1) Guaranteed by design, not tested at manufacturing

2) Tested at wafer probe

3) V_{ILIM1,2,3} thresholds are tested at 25 degC. Temperature range is based on characterization only.

Dynamic Electrical Characteristics

$V_{CC} = V_B = 15\text{ V}$, $V_S = V_{SS} = \text{COM}$, $T_A = 25^\circ\text{C}$, and $C_L = 1000\text{ pF}$ unless otherwise specified.

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|-------------------|--|-------|-------|------|--|--|
| I_{CSC} | Short Circuit Drain Current ¹⁾ | - | 3 | - | A | IRDM982-025MB, $T_J=25^\circ\text{C}$, $t_{SC}<20\mu\text{s}$ $V^* = 320\text{V}$, $V_{CC}=15\text{V}$ |
| | | - | 5 | - | | IRDM982-035MB, $T_J=25^\circ\text{C}$, $t_{SC}<20\mu\text{s}$ $V^* = 320\text{V}$, $V_{CC}=15\text{V}$ |
| SCSOA | Short Circuit duration period ¹⁾ | 20000 | - | - | ns | $V^* = 300\text{V}$ (IRDM982-025MB,- 35MB), $V_{CC}=+15\text{V}$ to 0V , line to line short |
| t_{RR} | Reverse recovery time ¹⁾ | - | 80 | - | ns | $I_D=1\text{A}$, $di/dt=100\text{A}/\mu\text{s}$ |
| t_{ILIM} | ILIM to PWM current limit propagation delay | - | 3000 | - | ns | $C_{LOAD} = 1\text{nF}$, $F_{CLKIN} = 32.768\text{kHz}$ |
| $t_{ILIMFIL}$ | ILIM filter time ¹⁾ | 500 | 1000 | 1700 | ns | VILIM=2V, $T_a=25\text{C}$ |
| | | 400 | 800 | 1400 | | VILIM=2V, $T_a=125\text{C}$ |
| | | 600 | 1200 | 2000 | | VILIM=2V, $T_a=-40\text{C}$ |
| t_{HFILA} | Hall differential input analog filter ¹⁾ | - | 1500 | - | ms | $F_{CLKIN} = 32.768\text{kHz}$ |
| t_{HFILD} | Hall input digital filter delay ¹⁾ | - | 2500 | - | | $F_{CLKIN} = 32.768\text{kHz}$ |
| $t_{HALLSAT}$ | HALL input response time from saturation ¹⁾ | - | 5000 | - | | $F_{CLKIN} = 32.768\text{kHz}$ |
| t_{HALLPG} | HALL input to PG output propagation delay | - | 5000 | - | | $F_{CLKIN} = 32.768\text{kHz}$ |
| t_{VSPACT} | VSP standby to PWM active time | 14.0 | 17.5 | 22.0 | | CVDD=2.2uF, VSP=0→5.4V, $F_{CLKIN} = 32.768\text{kHz}$ |
| $T_{VSPONDELAY}$ | VSP active to PWM duty active | 2.0 | 3.5 | 5.0 | VSP from 1.8V to 2.6V, $F_{CLKIN} = 32.768\text{kHz}$ | |
| $t_{VDDHOLD}$ | VDD hold time at standby ¹⁾ | 4.9 | 5.0 | 5.1 | S | CVDD=2.2uF, VSP=2→0V, $F_{CLKIN} = 32.768\text{kHz}$ |
| $t_{RLOCKDETECT}$ | Rotor Lock detect time ¹⁾ | 4.9 | 5 | 5.1 | | VSP>2.1V, Elec freq <3Hz, $F_{CLKIN} = 32.768\text{kHz}$ |
| DT | Deadtime | - | 1000 | - | ns | $F_{CLKIN} = 32.768\text{kHz}$ |
| PW_{HIN} | Internal high side minimum pulse width | - | 400 | - | | Not a final output of a part , $F_{CLKIN} = 32.768\text{kHz}$ |
| PW_{LIN} | Internal low side minimum pulse width | - | 100 | - | | Not a final output of a part , $F_{CLKIN} = 32.768\text{kHz}$ |
| SPD_{OVER} | Over speed ¹⁾ | - | 200 | - | Hz | $F_{CLKIN} = 32.768\text{kHz}$ |
| SPD_{PWMCHG} | Block commutation to sine PWM change speed ¹⁾ | - | 3 | - | | 1 consecutive electrical angle update period, F_{CLKIN} =32.768kHz |
| SPD_{EFF1} | EFF bending point 1 speed ¹⁾ | - | 33.33 | - | | $F_{CLKIN} = 32.768\text{kHz}$ |
| SPD_{EFF2} | EFF bending point 2 speed ¹⁾ | - | 83.33 | - | | $F_{CLKIN} = 32.768\text{kHz}$ |

1) Guaranteed by design, not tested at manufacturing

Figures of Input Circuit and Table

The following Figure shows the interconnect bonding among the HVIC and MOSFETs within a package.

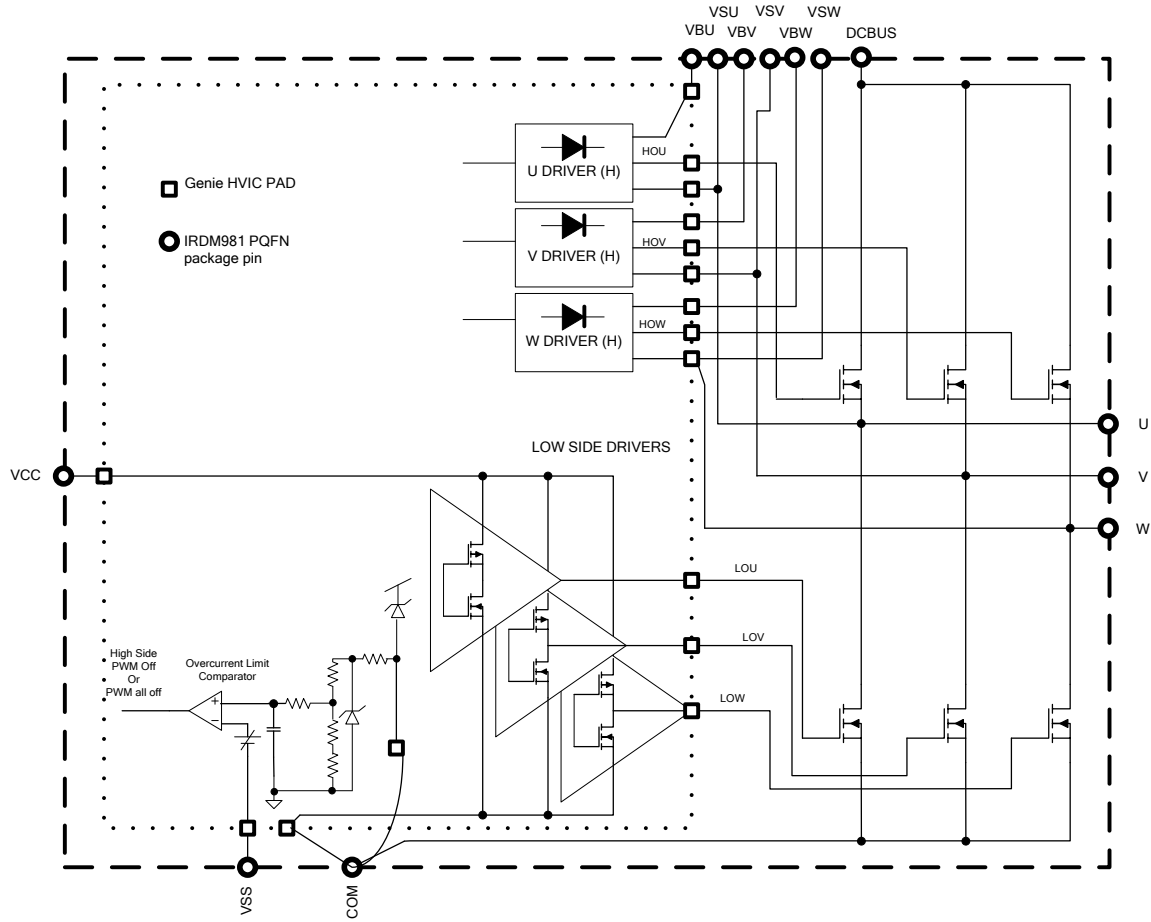


Figure 11 Connection diagram of VSS/COM and power pins/pads

The following Figures show the VSP input mapping, the Hall sensor input circuit, and the ISENSE pin input filter circuit.

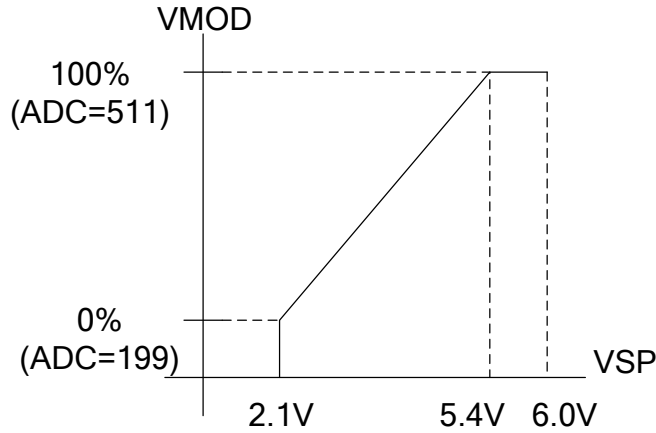


Figure 12 VSP Range and Thresholds

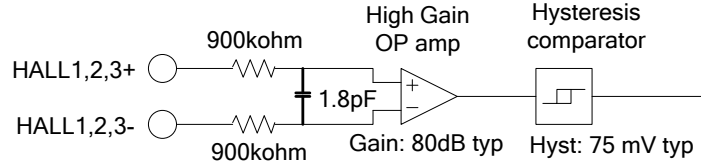


Figure 13 Hall sensor input circuit

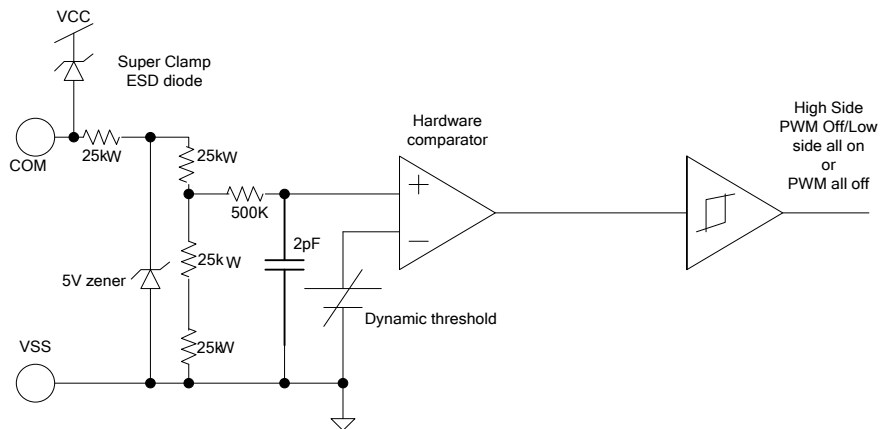


Figure 14 COM pin current limit comparator and analog filter

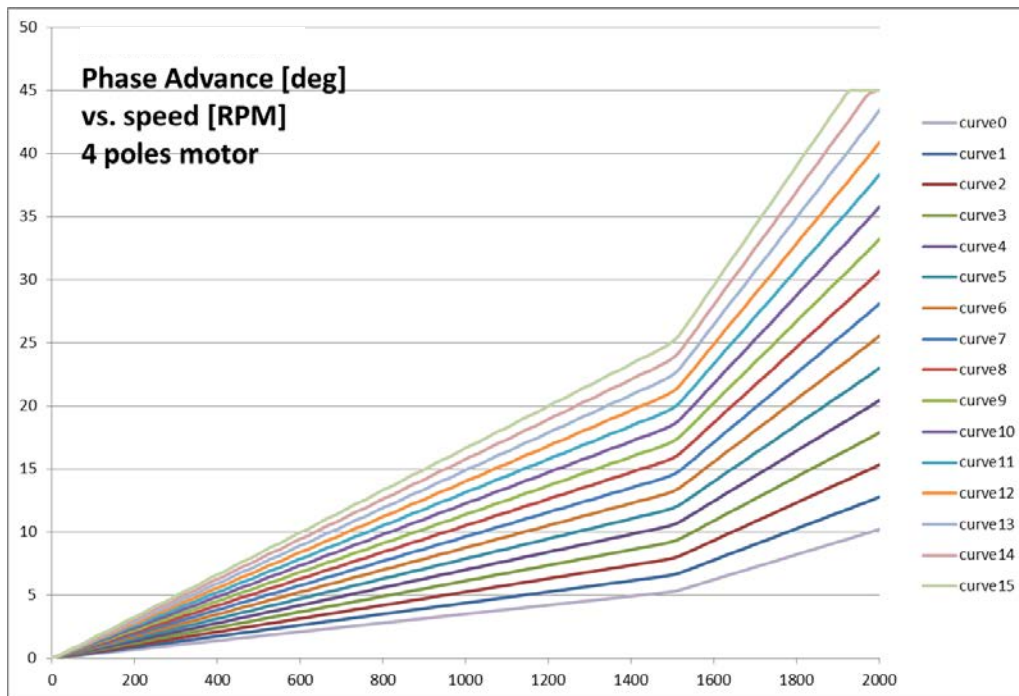
Load Curves

The following Table shows EFF pin mapping between input voltage and the advanced angle in degree per 50Hz of fundamental electrical frequency. Phase advance is by design clamped to be lower than 45 degrees at every frequency. At frequencies above 100 Hz the advancement is constant and it is kept to the same value at 100Hz.

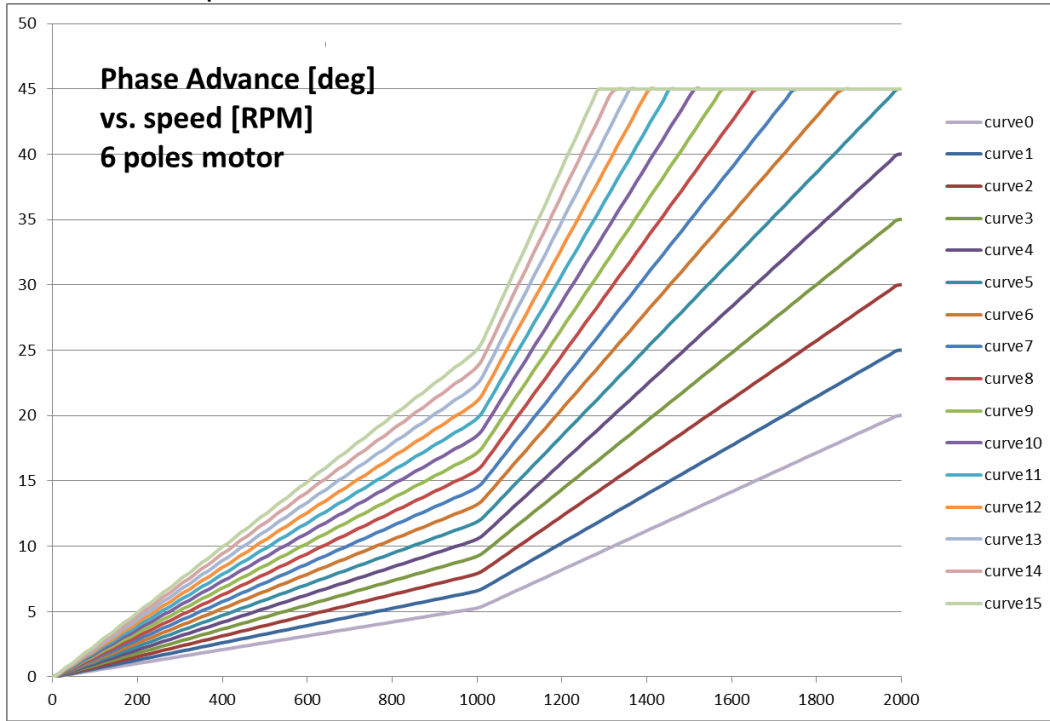
| Select | Degree/50Hz | Frequency [Hz] @ advance=45deg | EFF input | EFF digital input |
|-------------|-------------|--------------------------------|-----------------|-------------------|
| 15 | 25.49 | 64.22 | 3.094V – 3.300V | 152 |
| 14 | 24.15 | 65.75 | 2.888V – 3.087V | 144 |
| 13 | 22.81 | 68.04 | 2.681V – 2.881V | 136 |
| 12 | 21.47 | 70.34 | 2.475V – 2.675V | 128 |
| 11 | 20.12 | 72.63 | 2.269V – 2.469V | 120 |
| 10 | 18.78 | 75.69 | 2.063V – 2.262V | 112 |
| 9 | 17.44 | 78.75 | 1.856V – 2.056V | 104 |
| 8 | 16.10 | 81.80 | 1.650V – 1.850V | 96 |
| 7 | 14.76 | 87.16 | 1.444V – 1.644V | 88 |
| 6 | 13.42 | 92.51 | 1.238V – 1.437V | 80 |
| 5 | 12.07 | 99.39 | 1.031V – 1.231V | 72 |
| 4 | 10.73 | Advance=40deg above 100Hz | 0.825V – 1.025V | 64 |
| 3 | 9.39 | Advance=35deg above 100Hz | 0.619V – 0.819V | 56 |
| 2 | 8.05 | Advance=30deg above 100Hz | 0.413V – 0.612V | 48 |
| 1 | 6.71 | Advance=25deg above 100Hz | 0.206V – 0.406V | 40 |
| Default = 0 | 5.37 | Advance=20deg above 100Hz | 0.000V – 0.200V | 32 |

Table 2a EFF Parameters Selection

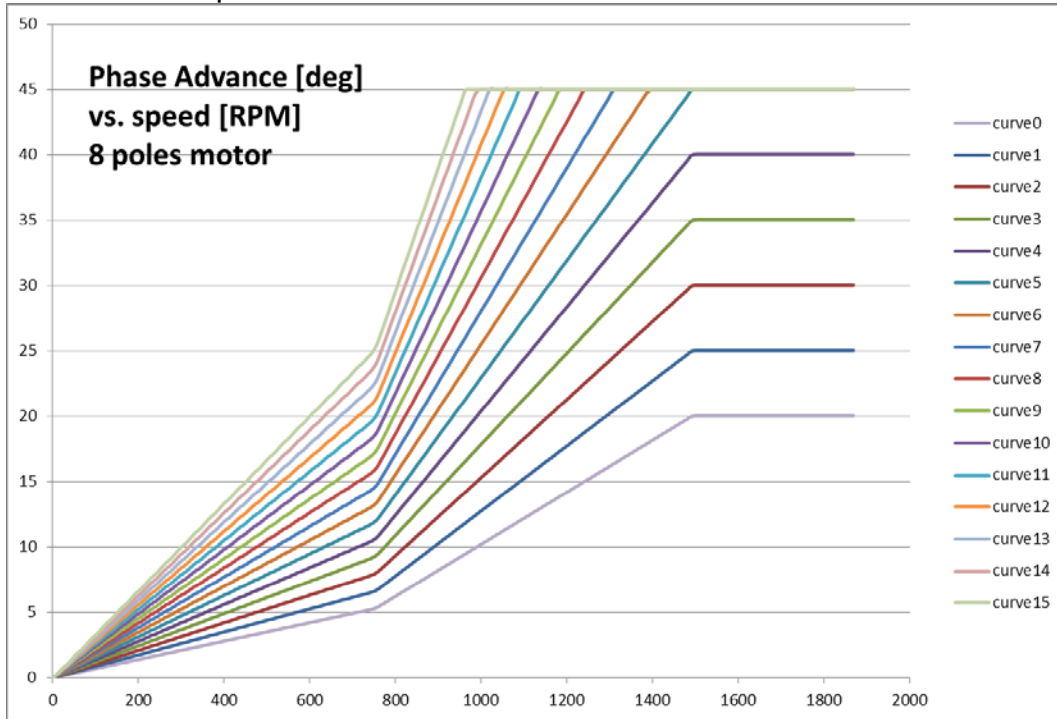
Load curves for 4 poles motor



Load curves for 6 poles motor



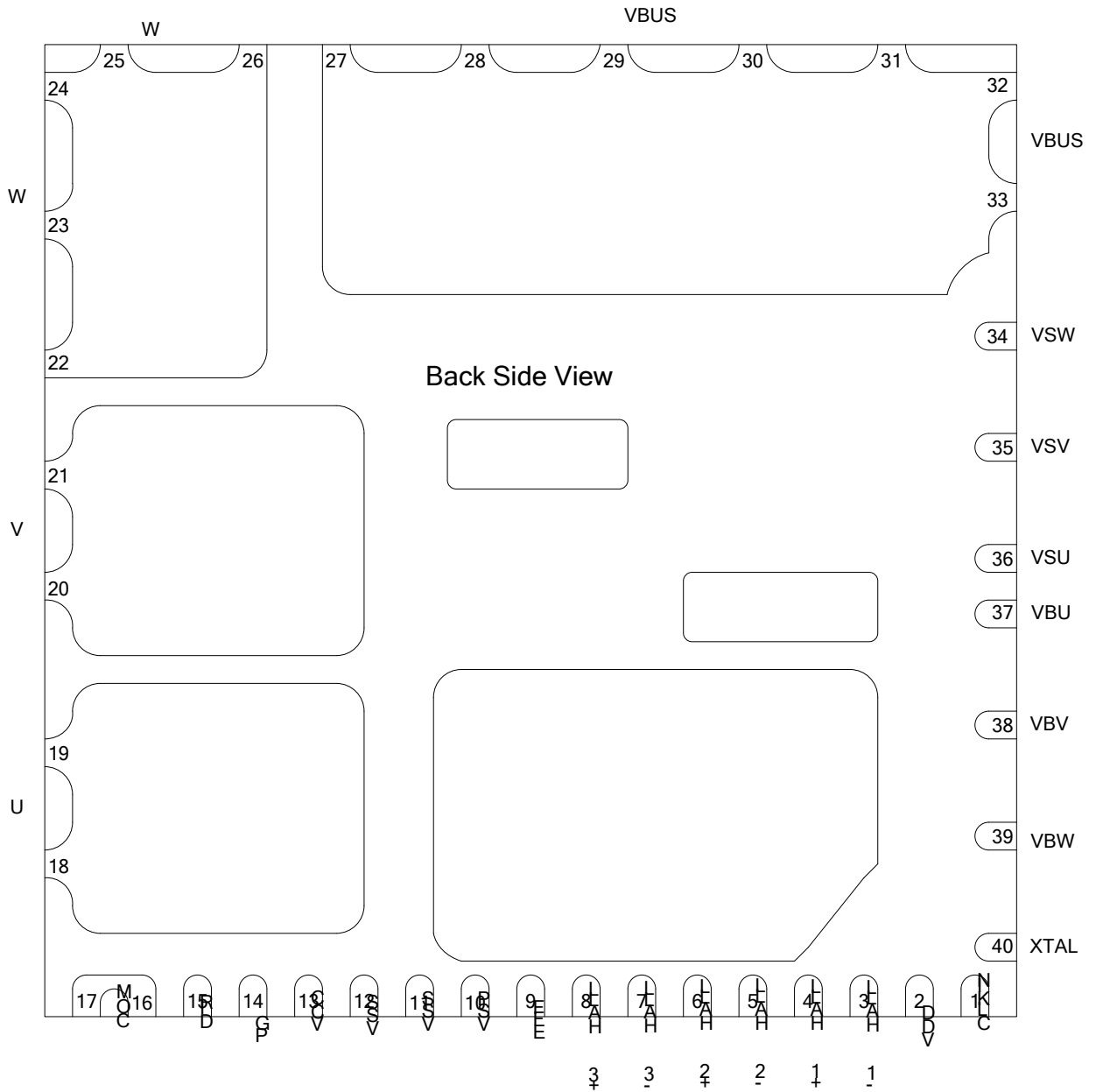
Load curves for 8 poles motor



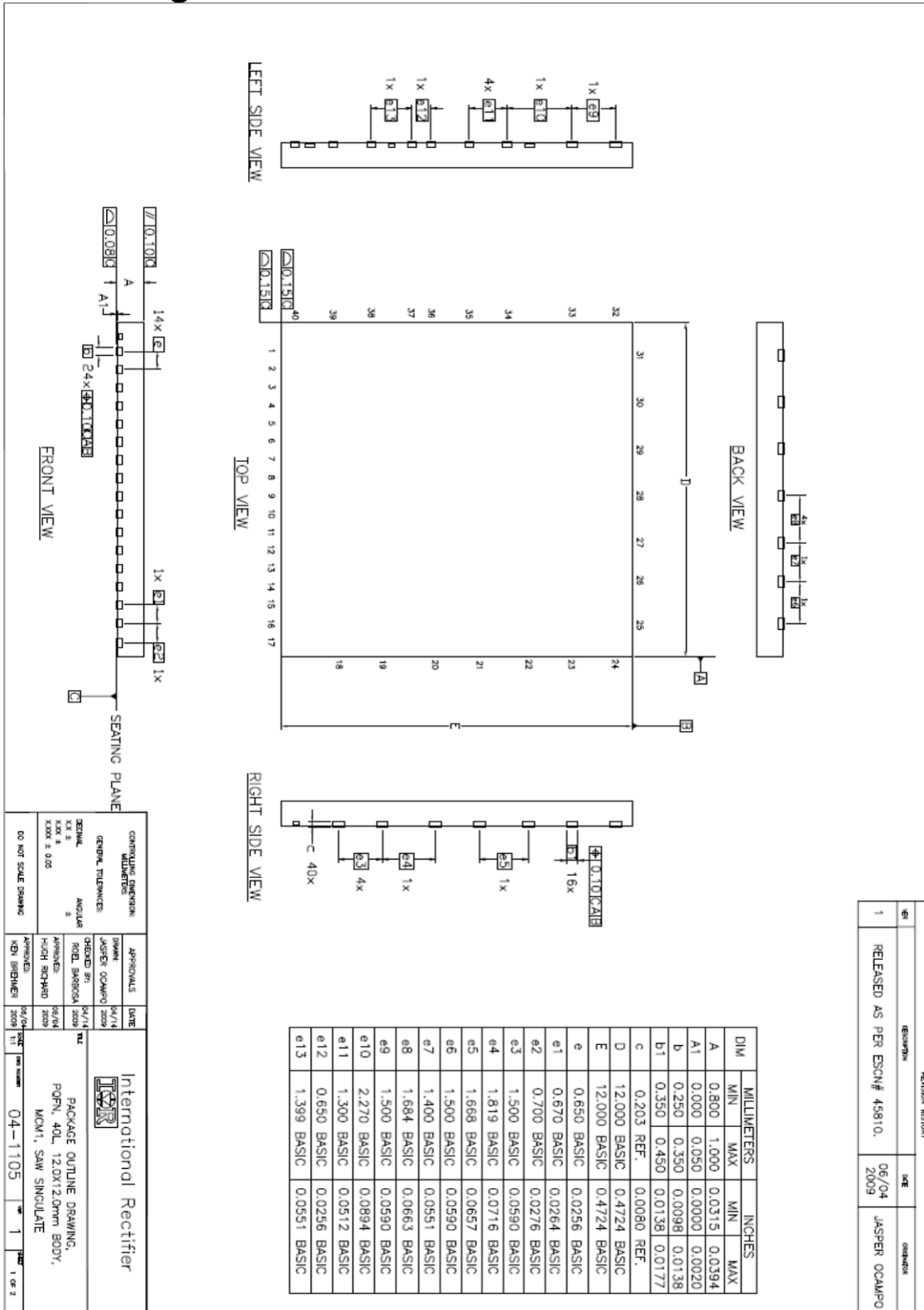
Lead Definitions

| Symbol | Pin # | Description |
|---------------|------------------------------|--|
| VSP | 10 | Voltage Set Point analog input. Provides the value of the PWM modulation index to the controller. |
| PG | 14 | Provides speed feedback to through pulses per revolution. It is an open drain output 15V tolerant. Output is a square wave of a 3 pulses per electrical cycle of fundamental frequency |
| DIR | 15 | Motor Direction Input (internally pulled up high = U→V→W) |
| EFF | 9 | Load curve selection parameter Input for efficiency improvement |
| XTAL | 40 | Clock buffer output |
| CLKIN | 1 | Clock buffer input |
| VSS | 11 | Logic ground |
| COM | 16,17 | Analog input ITRIP and Power Ground and Low side MOSFET source |
| VCC | 13 | 15V supply voltage |
| HALL1+ | 4 | Hall sensor 1 positive input |
| HALL1- | 3 | Hall sensor 1 negative input |
| HALL2+ | 6 | Hall sensor 2 positive input |
| HALL2- | 5 | Hall sensor 2 negative input |
| HALL3+ | 8 | Hall sensor 3 positive input |
| HALL3- | 7 | Hall sensor 3 negative input |
| VDD | 2 | 3.3V output |
| U | 18,19 | U phase output |
| V | 20,21 | V phase output |
| W | 22,23,24, 25,26 | W phase output |
| VBU | 37 | Phase U High side Bootstrap capacitor positive |
| VBV | 38 | Phase V High side Bootstrap capacitor positive |
| VBW | 39 | Phase W High side Bootstrap capacitor positive |
| VSU | 36 | Phase U High side Bootstrap capacitor negative |
| VSV | 35 | Phase V High side Bootstrap capacitor negative |
| VSW | 34 | Phase W High side Bootstrap capacitor negative |
| DCBUS | 27,28,29, 30,31,32, 33 | DC Bus voltage |

Lead Assignments



Package Outline

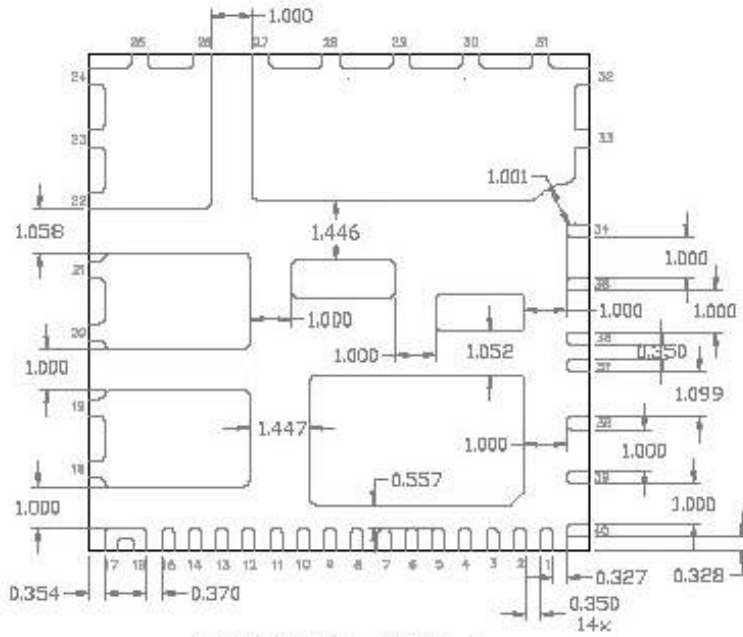
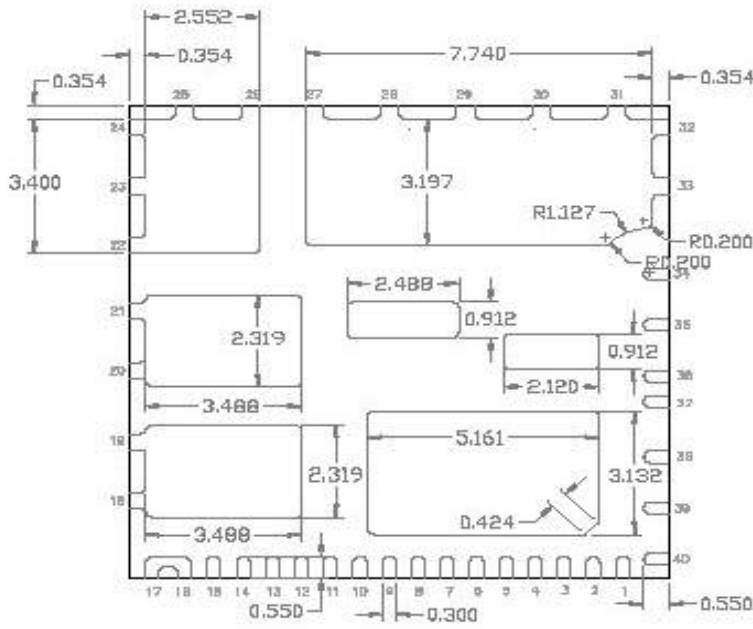


| REV | DESCRIPTION | DATE | BY |
|-----|------------------------------|------------|---------------|
| 1 | RELEASED AS PER ESCN# 43810. | 06/04/2009 | JASPER OCM/PO |

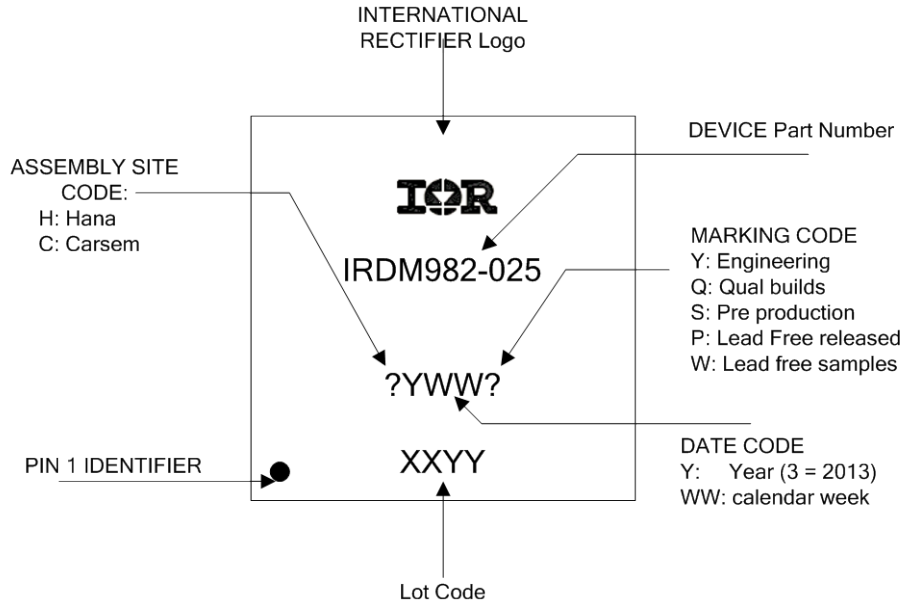
| CONTROLLING DIMENSIONS | | APPROVALS | | DATE | |
|------------------------|---------|---------------|---------------|------------|--|
| GENERAL DIMENSIONS | ANGULAR | DRAWN | CHECKED BY | DATE | |
| XXX ± | ± | JOSEPH OCM/PO | REEL SAMBROSA | 04/14/2009 | |
| XXX ± 0.05 | | HIGH RICHARD | | 04/09/2009 | |
| DO NOT SCALE DRAWING | | APPROVED: | KEN BRENNER | 04/11/2009 | |

International Rectifier

PACKAGE OUTLINE DRAWING,
POFN, 40L, 12.0X12.0mm BODY,
MCM1, SAW SINGULATE

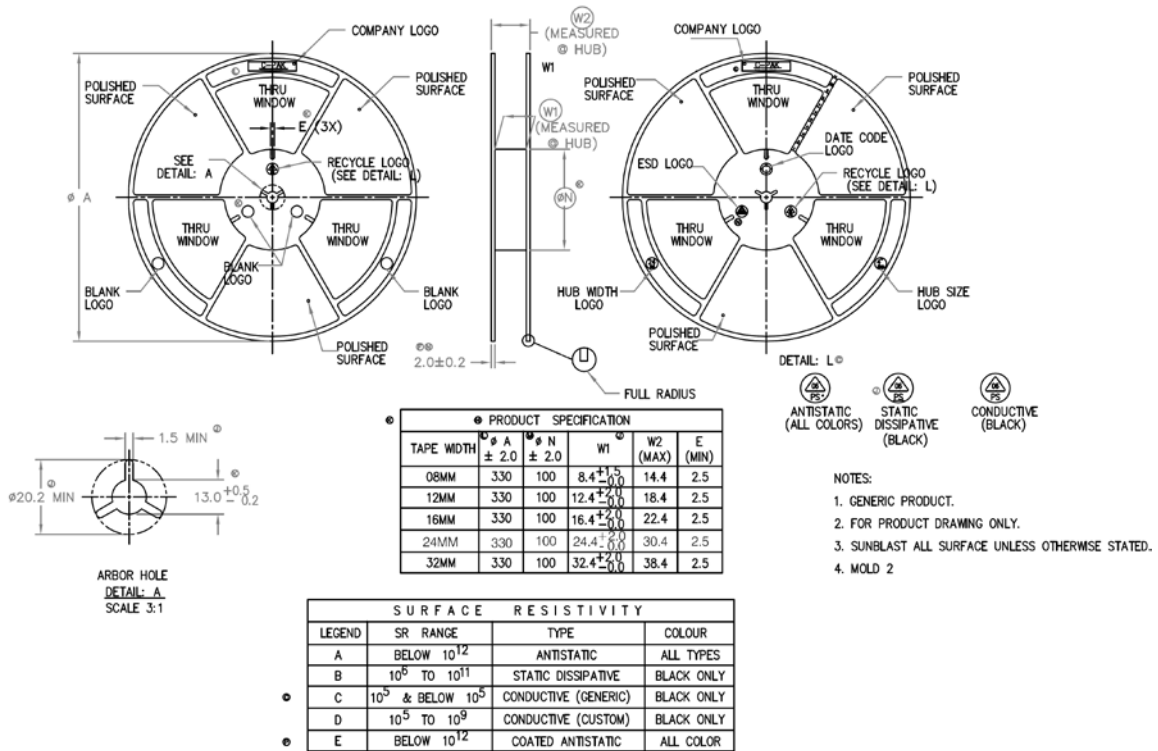
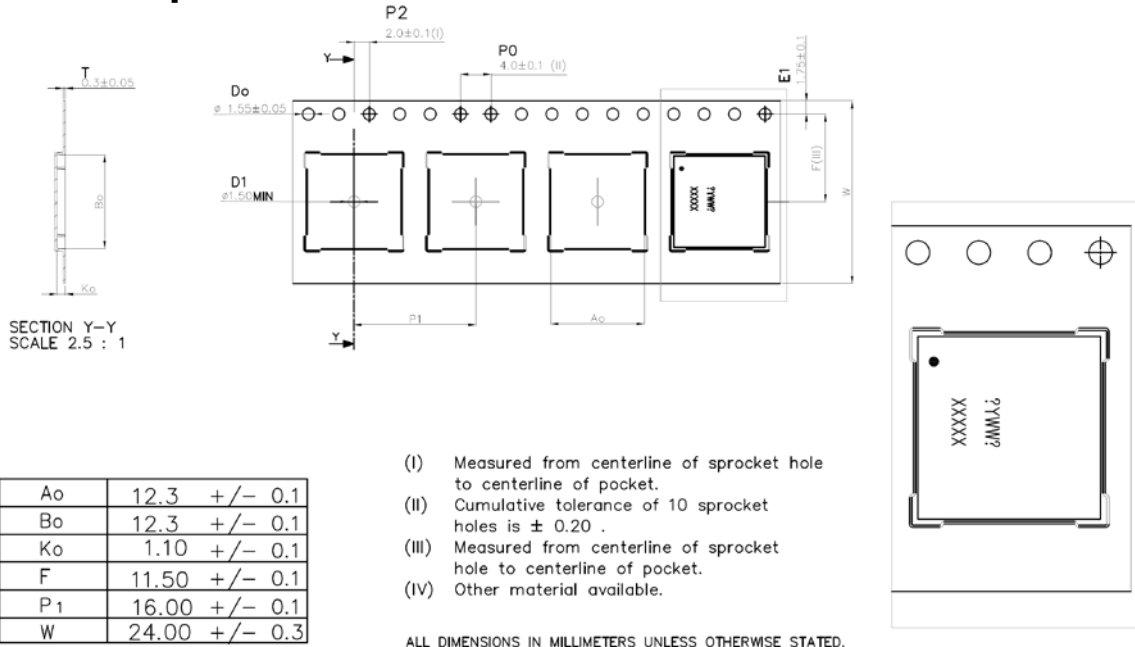
**BOTTOM VIEW- DETAIL 1****BOTTOM VIEW- DETAIL 2**Dimension in mm²

Package Marking



| Part number | Internal MOSFET |
|---------------|-----------------|
| IRDM982-025MB | 500V 2A |
| IRDM982-035MB | 500V 3A |

Tape and Reel Details



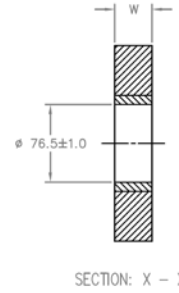
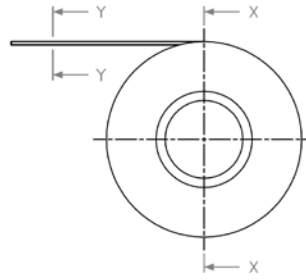
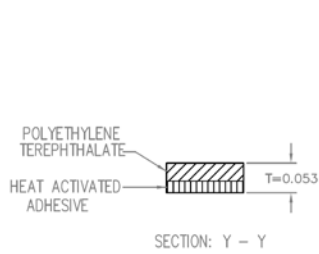


TABLE 2:

| STANDARD COVER TAPE WIDTH (W ± 0.1) | CARRIER TAPE WIDTH |
|-------------------------------------|--------------------|
| 5.3, 5.4 | 8 |
| 9.2, 9.3 | 12 |
| 13.3 | 16 |
| 21.0, 21.3 | 24 |
| 25.5 | 32 |
| 37.5 | 44 |
| 49.5 | 56 |

NOTES:

1. THICKNESS: 0.048–0.058 mm.
2. STANDARD LENGTH: 300 m
3. TENSILE STRENGTH: 7.7 kg/mm sq.
4. ELONGATION: 120%
5. SURFACE RESISTIVITY: 10^{11} ohms/SQ. MAX (STATIC DISSIPATIVE)
6. PEEL STRENGTH CONFORMS TO EIA SPEC. $55 \pm 25g$
7. LUMINOUS TRANSMITTANCE: 91%
8. HAZE: 50%
9. OTHER COVER TAPE WIDTH REFER TO W14.08–04

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

Soldering temperature profile

The following soldering temperature profile is recommended. Any temperature which may exceed those indicated below is not recommended and may cause a permanent damage to the physical component such as deformation.

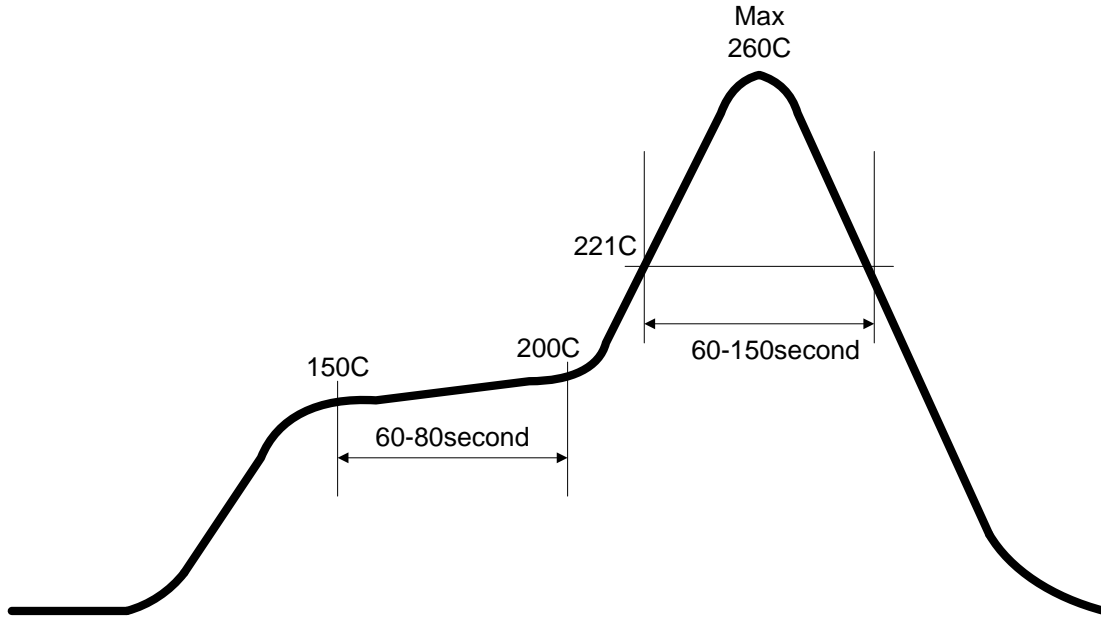


Figure 13 Recommended soldering temperature profile

| Condition | Value | Remark |
|------------------------------|-----------|--------|
| Temperature rise rate | 3°C | |
| Temperature fall rate | 6°C | |
| Number of reflow | 2 | |
| Manual soldering temperature | 260°C | |
| Manual soldering time | 10 second | |

Table 3 Recommended soldering reflow condition

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