XC9223/XC9224 Series

ETR0509_015

1A Driver Transistor Built-In Step-Down DC/DC Converters

☆GreenOperation-Compatible

■GENERAL DESCRIPTION

The XC9223/XC9224 series are synchronous step-down DC/DC converters with a 0.21Ω (TYP.) P-channel driver transistor and a synchronous 0.23Ω (TYP.) N-channel switching transistor built-in. A highly efficient and stable current can be supplied up to 1.0A by reducing ON resistance of the built-in transistor. With a high switching frequency of 1.0MHz or 2.0MHz, a small inductor is selectable; therefore, the XC9223/XC9224 series are ideally suited to applications with height limitation such as HDD or space-saving applications. Current limit value can be chosen either 1.2A (MIN.) when the LIM pin is high level, or 0.6A (MIN.) when the LIM pin is low level for using the power supply which current limit value differs such as USB or AC adapter. With the MODE/SYNC pin, the XC9223/XC9224 series provide mode selection of the fixed PWM control or automatically switching current limit PFM/PWM control. As for preventing unwanted switching noise, the XC9223/XC9224 series can be synchronized with an external clock signal within the range of ± 25% toward an internal clock signal via the MODE/SYNC pin. For protection against heat damage of the ICs, the XC9223/XC9224 series build in three protection functions: integral latch protection, thermal shutdown, and short-circuit protection. With the built-in UVLO (Under Voltage Lock Out) function, the internal P-channel driver transistor is forced OFF when input voltage becomes 1.8V or lower. The XC9223B/XC9224B series' detector function monitors the discretional voltage by external resistors.

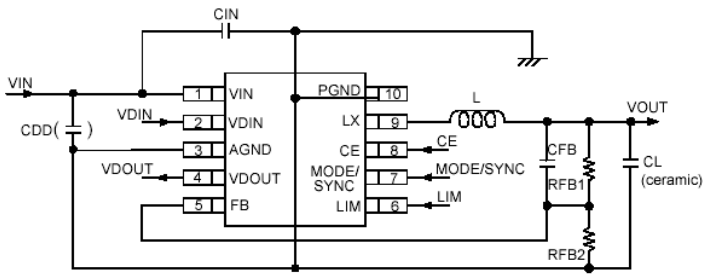
■APPLICATIONS

- ●Magnetic disk drive
- ●Note PCs / Tablet PCs
- ●CD-R / RW, DVD
- ●Mobile devices / terminals
- ●Digital still cameras / Camcorders
- ●Multi-function power supplies

■FEATURES

Input Voltage Range	: 2.5V ~ 6.0V
Output Voltage Range	: 0.9V ~ VIN (set by FB pin)
Oscillation Frequency	: 1MHz, 2MHz (±15% accuracy)
Output Current	: 1.0A
Maximum Current Limit	: 0.6A (MIN.) ~ 0.9A (MAX) with LIM pin='L' : 1.2A (MIN.) ~ 2.0A (MAX.) with LIM pin='H'
Controls	: PWM/PFM or PWM by MODE pin
Protection Circuits	: Thermal shutdown Integral latch method Short-circuit protection
Soft-Start Time	: 1ms (TYP.) internally set
Voltage Detector	: 0.712V Detection, N-channel open drain
Built-in P-channel MOSFET	: 0.21Ω
Built-in Synchronous N-channel MOSFET	: 0.23Ω (No Schottky Barrier Diode Required)
High Efficiency	: 95% (V_{IN}=5.0V, V_{OUT}=3.3V)
Synchronized with an External Clock Signal	
Ceramic Capacitor Compatible	
Packages	: MSOP-10, USP-10B
* SOP-8 package is available for the XC9223D type only.	
Environmentally Friendly	: EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

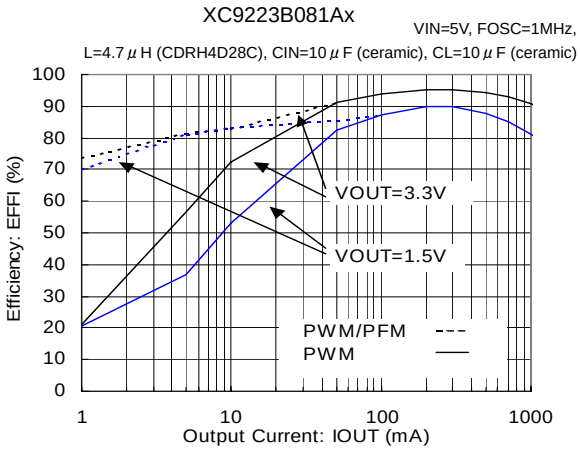


(*1) A capacitor of 2200pF~0.1μF is recommended to place at the C_{DD} between the AGND pin and the V_{IN} pin.

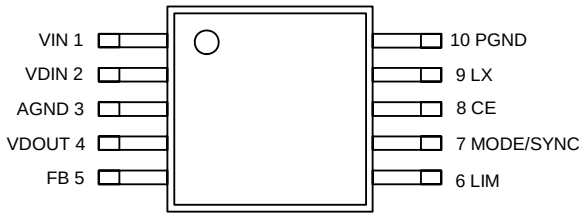
Please refer to the page showing INSTRUCTION ON PATTERN LAYOUT for more detail.

■TYPICAL PERFORMANCE CHARACTERISTICS

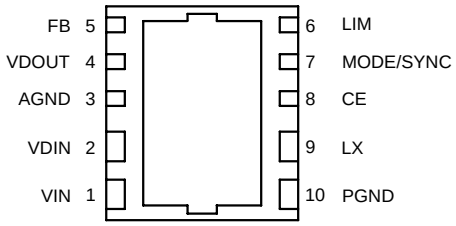
●Efficiency vs. Output Current



■PIN CONFIGURATION



MSOP-10
(TOP VIEW)



USP-10B
(BOTTOM VIEW)

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
MSOP-10 *	USP-10B *		
1	1	VIN	Input
2	2	VDIN	Voltage Detector Input
3	3	AGND	Analog Ground
4	4	VDOUT	VD Output
5	5	FB	Output Voltage Monitor
6	6	LIM	Over Current Limit Setting
7	7	MODE/SYNC	Mode Switch / External Clock Input
8	8	CE	Chip Enable
9	9	Lx	Output of Internal Power Switch
10	10	PGND	Power Ground

* For MSOP-10 and USP-10B packages, please short the GND pins (pin #3 and 10)

■FUNCTION CHART

1. CE Pin Function

CE PIN	OPERATIONAL STATE
H	ON
L	OFF *1

*1: Except for a voltage detector block in the XC9224 series.

2. MODE Pin Function

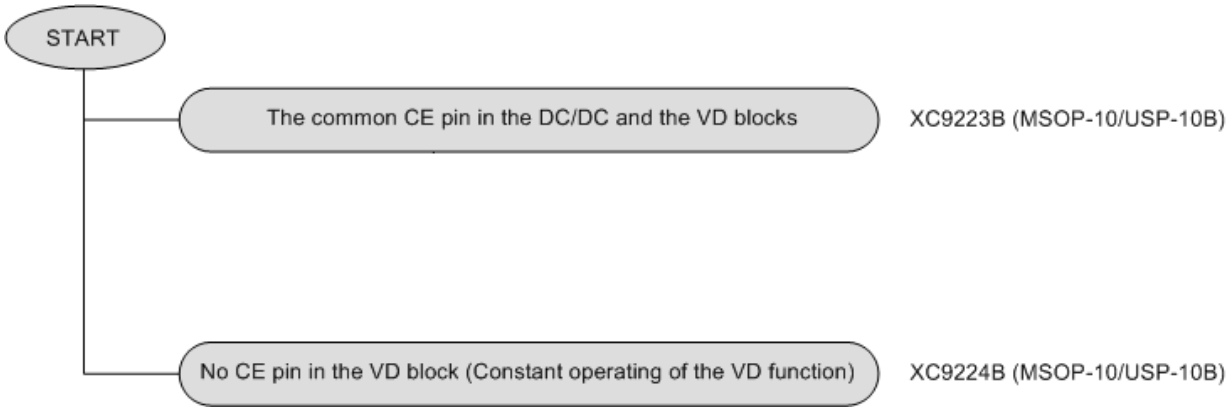
MODE PIN	FUNCTION
H	PWM Control
L	PWM/PFM Automatic Control

3. LIM Pin Function

LIM PIN	FUNCTION
H	Maximum Output Current: 1.0A
L	Maximum Output Current: 0.4A

■PRODUCT CLASSIFICATION

●Selection Guide



●Ordering Information

XC9223①②③④⑤⑥−⑦(*1) <The common CE pin in the DC/DC block and the voltage detector block.>
XC9224①②③④⑤⑥−⑦(*1) <No CE pin in the voltage detector block. (Constant operating of the voltage detector block) >

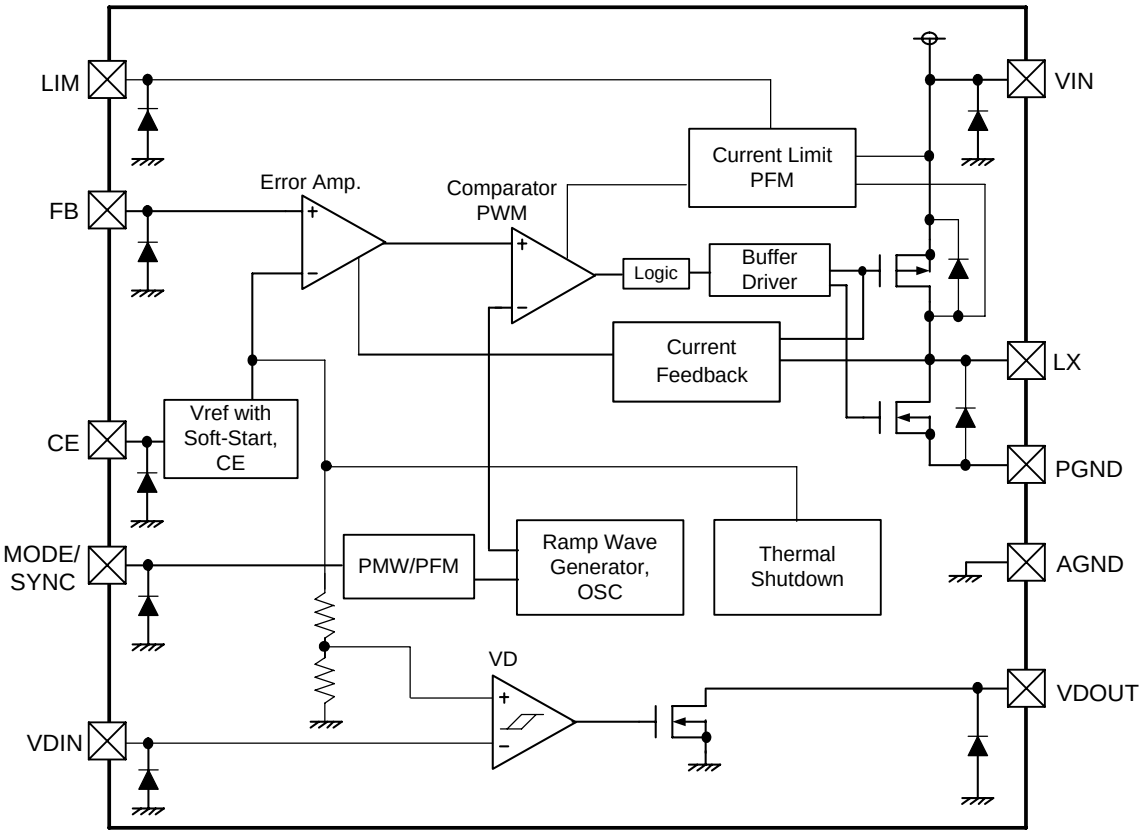
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	B	Transistor built-in, Output voltage freely set (FB voltage), Current Limit: 0.6A/1.2A
②③	Reference Voltage	08	Fixed reference voltage ①=0, ②=8
④	DC/DC Oscillation Frequency	1	1.0MHz
		2	2.0MHz
⑤⑥−⑦	Packages (Order Unit)	AR	MSOP-10 (1,000/Reel)
		AR-G	MSOP-10 (1,000/Reel)
		DR	USP-10B (3,000/Reel)
		DR-G	USP-10B (3,000/Reel)

(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

■BLOCK DIAGRAM

Ta=25°C

●XC9223B/XC9224B Series



■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage		V_{IN}	- 0.3 ~ 6.5	V
V_{DIN} Pin Voltage		V_{DIN}	- 0.3 ~ 6.5	V
V_{DOUT} Pin Voltage		V_{DOUT}	- 0.3 ~ 6.5	V
V_{DOUT} Pin Current		I_{DOUT}	10	mA
FB Pin Voltage		V_{FB}	- 0.3 ~ 6.5	V
LIM Pin Voltage		V_{LIM}	- 0.3 ~ 6.5	V
MODE/SYNC Pin Voltage		$V_{MODE/SYNC}$	- 0.3 ~ 6.5	V
CE Pin Voltage		V_{CE}	- 0.3 ~ 6.5	V
Lx Pin Voltage		V_{Lx}	- 0.3 ~ V_{DD} + 0.3	V
Lx Pin Current		I_{Lx}	2000	mA
Power Dissipation	MSOP-10	Pd	500 (*1)	mW
	USP-10B		150	
Operating Temperature Range		Topr	- 40 ~ + 85	℃
Storage Temperature Range		Tstg	- 55 ~ +125	℃

*1: When implemented on a PCB.

■ELECTRICAL CHARACTERISTICS

XC9223/XC9224 Series

Topr=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
Input Voltage	V_{IN}		2.5	-	6.0	V	-
FB Voltage	V_{FB}		0.784	0.800	0.816	V	①
Output Voltage Setting Range	V_{OUTSET}		0.9	-	VIN	V	③
Maximum Output Current 1 (*1)	$I_{OUTMAX1}$		0.4	-	-	A	③
Maximum Output Current 2 (*1)	$I_{OUTMAX2}$		1.0	-	-	A	③
U.V.L.O. Voltage	V_{UVLO}	FB=V_{FB} x 0.9, V_{IN} Voltage which Lx pin voltage holding 'L' level (*8)	1.55	1.80	2.00	V	①
Supply Current 1	I_{DD1}	FB=V_{FB} x 0.9, MODE/SYNC=0V		D1-1 (*2)		μA	②
Supply Current 2	I_{DD2}	FB=V_{FB} x 1.1 (Oscillation stops), MODE/SYNC=0V		D1-2 (*2)		μA	②
Stand-by Current	I_{STB}	CE=0V		D1-6 (*2)		μA	②
Oscillation Frequency	fosc	Connected to external components, I_{OUT}=10mA		D1-3 (*2)		MHz	③
External Clock Signal Synchronized Frequency	SYNCOSC	Connected to external components, I_{OUT}=10mA, apply an external clock signal to the MODE/SYNC		D1-4 (*2)		MHz	④
External Clock Signal Cycle	SYNCDTY		25	-	75	%	④
Maximum Duty Cycle	MAXDTY	FB=V_{FB} x 0.9	100	-	-	%	①
Minimum Duty Cycle	MINDTY	FB=V_{FB} x 1.1	-	-	0	%	①
PFM Switch Current	I_{PFM}	Connected to external components, MODE/SYNC=0V, I_{OUT}=10mA	-	200	250	mA	③
Efficiency (*3)	EFFI	Connected to external components, V_{IN}=5.0V, V_{OUT}=3.3V, I_{OUT}=200mA	-	95	-	%	③
Lx SW 'H' On Resistance (*4)	R_{LxH}	FB=V_{FB} x 0.9, I_{Lx}=V_{IN}-0.05V	-	0.21	0.3 (*7)	Ω	①
Lx SW 'L' On Resistance	R_{LxL}		-	0.23	0.3 (*7)	Ω	-
Current Limit 1	I_{LIM1}	LIM=0V	0.6	-	0.9	A	①
Current Limit 2	I_{LIM2}	LIM=V_{IN}	1.2	-	2.0	A	①
Integral Latch Time (*5)	T_{LAT}	FB=V_{FB} x 0.9, Short Lx by 1Ω resistance		D1-5 (*2)		ms	①
Short Detect Voltage	V_{SHORT}	FB Voltage which Lx becomes 'L' (*8)	0.3	0.4	0.5	V	①
Soft-Start Time	T_{SS}	CE=0V→V_{IN}, I_{OUT}=1mA	0.5	1.0	2.0	ms	①
Thermal Shutdown Temperature	T_{TSD}		-	150	-	°C	-
Hysteresis Width	T_{HYS}		-	20	-	°C	-
CE 'H' Voltage	V_{CEH}	FB=V_{FB} x 0.9, Voltage which Lx becomes 'H' after CE voltage changed from 0.4V to 1.2V (*8)	1.2	-	-	V	①
CE 'L' Voltage	V_{CEL}	FB=V_{FB} x 0.9, Voltage which Lx becomes 'L' after CE voltage changed from 1.2V to 0.4V (*8)	-	-	0.4	V	①
MODE/SYNC 'H' Voltage	$V_{MODE/SYNCH}$		1.2	-	-	V	③
MODE/SYNC 'L' Voltage	$V_{MODE/SYNCL}$		-	-	0.4	V	③
LIM 'H' Voltage	V_{LIMH}		1.2	-	-	V	①
LIM 'L' Voltage	V_{LIML}	I_{OUT}=I_{LIM1} x 1.1, Check LIM voltage which Lx oscillated after CE voltage changed from 1.2V to 0.4V	-	-	0.4	V	①
CE 'H' Current	I_{CEH}	V_{IN}=CE=6.0V	-	-	0.1	A	⑤
CE 'L' Current	I_{CEL}	V_{IN}=6.0V, CE=0V	- 0.1	-	-	μA	⑤
MODE/SYNC 'H' Current	$I_{MODE/SYNCH}$	V_{IN}=6.0V	-	-	0.1	μA	⑤
MODE/SYNC 'L' Current	$I_{MODE/SYNCL}$	V_{IN}=6.0V, MODE/SYNC=0V	- 0.1	-	-	μA	⑤
LIM 'H' Current	I_{LIMH}	V_{IN}=LIM=6.0V	-	-	0.1	μA	⑤
LIM 'L' Current	I_{LIML}	V_{IN}=6.0V, LIM=0V	- 0.1	-	-	μA	⑤
FB 'H' Current	I_{FBH}	V_{IN}=FB=6.0V	-	-	0.1	μA	⑤
FB 'L' Current	I_{FBL}	V_{IN}=6.0V, FB=0V	- 0.1	-	-	μA	⑤
Lx SW 'H' Leak Current	I_{LeakH}	V_{IN}=Lx=6.0V, CE=0V	-	-	1.0	μA	⑥
Lx SW 'L' Leak Current (*6)	I_{LeakL}	V_{IN}=6.0V, Lx=CE=0V	- 3.0	-	-	μA	⑥

■ELECTRICAL CHARACTERISTICS (Continued)

XC9223/XC9224 Series (Continued), Voltage Detector Block

Topr=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
Detect Voltage	V_{DF}	V_{DIN} Voltage which V_{DOUT} becomes 'H' to 'L', Pull-up resistor 200kΩ	0.676	0.712	0.744	V	⑦
Release Voltage	V_{DR}	V_{DIN} Voltage which V_{DOUT} becomes 'L' to 'H', Pull-up resistor 200kΩ	0.716	0.752	0.784	V	⑦
Hysteresis Width	V_{HYS}	$V_{HYS}=(V_{DR}-V_{DF}) / V_{DF}$ x 100	-	5	-	%	-
Output Current	I_{DOUT}	$V_{DIN}=V_{DF}$ x 0.9, apply 0.25V to V_{DOUT}	2.5	4.0	-	mA	⑦
Delay Time	T_{DLY}	Time until V_{DOUT} becomes 'L' to 'H' after V_{DIN} changed from 0V to 1.0V	0.5	2.0	8.0	ms	⑦
V_{DIN} 'H' Current	I_{VDINH}	$V_{IN}=V_{DIN}=6.0V$	-	-	0.1	μA	⑤
V_{DIN} 'L' Current	I_{VDINL}	$V_{IN}=6.0V$, $V_{DIN}=0V$	- 0.1	-	-	μA	⑤
V_{DOUT} 'H' Current	I_{VDOUTH}	$V_{IN}=V_{DIN}=V_{DOUT}=6.0V$	-	-	1.0	μA	⑤
V_{DOUT} 'L' Current	I_{VDOUTL}	$V_{IN}=V_{DIN}=6.0V$, $V_{DOUT}=0V$	- 1.0	-	-	μA	⑤

Test Condition: Unless otherwise stated, V_{IN}=3.6V, CE=V_{IN}, MODE/SYNC=V_{IN}

NOTE:

*1: When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.

*2: Refer to the chart below.

*3: EFFI = { (output voltage x output current) / (input voltage x input current) } x 100

*4: On resistance (Ω)= (V_{IN}- Lx pin measurement voltage) / 100mA

*5: Time until it short-circuits Lx with GND through 1Ω of resistance from a state of operation and is set to Lx=Low from current limit pulse generating.

*6: When temperature is high, a current of approximately 100μA may leak.

*7: Designed value.

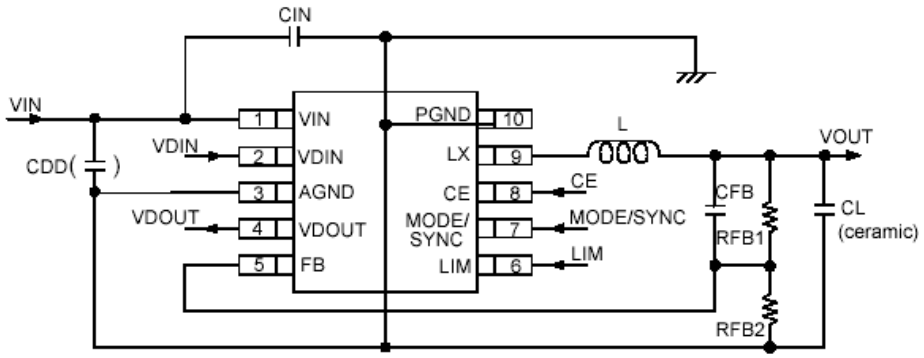
*8: Whether the Lx pin is high level or low level is judged at the condition of "H">V_{IN}-0.1V and "L"<0.05V.

●Electrical Characteristics Standard Values

No.	PARAMETER	SYMBOL	1MHz			2MHz		
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
D1-1	Supply Current 1	I_{DD1}	-	380	700	-	440	800
D1-2	Supply Current 2	I_{DD2}	-	30	60	-	45	80
D1-3	Oscillation Frequency	F_{OSC}	0.85	1.00	1.15	1.7	2.0	2.3
D1-4	External Clock Synchronous Oscillation	SYNCOSC	0.75	-	1.25	1.5	-	2.5
D1-5	Integral Latch Time	T_{LAT}	-	6.0	15.0	-	3.0	15.0

No.	PARAMETER	SYMBOL	XC9223 SERIES			XC9224 SERIES		
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
D1-6	Stand-by Current	I_{STB}	-	0.1	2.0	-	7.0	15.0

■TYPICAL APPLICATION CIRCUIT



(*1) A capacitor of 2200pF~0.1μF is recommended to place at the C_{DD} between the AGND pin and the V_{IN} pin.
Please refer to the page showing INSTRUCTION ON PATTERN LAYOUT for more detail.

<Output Voltage Setting>
Output voltage can be set by adding external split resistors. Output voltage is determined by the following equation, based on the values of R_{FB1} and R_{FB2}. The sum of R_{FB1} and R_{FB2} should normally be 1MΩ or less.
$V_{OUT} = 0.8 \times (R_{FB1} + R_{FB2}) / R_{FB2}$

The value of CFB, speed-up capacitor for phase compensation, should be $fzfb = 1 / (2 \times \pi \times C_{FB1} \times R_{FB1})$ which is equal to 20kHz. Adjustments are required from 1kHz to 50kHz depending on the application, value of inductance (L), and value of load capacity (CL).

[Example of calculation]
When R_{FB1}=470kΩ, R_{FB2}=150kΩ,
$V_{OUT1} = 0.8 \times (470k + 150k) / 150k = 3.3V$

[Typical example]

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{FB} (pF)	V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{FB} (pF)
1.0	75	300	110	2.5	510	240	15
1.2	150	300	51	3.0	330	120	24
1.5	130	150	62	3.3	470	150	18
1.8	300	240	27	5.0	430	82	18

* When fzfb = 20kHz

[External components]
1MHz:
L: 4.7μH (CDRH4D28C, SUMIDA)
C_L: 10μF (ceramic)
C_{IN}: 10μF (ceramic)

2MHz:
L: 2.2μH (CDRH4D28, SUMIDA)
2.2μH (VLCF4020T-2R2N1R7, TDK)
C_L: 10μF (ceramic)
C_{IN}: 10μF (ceramic)

* As for C_{IN} and C_L, use output capacitors of 10μF or more. (Ceramic capacitor compatible)
* High ESR (Equivalent Series Resistance) that comes by using a tantalum or an electrolytic capacitor causes high ripple voltage. Furthermore, it can cause an unstable operation. Use the IC after you fully confirm with an actual device.

■OPERATIONAL EXPLANATION

Each unit of the XC9223/XC9224 series consists of a reference voltage source, a ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, output voltage adjustment resistors, P-channel MOS driver transistor, N-channel MOS synchronous rectification switching transistor, current limiter circuit, U.V.L.O. circuit and others. The series compares, using the error amplifier, the internal reference voltage to the VOUT pin with the voltage feedback via resistors RFB1 and RFB2. Phase compensation is performed on the resulting error amplifier output, to input a signal to the PWM comparator to determine the turn-on time during PWM operation. The PWM comparator compares, in terms of voltage level, the signal from the error amplifier with the ramp wave from the ramp wave circuit, and delivers the resulting output to the buffer driver circuit to cause the Lx pin to output a switching duty cycle. This process is continuously performed to ensure stable output voltage. The current feedback circuit monitors the P-channel MOS driver transistor current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when a low ESR capacitor, such as a ceramic capacitor, is used, ensuring stable output voltage.

<Reference Voltage Source>
The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

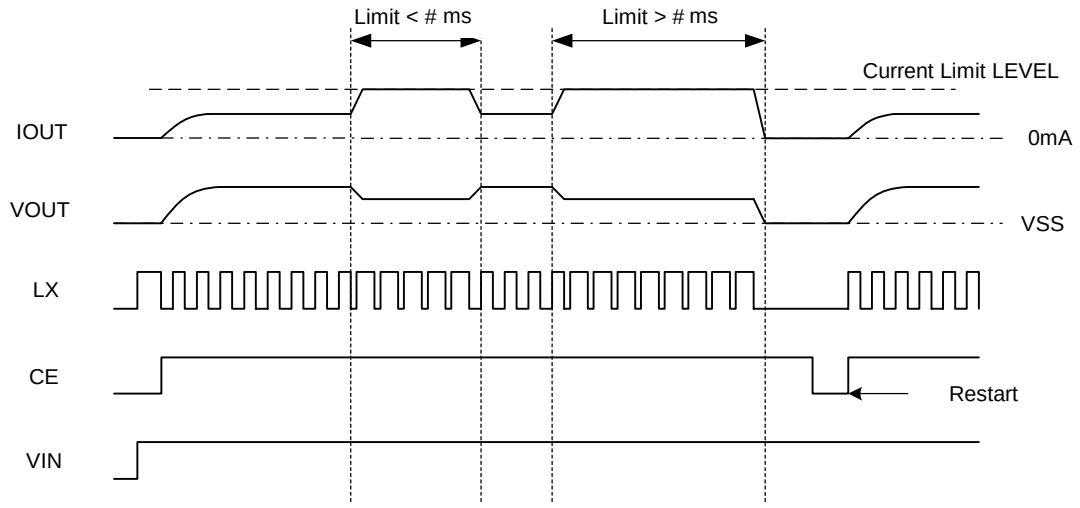
<Ramp Wave Circuit>
The ramp wave circuit determines switching frequency. The frequency is fixed internally and can be selected from 1.0MHz and 2.0MHz. Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

<Error Amplifier>
The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal resistors (RFB1 and RFB2). When a voltage lower than the reference voltage is fed back, the output voltage of the error amplifier increases. The gain and frequency characteristics of the error amplifier output are fixed internally to deliver an optimized signal to the mixer.

<Current Limit>
The current limiter circuit of the XC9223/XC9224 series monitors the current flowing through the P-channel MOS driver transistor connected to the Lx pin, and features a combination of the constant-current type current limit mode and the operation suspension mode. For the current limit values, please select the values either from 1.2A (MIN.) when the LIM pin is high level or 0.6A (MIN.) when the LIM pin is low level.

①When the driver current is greater than a specific level, the constant-current type current limit function operates to turn off the pulses from the Lx pin at any given time.
②When the driver transistor is turned off, the limiter circuit is then released from the current limit detection state.
③At the next pulse, the driver transistor is turned on. However, the transistor is immediately turned off in the case of an over current state.
④ When the over current state is eliminated, the IC resumes its normal operation.

The IC waits for the over current state to end by repeating the steps ① through ③. If an over current state continues for several msec and the above three steps are repeatedly performed, the IC performs the function of latching the OFF state of the driver transistor, and goes into operation suspension mode. After being put into suspension mode, the IC can resume operation by turning itself off once and then starting it up using the CE pin, or by restoring power to the VIN pin. Integral latch time may be released from a current limit detection state because of the noise. Depending on the state of a substrate, it may result in the case where the latch time may become longer or the operation may not be latched. Please locate an input capacitor as close as possible.



■OPERATIONAL EXPLANATION (Continued)

<Thermal Shutdown>
For protection against heat damage of the ICs, thermal shutdown function monitors chip temperature. The thermal shutdown circuit starts operating and the driver transistor will be turned off when the chip's temperature reaches 150°C. When the temperature drops to 130°C or less after shutting of the current flow, the IC performs the soft start function to initiate output startup operation.

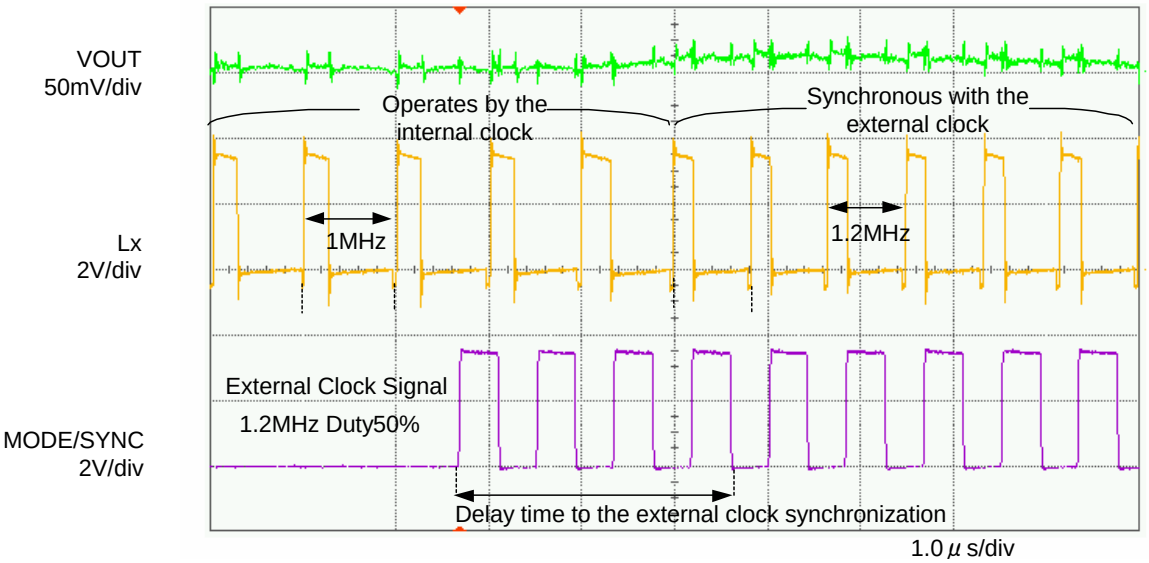
<Short-Circuit Protection>
The short-circuit protection circuit monitors FB voltage. In case where output is accidentally shorted to the Ground and when the FB voltage decreases less than half of the FB voltage, the short-circuit protection operates to turn off and to latch the driver transistor. In latch mode, the operation can be resumed by either turning the IC off and on via the CE pin, or by restoring power supply to the VIN pin.

<Voltage Detector>
The detector block of the XC9223/9224 series detects a signal inputted from the VDIN pin by the VDOUT pin (N-ch open-drain).

<U.V.L.O. Circuit>
When the VIN pin voltage becomes 1.8V (TYP.) or lower, the driver transistor is forced OFF to prevent false pulse output caused by unstable operation of the internal circuitry. When the VIN pin voltage becomes 2.0V (TYP.) or higher, switching operation takes place. By releasing the U.V.L.O. function, the IC performs the soft-start function to initiate output startup operation. The U.V.L.O. function operates even when the VIN pin voltage falls below the U.V.L.O. operating voltage for tens of ns.

<MODE/SYNC>
A MODE/SYNC pin has two functions, a MODE switch and an input of external clock signal. The MODE/SYNC pin operates as the PWM mode when applying high level of direct current and the PFM/PWM automatic switching mode by applying low level of direct current, which is the same function as the normal MODE pin. By applying the external clock signal (±25% of the internal clock signal, ON duty 25% to 75%), the MODE/SYNC pin switches to the internal clock signal. Also the circuit will synchronize with the falling edge of external clock signal. While synchronizing with the external clock signal, the MODE/SYNC pin becomes the PWM mode automatically. If the MODE/SYNC pin holds high or low level of the external clock signal for several μs, the MODE/SYNC pin stops synchronizing with the external clock and switches to the internal clock operation. (Refer to the chart below.)

・External Clock Synchronization Function

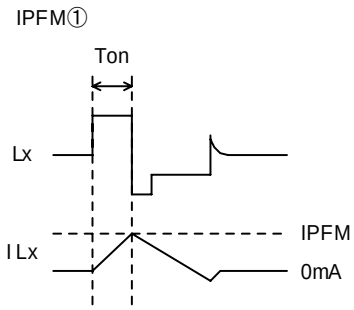


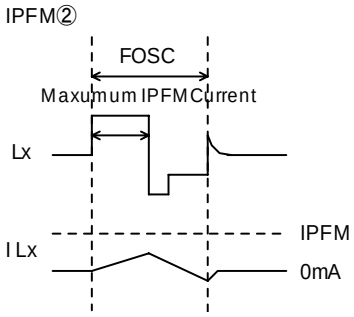
* When an input of MODE/SYNC is changed from "L" voltage into a clock signal of 1.2MHz and 50% duty.

■OPERATIONAL EXPLANATION (Continued)

<PFM Switch Current>
In PFM control operation, until coil current reaches to a specified level (I_{PFM}), the IC keeps the P-ch MOSFET on. In this case, time that the P-ch MOSFET is kept on (TON) can be given by the following formula.
$TON = L \times I_{PFM} / (V_{IN} - V_{OUT})$ →I_{PFM}①

<Maximum I_{PFM} Limit>
In PFM control operation, the maximum duty cycle (MAXPFM) is set to 50% (TYP.). Therefore, under the condition that the duty increases (e.g. the condition that the step-down ratio is small), it's possible for P-ch MOSFET to be turned off even when coil current doesn't reach to I_{PFM}. →I_{PFM}②

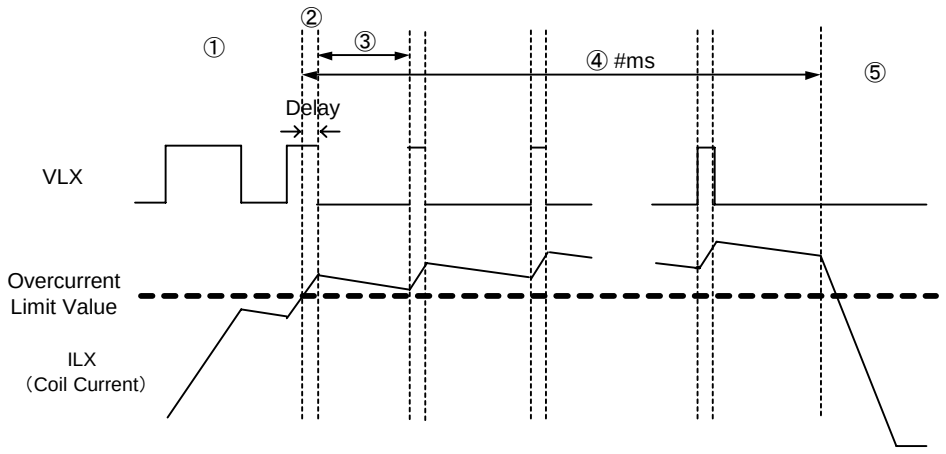




■NOTES ON USE

1. The XC9223/XC9224 series is designed for use with ceramic output capacitors. If, however, the potential difference between dropout voltage, a ceramic capacitor may fail to absorb the resulting high switching energy and oscillation could occur on the output. In this case, use a larger capacitor etc. to compensate for insufficient capacitance.
2. Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.
3. In PWM control, very narrow pulses will be outputted, and there is the possibility that some cycles may be skipped completely. This may happens while synchronizing with an external clock.
4. When the difference between V_{IN} and V_{OUT} is small, and the load current is heavy, very wide pulses will be outputted and there is the possibility that some cycles may be skipped completely.
5. With the IC, the peak current of the coil is controlled by the current limit circuit. Since the peak current increases when dropout voltage or load current is high, current limit starts operating, and this can lead to instability. When peak current becomes high, please adjust the coil inductance value and fully check the circuit operation. In addition, please calculate the peak current according to the following formula:
   $Ipk = (V_{IN} - V_{OUT}) \times OnDuty / (2 \times L \times fosc) + I_{DOUT}$
   L: Coil Inductance Value
   fosc: Oscillation Frequency
6. When the peak current, which exceeds limit current, flows within the specified time, the built-in P-ch driver transistor is turned off (an integral latch circuit). During the time until it detects limit current and before the built-in transistor can be turned off, the current for limit current flows; therefore, care must be taken when selecting the rating for the coil.
7. The voltage drops because of ON resistance of a driver transistor or in-series resistance of a coil. For this, the current limit may not be attained to the limit current value, when input voltage is low.
8. Malfunction may occur in the U.V.L.O. circuit because of the noise when pulling current at the minimum operation voltage.
9. This IC and the external components should be used within the stated absolute maximum ratings in order to prevent damage to the device.
10. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. The board should be laid out so that capacitors are placed as close to the chip as possible.
11. In heavy load, the noise of DC/DC may influence and the delay time of the voltage detector may be prolonged.
12. Output voltage may become unstable when synchronizing high internal frequency with the external clock. In such a case, please use a larger output capacitor etc. to compensate for insufficient capacitance.
13. When a voltage lower than minimum operating voltage is applied, the output voltage may fall before reaching the over current limit.
14. When the IC is used in high temperature, output voltage may increase up to input voltage level at light load (less than 100 μA) because of the leak current of the driver transistor.
15. The current limit is set to LIM=H: 2000mA (MAX.). However, the current of 2000mA or more may flow. In case that the current limit functions while the V_{OUT} pin is shorted to the GND pin, when P-ch MOSFET is ON, the potential difference for input voltage will occur at both ends of a coil. For this, the time rate of coil current becomes large. By contrast, when N-ch MOSFET is ON, there is almost no potential difference at both ends of the coil since the V_{OUT} pin is shorted to the GND pin. Consequently, the time rate of coil current becomes quite small. According to the repetition of this operation, and the delay time of the circuit, coil current will be converged on a certain current value, exceeding the amount of current, which is supposed to be limited originally. The short protection does not operate during the soft-start time. The short protection starts to operate and the circuit will be disabled after the soft-start time. Current larger than over current limit may flow because of a delay time of the IC when step-down ratio is large. A coil should be used within the stated absolute maximum rating in order to prevent damage to the device.

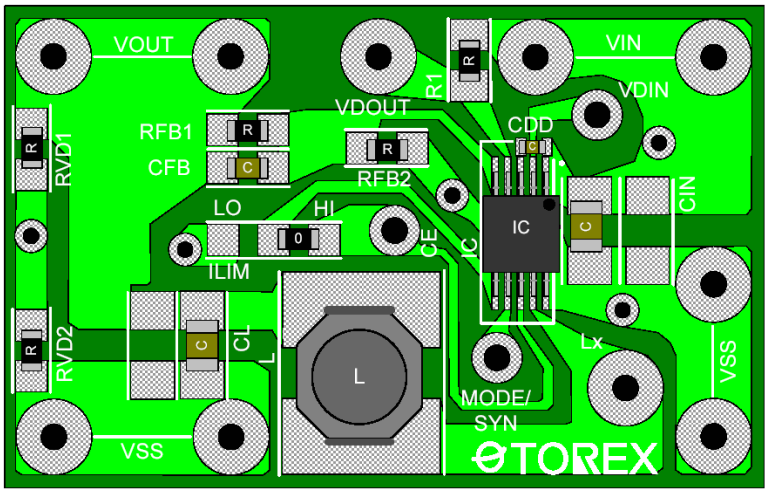
①Current flows into P-ch MOSFET to reach the current limit (I_{LIM}).
②The current of I_{LIM} (2000mA, MAX.) or more flows since the delay time of the circuit occurs during from the detection of the current limit to OFF of P-ch MOSFET.
③Because of no potential difference at both ends of the coil, the time rate of coil current becomes quite small.
④Lx oscillates very narrow pulses by the current limit for several msec.
⑤The short protection operates, stopping its operation.



■INSTRUCTION ON PATTERN LAYOUT

1. In order to stabilize VIN's voltage level, we recommend that a by-pass capacitor (CIN) be connected as close as possible to the VIN & VSS pins.
2. Please mount each external component, especially CIN, as close to the IC as possible.
3. Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
4. Make sure that the PCB GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.
5. Unstable operation may occur at the heavy load because of a spike noise. 2200pF ~0.1μF of a capacitor, CDD, is recommended to use between the AGND pin and the VIN pin for reducing noise.

・TOP VIEW



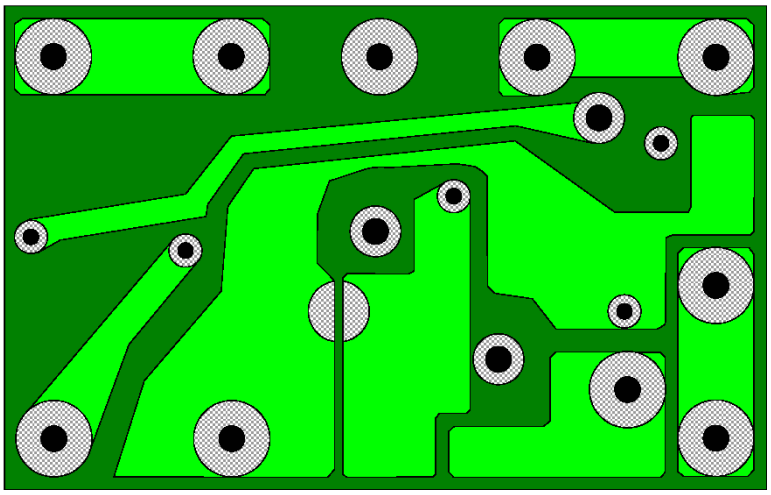
Inductor

Jumper Chip

Resistor

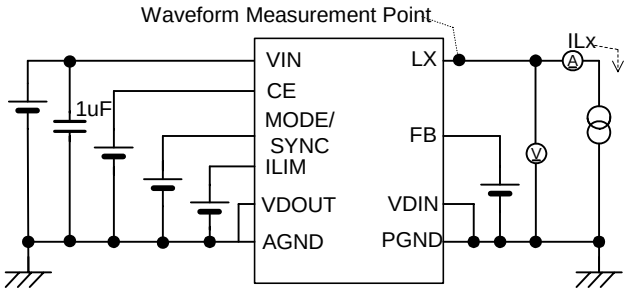
Ceramic Capaticor

・BOTTOM VIEW

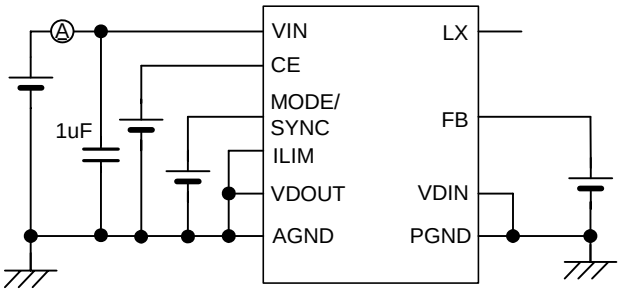


■TEST CIRCUITS

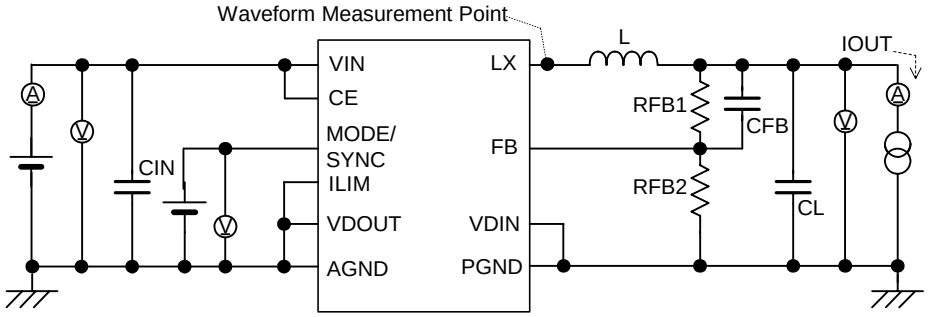
Circuit ①



Circuit ②

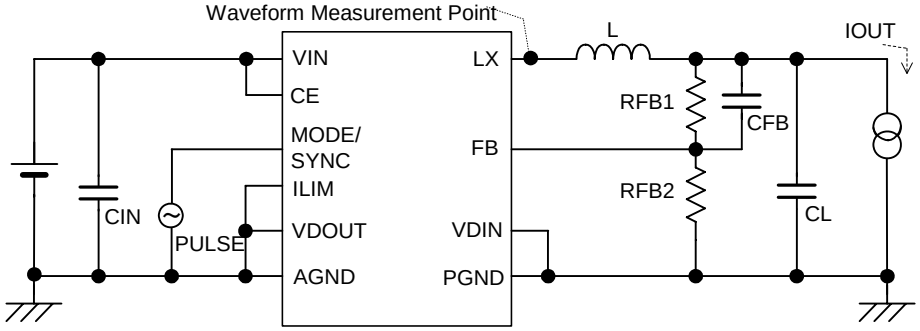


Circuit ③



* External Components
L (1MHz) : 4.7μH (CDRH4D28C, SUMIDA)
L (2MHz) : 2.2μH (VLCF4020T-2R2N1R7, TDK)
CIN : 10μF (ceramic)
CL : 10μF (ceramic)
RFB1 : 130kΩ
RFB2 : 150kΩ
CFB : 62pF (ceramic)

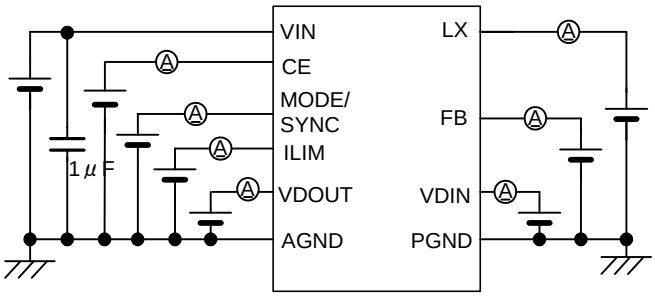
Circuit ④



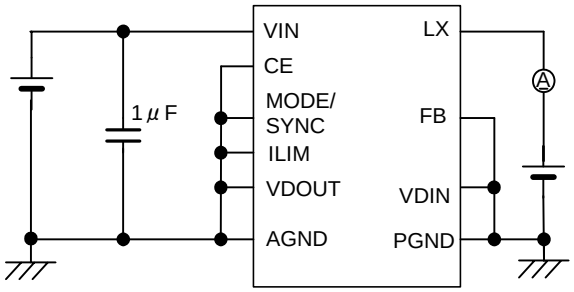
* External Components
L (1MHz) : 4.7μH (CDRH4D28C, SUMIDA)
L (2MHz) : 2.2μH (VLCF4020T-2R2N1R7, TDK)
CIN : 10μF (ceramic)
CL : 10μF (ceramic)
RFB1 : 130kΩ
RFB2 : 150kΩ
CFB : 62pF (ceramic)

■TEST CIRCUITS (Continued)

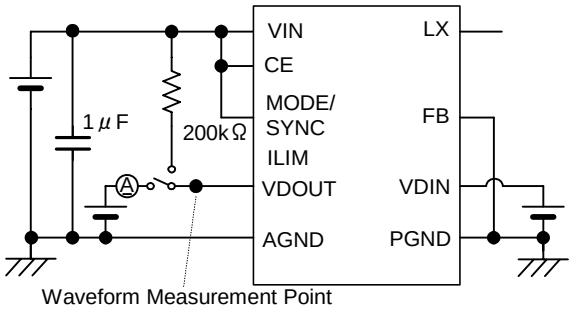
Circuit ⑤



Circuit ⑥



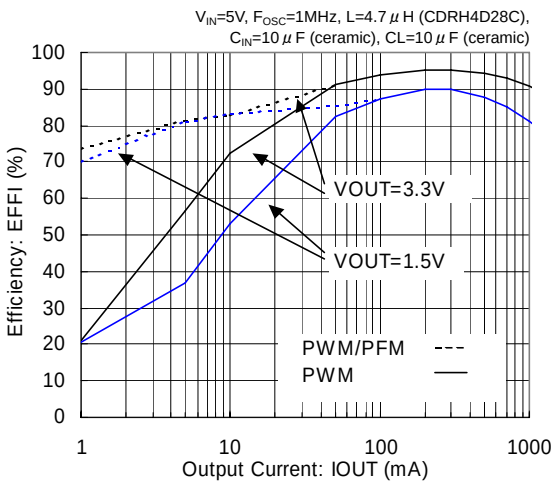
Circuit ⑦



■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output Current

XC9223B081Ax



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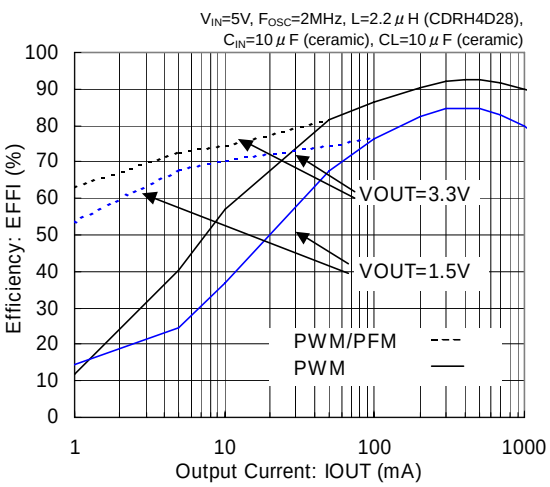

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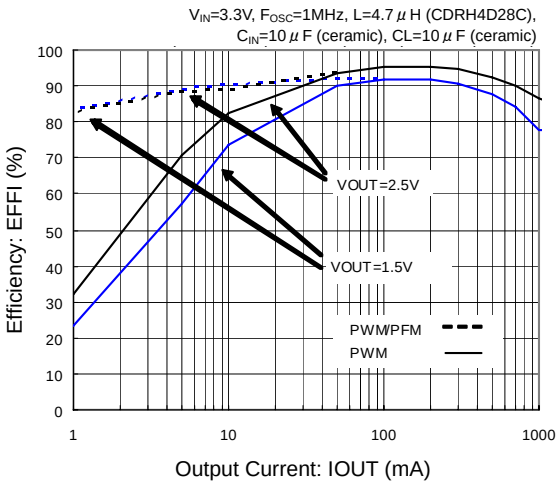

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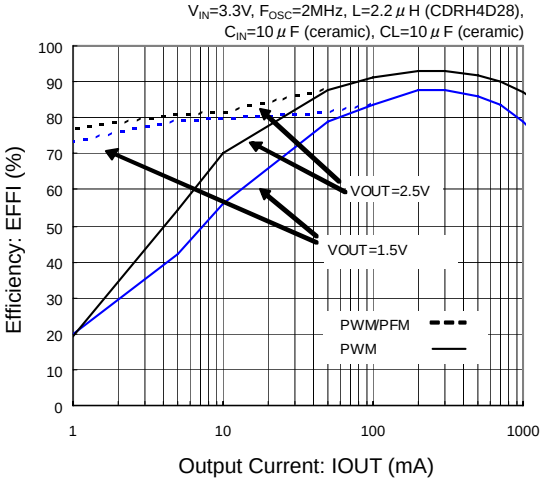
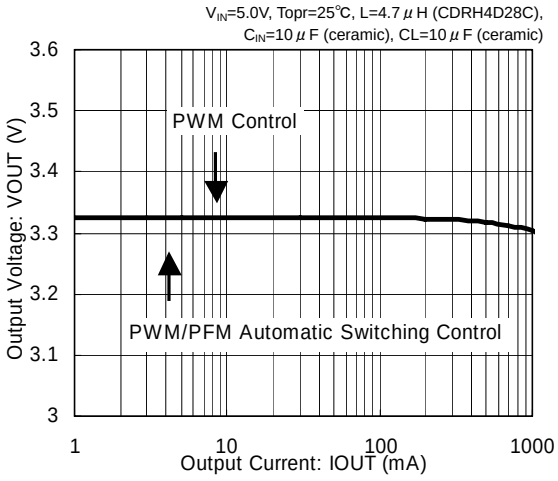


(2) Output Voltage vs. Output Current

XC9223B081Ax



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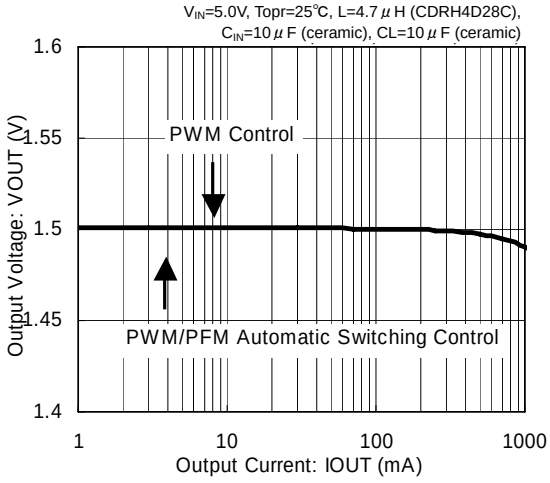
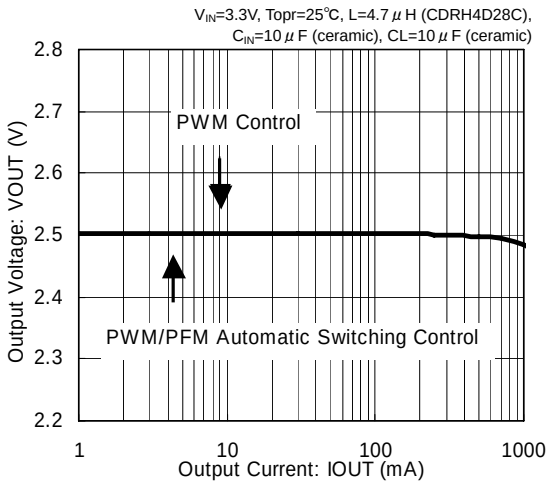


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(2) Output Voltage vs. Output Current (Continued)

XC9223B081Ax



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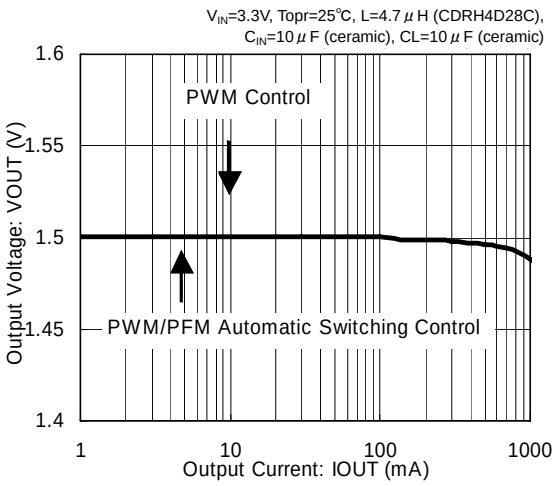
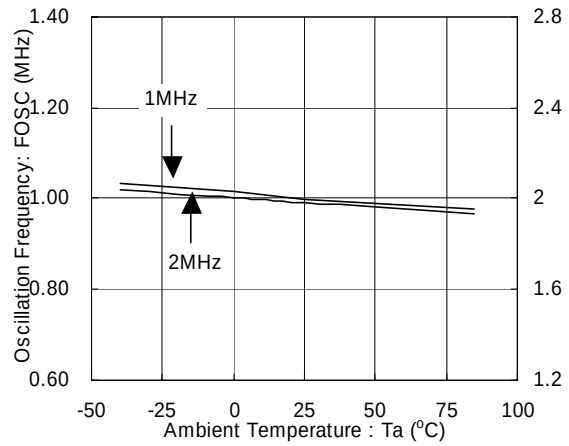


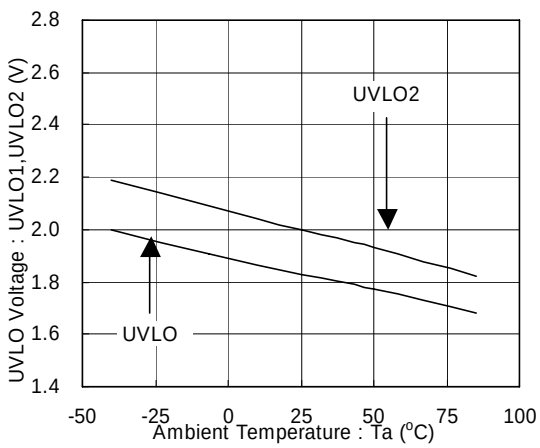
(3) Oscillation Frequency vs. Ambient Temperature

XC9223/XC9224 Series



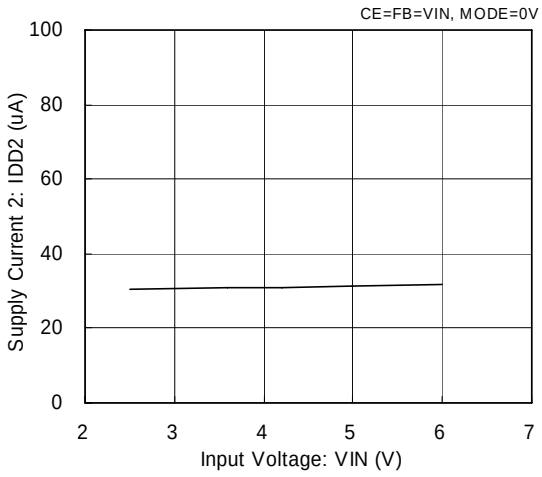
(4) U.V.L.O. Voltage vs. Ambient Temperature

XC9223/XC9224 Series

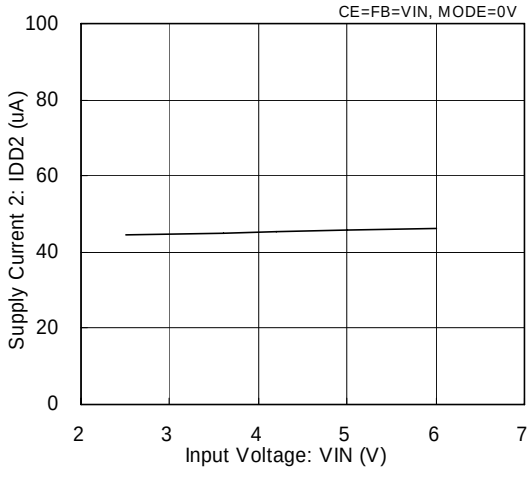


(5) Supply Current 2 vs. Input Voltage

XC9223/XC9224 Series (1MHz)

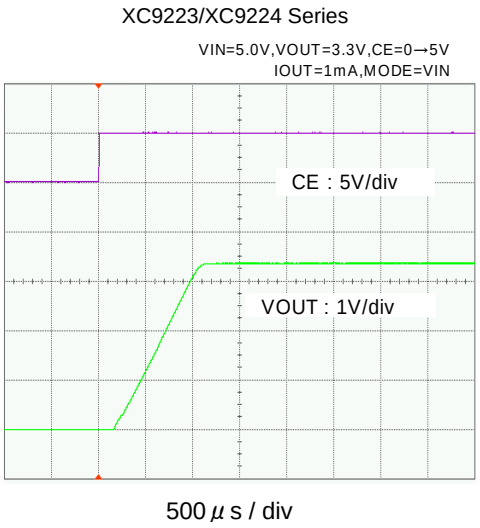


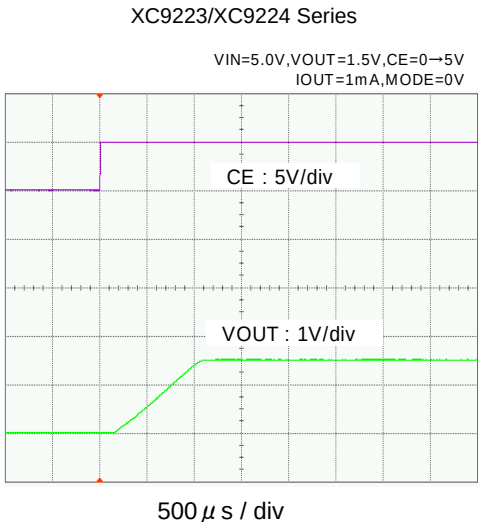
XC9223/XC9224 Series (2MHz)



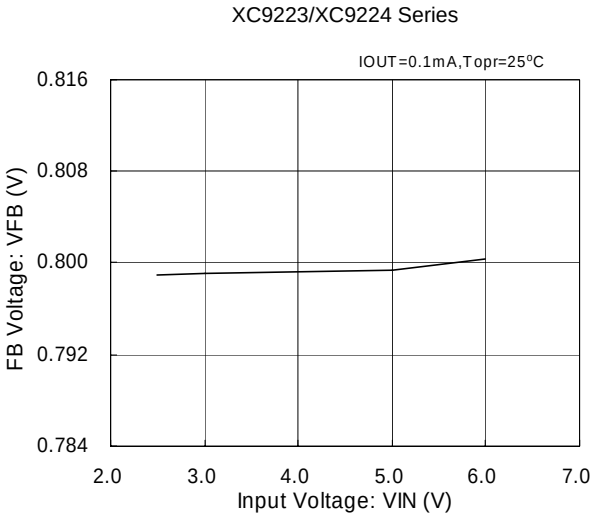
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(6) Soft Start Time





(7) FB Voltage vs. Supply Voltage

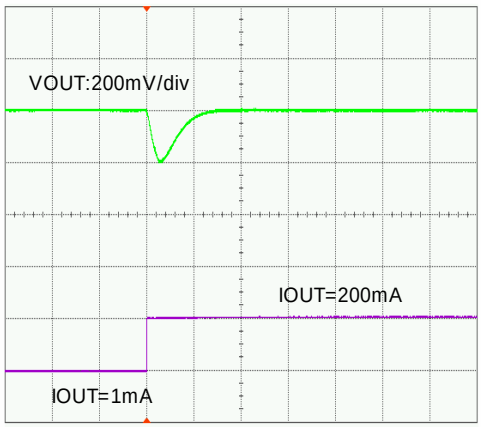


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

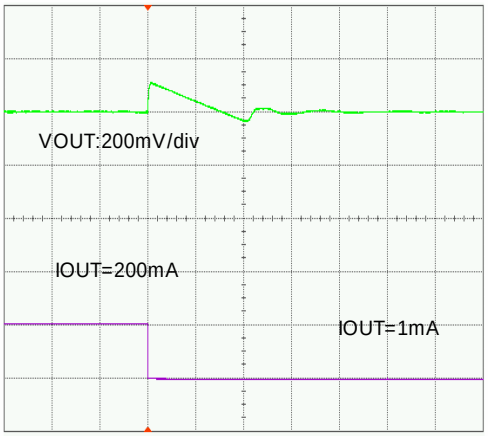
(8) Load Transient Response

XC9223B081Ax <1MHz>

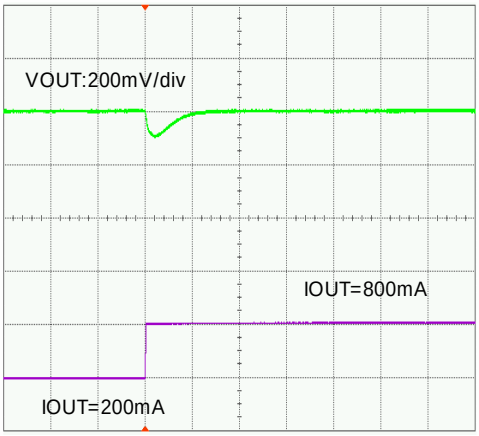
V_{IN}=5.0V, V_{OUT}=3.3V, MODE/SYNC=V_{IN} (PWM control)
L=4.7μH (CDRH4D28C), C_{IN}=10μF (ceramic), C_L=10μF (ceramic), Topr=25°C



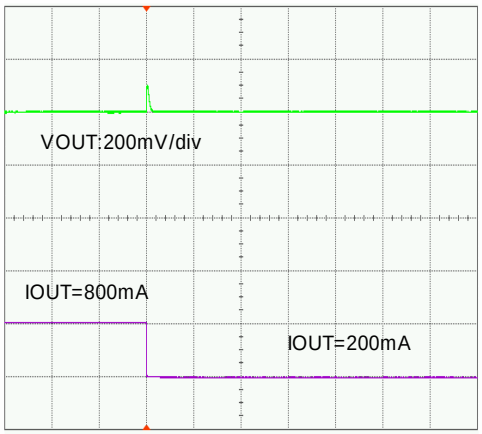
50μs / div



500μs / div

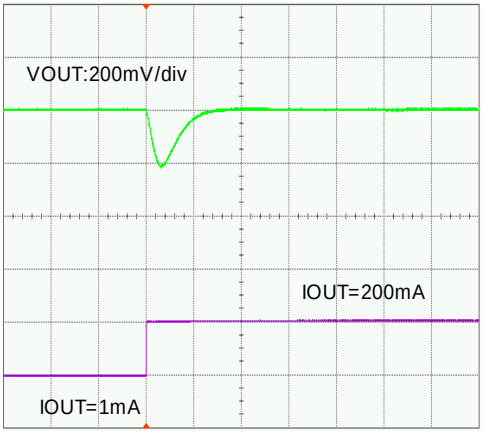


50μs / div

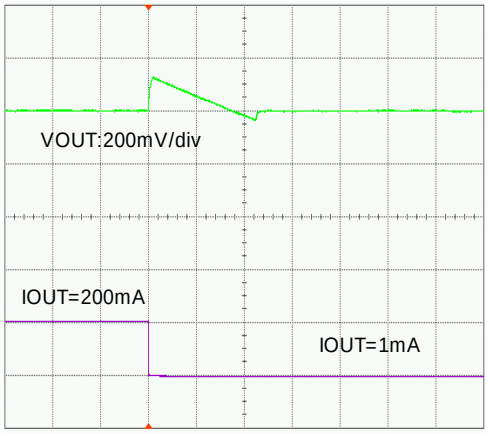


500μs / div

V_{IN}=5.0V, V_{OUT}=3.3V, MODE/SYNC=0V (PWM/PFM automatic switching control)
L=4.7μH (CDRH4D28C), C_{IN}=10μF (ceramic), C_L=10μF (ceramic), Topr=25°C



50μs / div



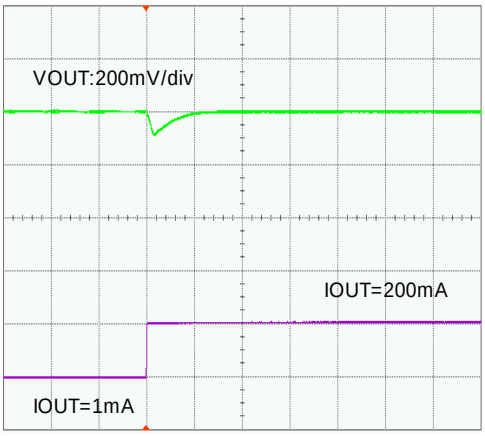
500μs / div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

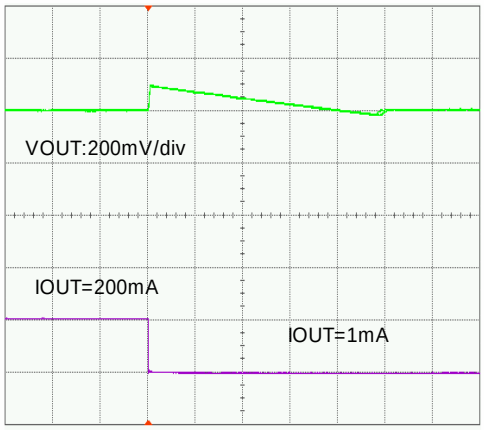
(8) Load Transient Response (Continued)

XC9223B081Ax <1MHz> (Continued)

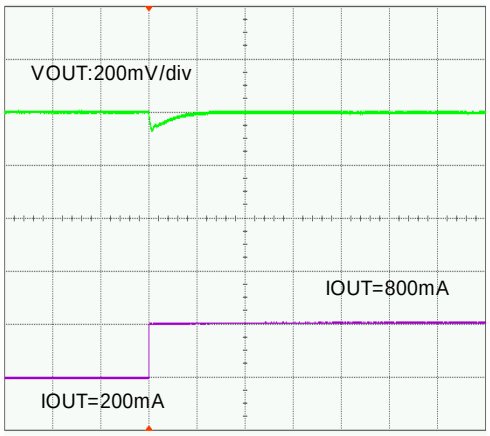
VIN=5.0V, VOUT=1.5V, MODE/SYNC=VIN (PWM control)
L=4.7μH (CDRH4D28C), CIN=10μF (ceramic), CL=10μF (ceramic), Topr=25°C



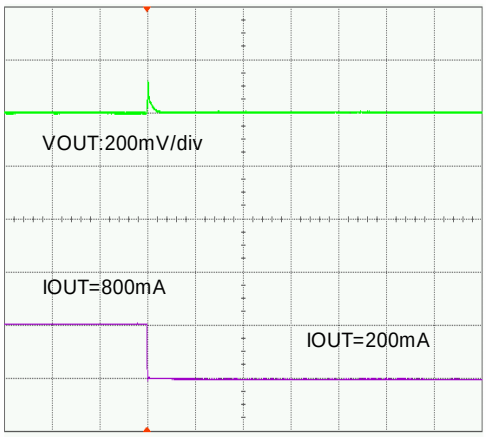
50μs / div



200μs / div

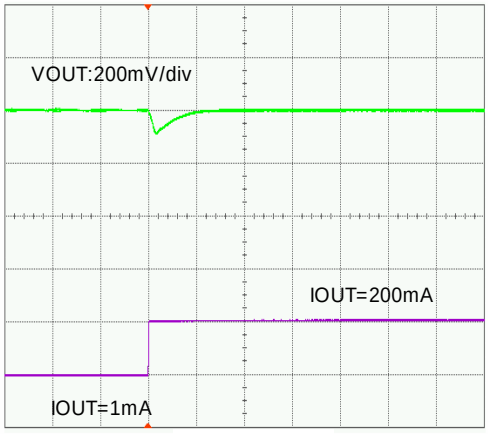


50μs / div

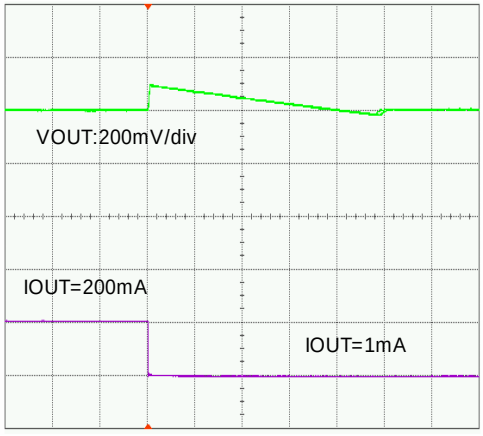


200μs / div

VIN=5.0V, VOUT=1.5V, MODE/SYNC=0V (PWM/PFM automatic switching control)
L=4.7μH (CDRH4D28C), CIN=10μF (ceramic), CL=10μF (ceramic), Topr=25°C



50μs / div



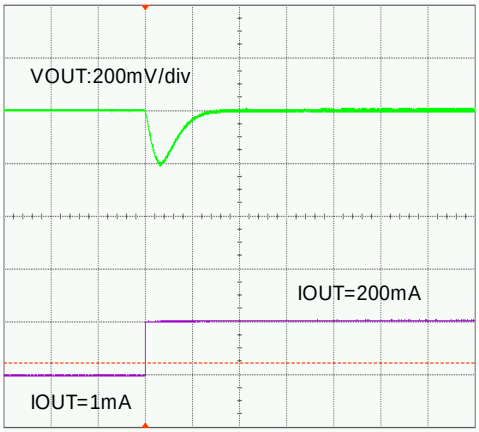
200μs / div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

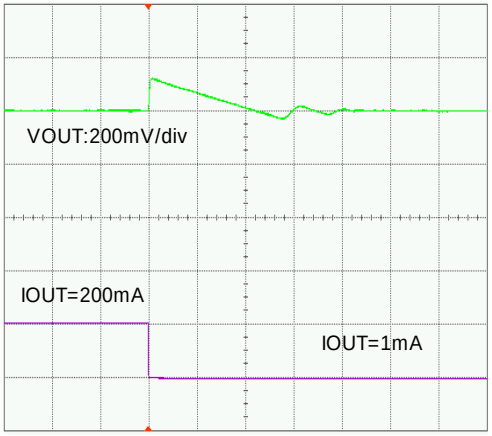
(8) Load Transient Response (Continued)

XC9223B082Ax <2MHz>

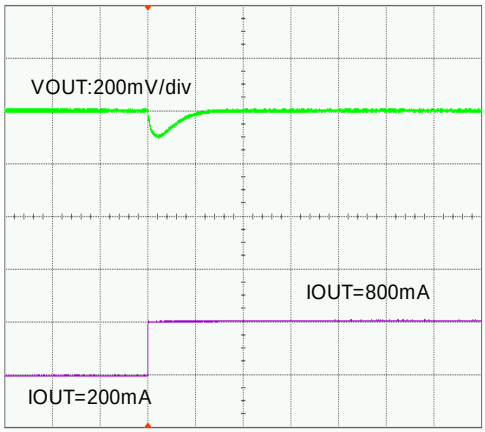
VIN=5.0V, VOUT=3.3V, MODE/SYNC=VIN (PWM control)
L=2.2μH (CDRH4D28), CIN=10μF (ceramic), CL=10μF (ceramic), Topr=25°C



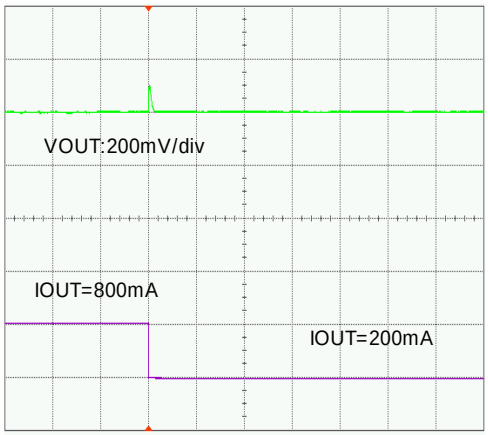
50μs / div



500μs / div

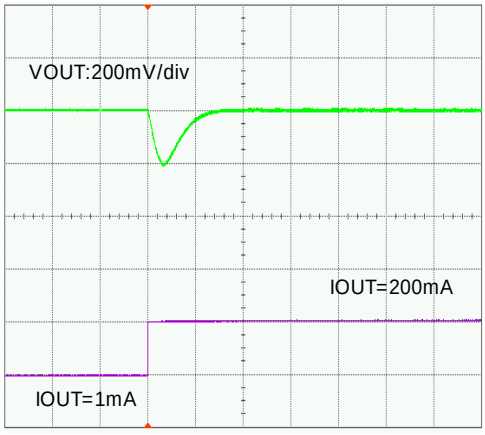


50μs / div

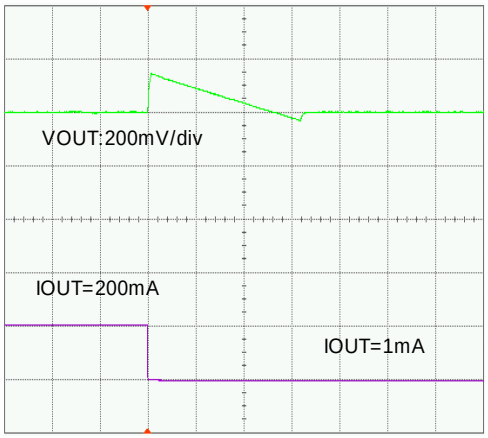


500μs / div

VIN=5.0V, VOUT=3.3V, MODE/SYNC=0V (PWM/PFM automatic switching control)
L=2.2μH (CDRH4D28C), CIN=10μF (ceramic), CL=10μF (ceramic), Topr=25°C



50μs / div



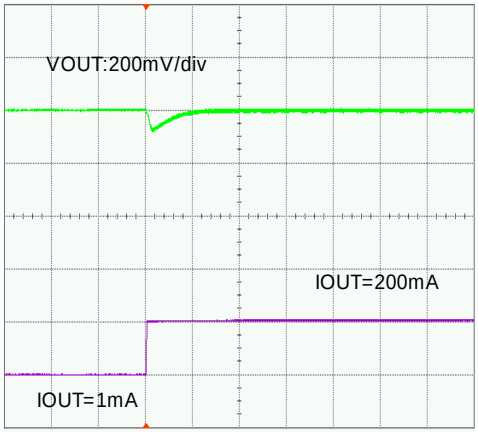
500μs / div

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

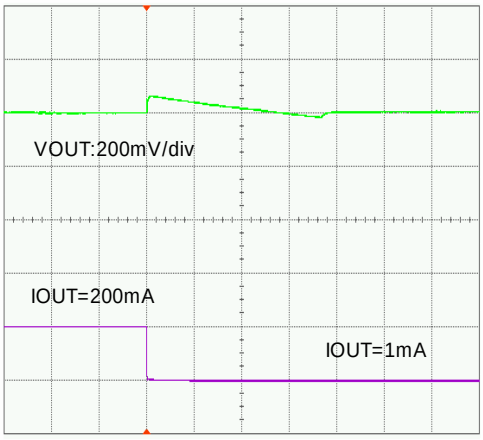
(8) Load Transient Response (Continued)

XC9223B082Ax <2MHz> (Continued)

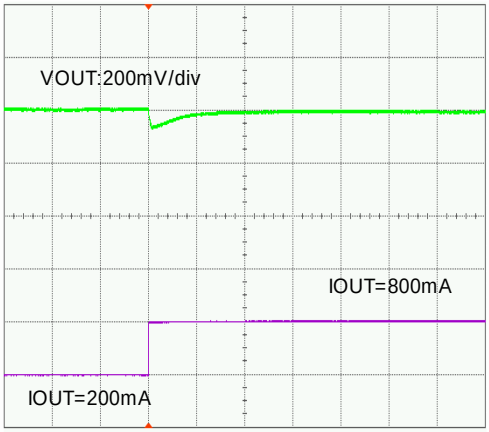
VIN=5.0V, VOUT=1.5V, MODE/SYNC=VIN (PWM control)
L=2.2μH (CDRH4D28), CIN=10μF (ceramic), CL=10μF (ceramic), Topr=25°C



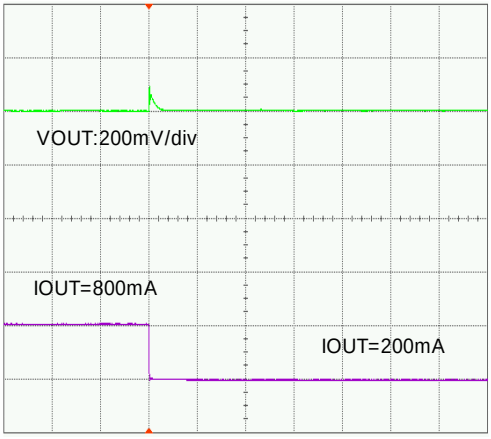
50μs / div



200μs / div

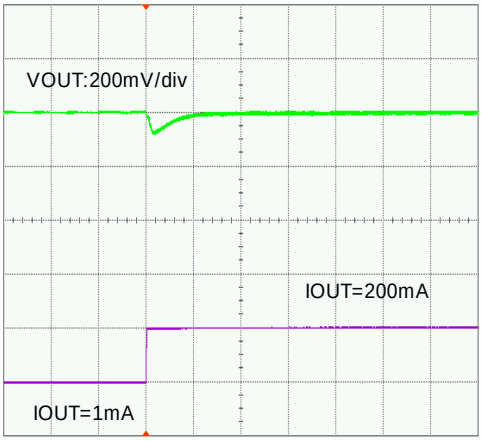


50μs / div

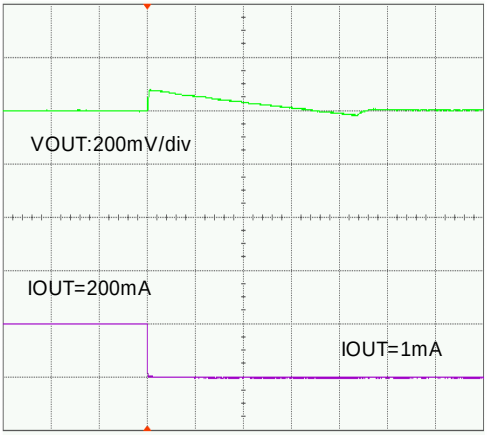


200μs / div

VIN=5.0V, VOUT=1.5V, MODE/SYNC=0V (PWM/PFM automatic switching control)
L=2.2μH (CDRH4D28C), CIN=10μF (ceramic), CL=10μF (ceramic), Topr=25°C



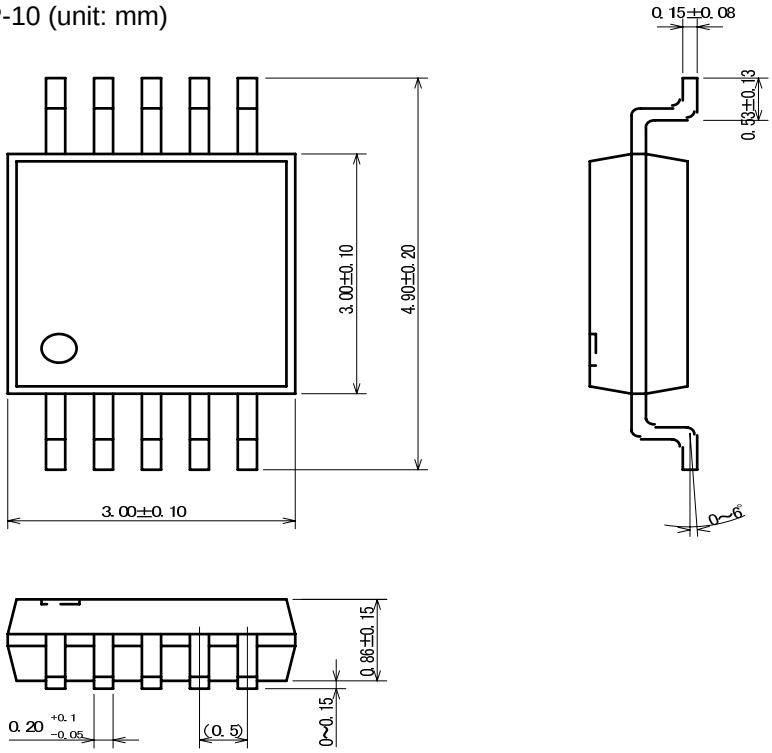
50μs / div



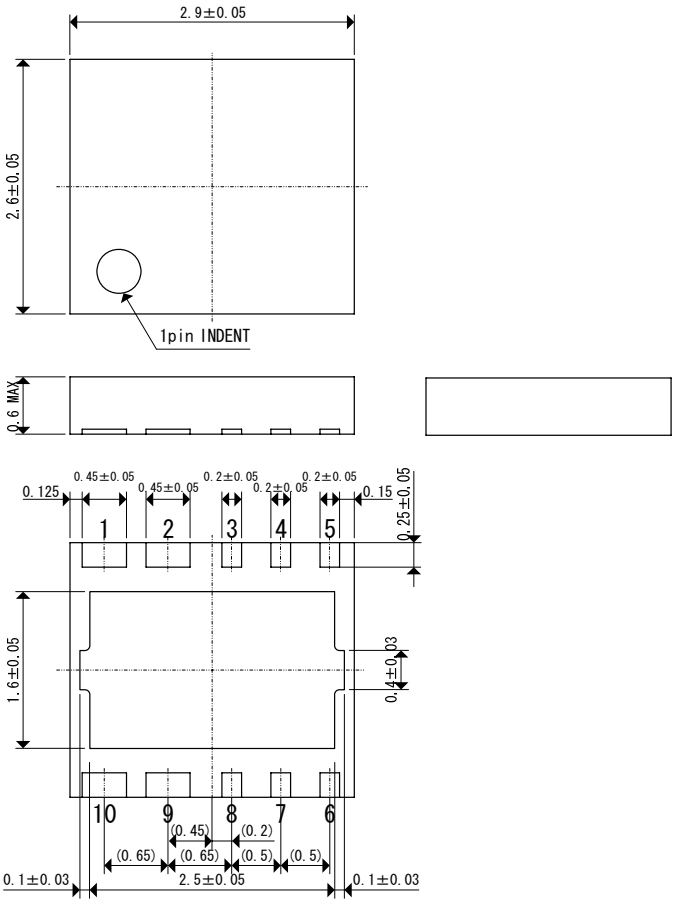
200μs / div

■PACKAGE INFORMATION

●MSOP-10 (unit: mm)

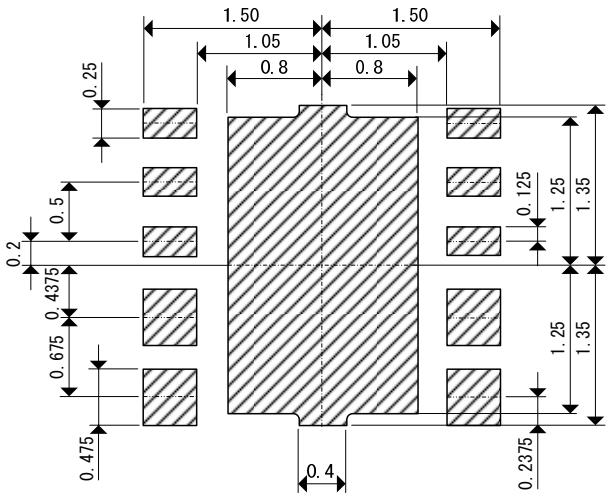


●USP-10B (unit: mm)

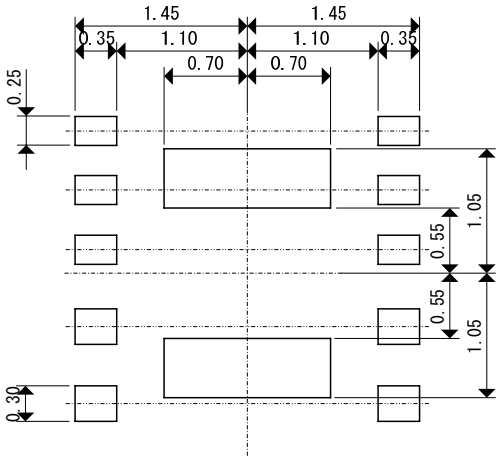


■PACKAGE INFORMATION (Continued)

●USP-10B Reference Pattern Layout

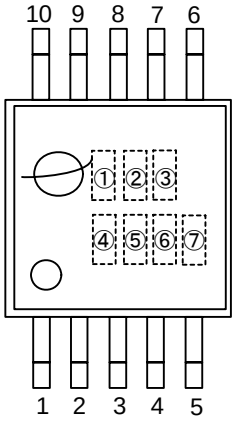


●USP-10B Reference Metal Mask Design



■MARKING RULE

●MSOP-10



MSOP-10
(TOP VIEW)

① represents products series

MARK	PRODUCT SERIES
0	XC9223xxxxAx
A	XC9224xxxxAx

② represents type of DC/DC converters

MARK	PRODUCT SERIES
B	XC9223/9224BxxxAx

③④ represents reference voltage

MARK		PRODUCT SERIES
③	④	
0	8	XC9223/9224x08xAx

⑤ represents oscillation frequency

MARK	OSCILLATION FREQUENCY	PRODUCT SERIES
1	1.0MHz	XC9223/9224xxx1Ax
2	2.0MHz	XC9223/9224xxx2Ax

⑥⑦ represents production lot number
01 to 09, 0A to 0Z, 10 to 19, 1A~ in order. (G, I, J, O, Q, W excluded)
Note: No character inversion used.

ex.)

MARKING		PRODUCTION LOT NUMBER
⑥	⑦	
0	3	03
1	A	1A

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