

Features

- Very high-speed: 45 ns
- Temperature ranges:
 - Automotive-A: -40 °C to +85 °C
 - Automotive-E: -40 °C to +125 °C
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62128DV30
- Ultra low standby power
 - Typical standby current: 1 μA
 - Maximum standby current: 4 μA
- Ultra low active power
 - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 32-pin small outline integrated circuit (SOIC), 32-pin thin small outline package (TSOP) Type I, and 32-pin STSOP packages

Functional Description

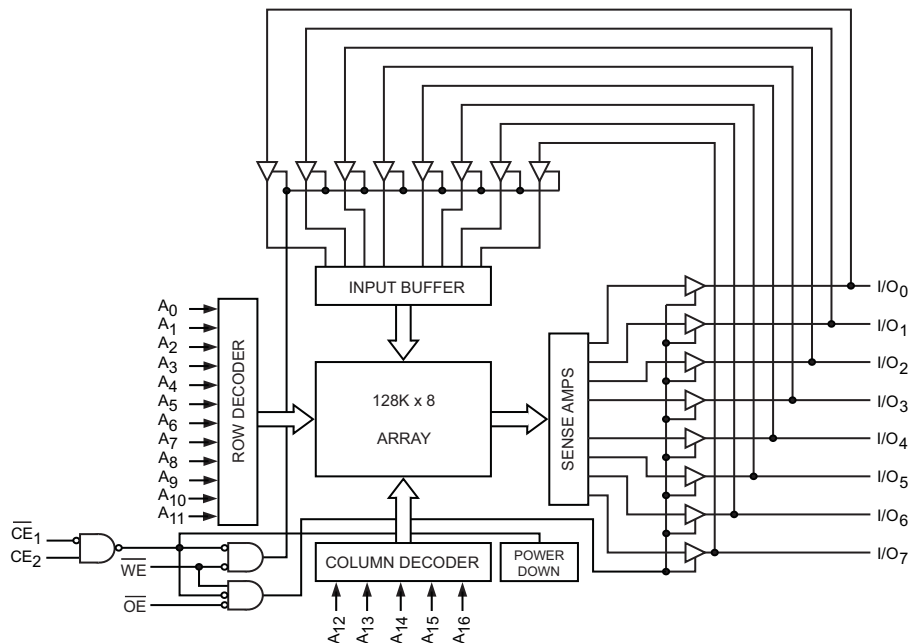
The CY62128EV30 is a high performance CMOS static RAM module organized as 128K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE}_1 HIGH or CE_2 LOW). The eight input and output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or a write operation is in progress (CE_1 LOW and CE_2 HIGH and WE LOW).

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (WE) inputs LOW. Data on the eight I/O pins is then written into the location specified on the Address pin (A₀ through A₁₆).

To read from the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related resources, [click here](#).

Logic Block Diagram



Contents

Pin Configuration	3	Ordering Information	13
Product Portfolio	3	Ordering Code Definitions	13
Pin Definitions	4	Package Diagrams	14
Maximum Ratings	5	Acronyms	17
Operating Range	5	Document Conventions	17
Electrical Characteristics	5	Units of Measure	17
Capacitance	6	Document History Page	18
Thermal Resistance	6	Sales, Solutions, and Legal Information	19
AC Test Loads and Waveforms	6	Worldwide Sales and Design Support	19
Data Retention Characteristics	7	Products	19
Data Retention Waveform	7	PSoC [®] Solutions	19
Switching Characteristics	8	Cypress Developer Community	19
Switching Waveforms	9	Technical Support	19
Truth Table	12		

Pin Configuration

Figure 1. 32-pin STSOP pinout [1]

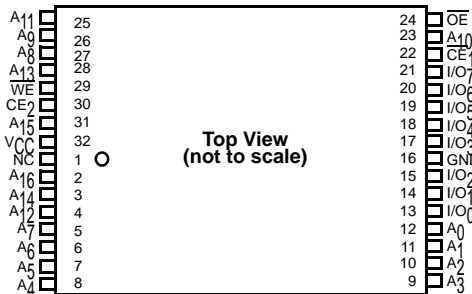


Figure 2. 32-pin TSOP I pinout [1]

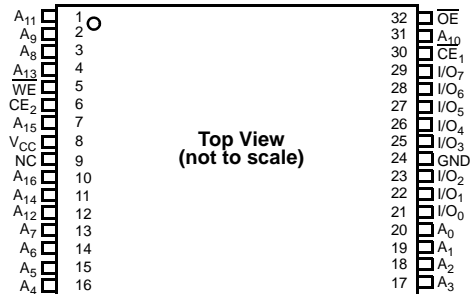
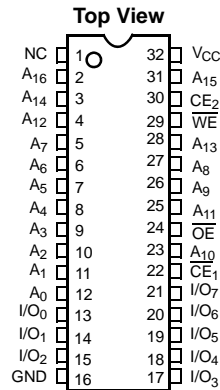


Figure 3. 32-pin SOIC pinout [1]



Product Portfolio

Product	Range	V _{CC} Range (V)		Speed (ns)	Power Dissipation						
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)		
					f = 1 MHz		f = f _{max}				
Min	Typ [2]	Max	Typ [2]	Max	Typ [2]	Max	Typ [2]	Max			
CY62128EV30LL	Automotive-A	2.2	3.0	3.6	45	1.3	2.0	11	16	1	4
CY62128EV30LL	Automotive-E	2.2	3.0	3.6	55	1.3	4.0	11	35	1	30

Notes

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Pin Definitions

I/O Type	Description
Input	A₀–A₁₆ . Address inputs
Input/output	I/O₀–I/O₇ . Data lines. Used as input or output lines depending on operation.
Input/control	WE . Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/control	CE₁ . Chip Enable 1, Active LOW.
Input/control	CE₂ . Chip Enable 2, Active HIGH.
Input/control	OE . Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When de-asserted HIGH, I/O pins are tri-stated, and act as input data pins.
Ground	GND . Ground for the device.
Power supply	V_{CC} . Power supply for the device.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential [3, 4]	-0.3 V to $V_{CC(max)}$ + 0.3 V
DC voltage applied to outputs in High Z state [3, 4]	-0.3 V to $V_{CC(max)}$ + 0.3 V
DC input voltage [3, 4]	-0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch up current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [5]
CY62128EV30LL	Automotive-A	-40 °C to +85 °C	2.2 V to 3.6 V
	Automotive-E	-40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Auto-A)			55 ns (Auto-E)			Unit
			Min	Typ [6]	Max	Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	$I_{OH} = -0.1 \text{ mA}, V_{CC} \leq 2.70 \text{ V}$	2.0	-	-	2.0	-	-	V
		$I_{OH} = -1.0 \text{ mA}, V_{CC} \geq 2.70 \text{ V}$	2.4	-	-	2.4	-	-	V
V_{OL}	Output LOW voltage	$I_{OL} = 0.1 \text{ mA}$	-	-	0.4	-	-	0.4	V
		$I_{OL} = 2.1 \text{ mA}, V_{CC} \geq 2.70 \text{ V}$	-	-	0.4	-	-	0.4	V
V_{IH}	Input HIGH voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$	1.8	-	$V_{CC} + 0.3 \text{ V}$	1.8	-	$V_{CC} + 0.3 \text{ V}$	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.2	-	$V_{CC} + 0.3 \text{ V}$	2.2	-	$V_{CC} + 0.3 \text{ V}$	V
V_{IL}	Input LOW voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$	-0.3	-	0.6	-0.3	-	0.6	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-0.3	-	0.8	-0.3	-	0.8	V
I_{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1	-	+1	-4	-	+4	μA
I_{OZ}	Output leakage current	$GND \leq V_O \leq V_{CC}$, output disabled	-1	-	+1	-4	-	+4	μA
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	-	11	16	-	11	35	mA
		$f = 1 \text{ MHz}$	-	1.3	2.0	-	1.3	4.0	mA
I_{SB1} [7]	Automatic CE power-down current — CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}, CE_2 \leq 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V}, f = f_{max}$ (address and data only), $f = 0$ (OE and WE), $V_{CC} = 3.60 \text{ V}$	-	1	4	-	1	35	μA
I_{SB2} [7]	Automatic CE power-down current — CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}, CE_2 \leq 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} < 0.2 \text{ V}, f = 0, V_{CC} = 3.60 \text{ V}$	-	1	4	-	1	30	μA

Notes

- $V_{IL(min)}$ = -2.0 V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.75 \text{ V}$ for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to $V_{CC(min)}$ and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25 \text{ }^\circ\text{C}$.
- Chip enables (\overline{CE}_1 and CE_2) must be at CMOS level to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.

Capacitance

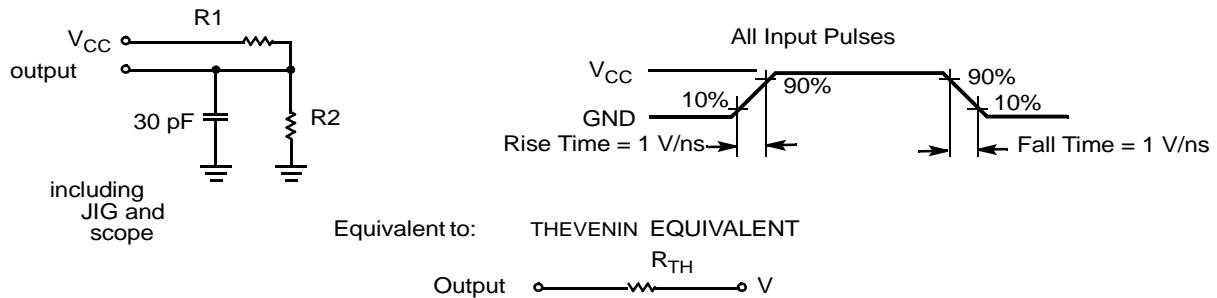
Parameter [8]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	32-pin TSOP I	32-pin SOIC	32-pin STSOP	Unit
Θ _{JA}	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	33.01	48.67	32.56	°C/W
Θ _{JC}	Thermal resistance (Junction to case)		3.42	25.86	3.59	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Note

8. Tested initially and after any design or process changes that may affect these parameters.

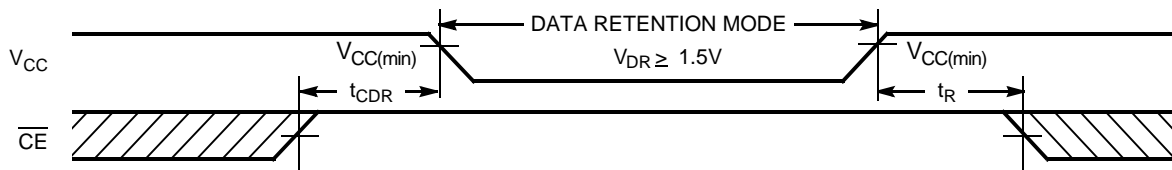
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[9]	Max	Unit	
V_{DR}	V_{CC} for data retention		1.5	–	–	V	
I_{CCDR} ^[10]	Data retention current	$V_{CC} = 1.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $\overline{CE}_2 \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	Automotive-A	–	–	3	μA
			Automotive-E	–	–	30	μA
t_{CDR} ^[11]	Chip deselect to data retention time		0	–	–	ns	
t_R ^[12]	Operation recovery time		CY62128EV30LL-45	45	–	–	ns
			CY62128EV30LL-55	55	–	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform^[13]



Notes

- 9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\text{ }^\circ\text{C}$.
- 10. Chip enables (\overline{CE}_1 and \overline{CE}_2) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- 11. Tested initially and after any design or process changes that may affect these parameters.
- 12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.
- 13. \overline{CE} is the logical combination of \overline{CE}_1 and \overline{CE}_2 . When \overline{CE}_1 is LOW and \overline{CE}_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW, \overline{CE} is HIGH.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns (Automotive-A)		55 ns (Automotive-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	45	–	55	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	–	25	ns
t_{LZOE}	\overline{OE} LOW to Low Z [16]	5	–	5	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z [16, 17]	–	18	–	20	ns
t_{LZCE}	\overline{CE} LOW to Low Z [16]	10	–	10	–	ns
t_{HZCE}	\overline{CE} HIGH to High Z [16, 17]	–	18	–	20	ns
t_{PU}	\overline{CE} LOW to Power-up	0	–	0	–	ns
t_{PD}	\overline{CE} HIGH to Power-down	–	45	–	55	ns
Write Cycle [18, 19]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	\overline{CE} LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data Hold from write end	0	–	0	–	ns
t_{HZWE}	\overline{WE} LOW to High Z [16, 17]	–	18	–	20	ns
t_{LZWE}	\overline{WE} HIGH to Low Z [16]	10	–	10	–	ns

Notes

14. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
15. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 4 on page 6.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the output enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of \overline{WE} , $CE = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write pulse width for Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to the sum of t_{SD} and t_{HZWE} .

Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

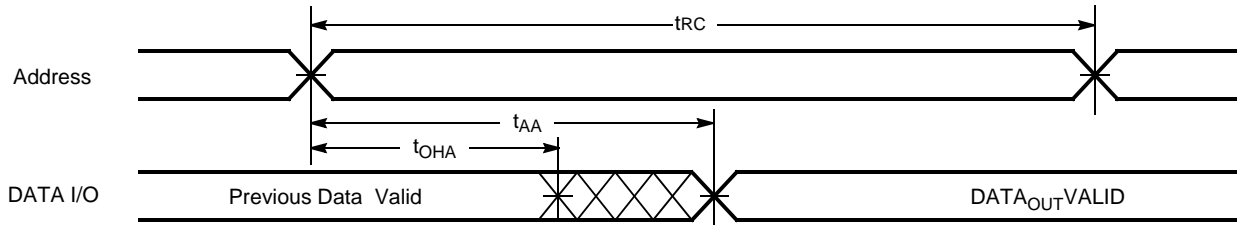
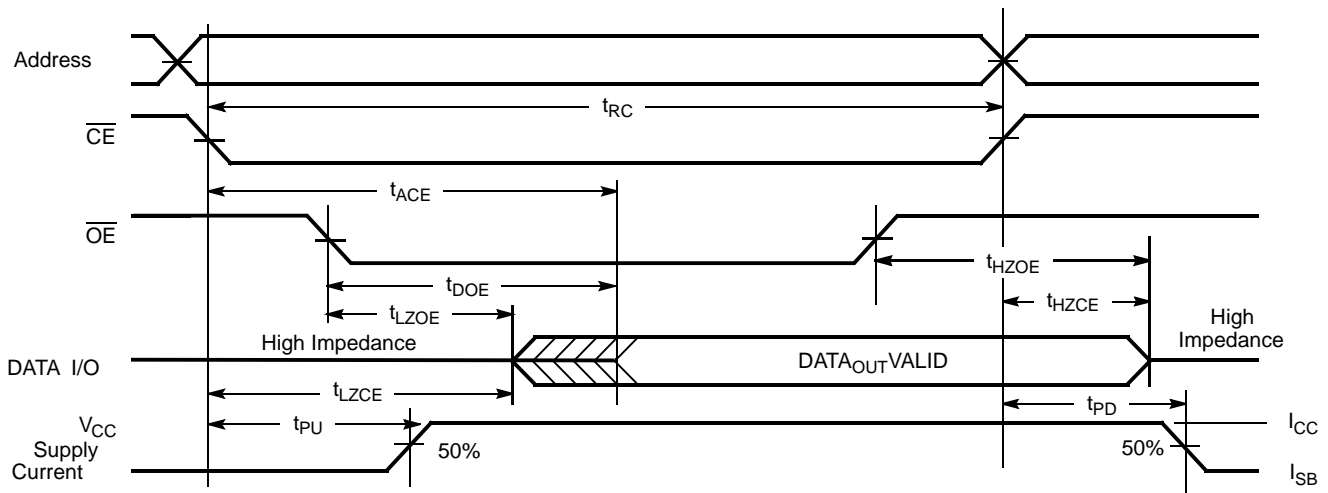


Figure 7. Read Cycle No. 2 (\overline{OE} Controlled) [21, 22, 23]



Notes

20. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.

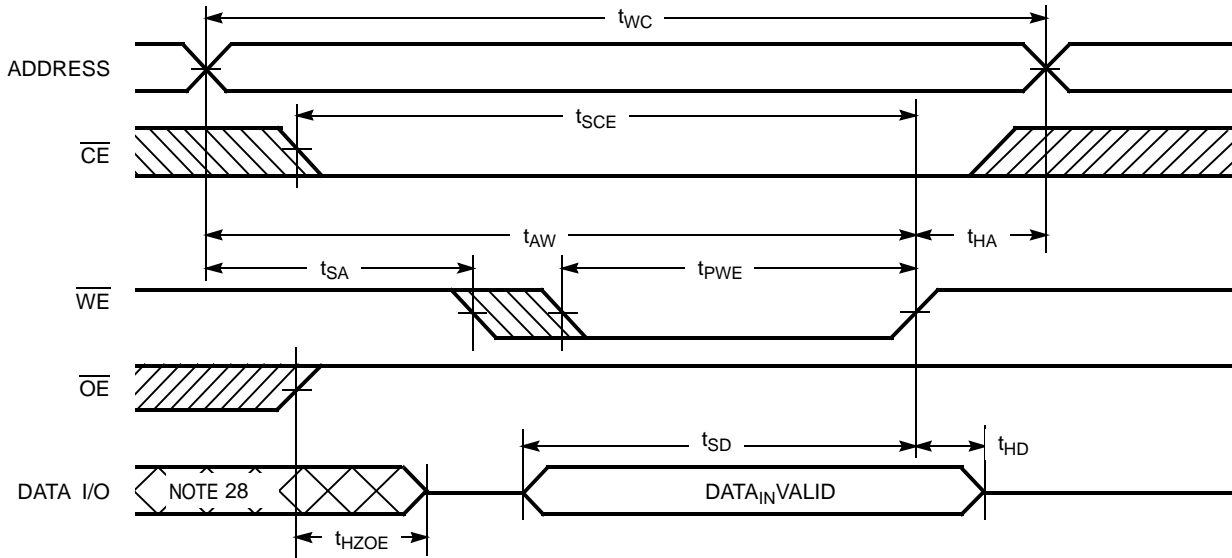
21. \overline{WE} is HIGH for read cycle.

22. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.

23. Address valid before or similar to \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (\overline{WE} Controlled) [24, 25, 26, 27]



Notes

- 24. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 25. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 26. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 27. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high impedance state.
- 28. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled) [29, 30, 31, 32]

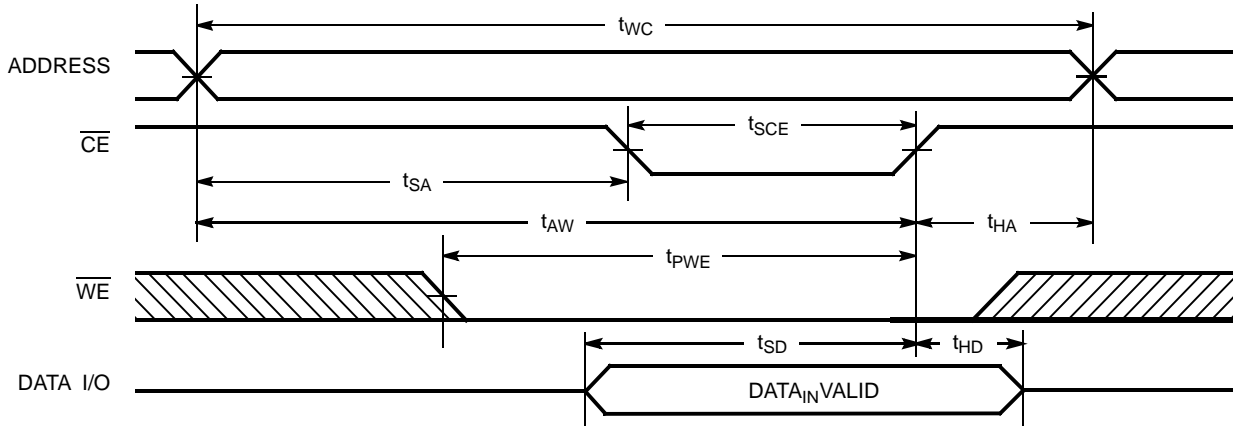
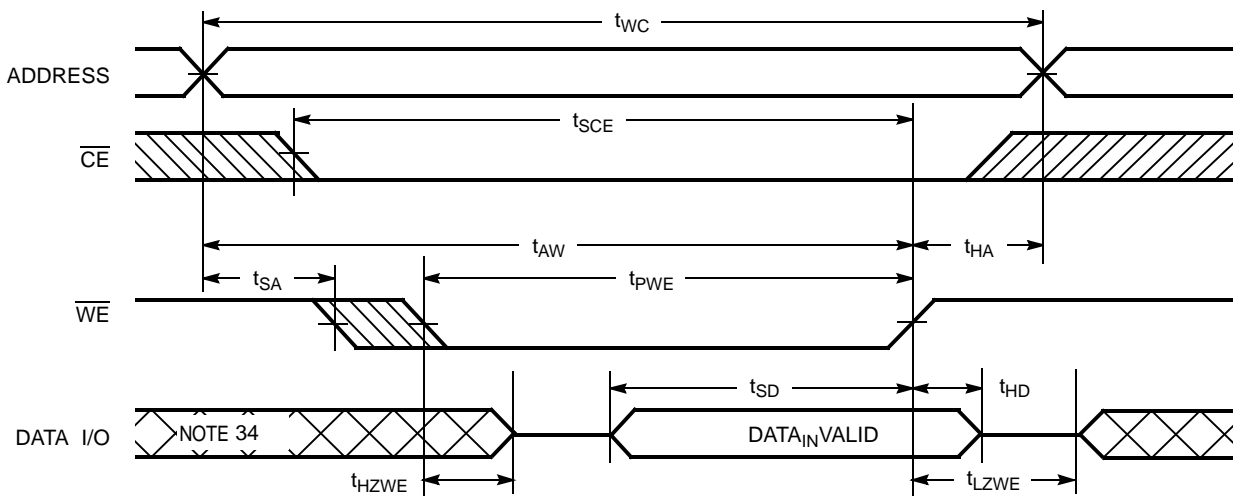


Figure 10. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [29, 32, 33]



Notes

- 29. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 30. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 31. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 32. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high impedance state.
- 33. The minimum write pulse width should be equal to the sum of t_{SD} and t_{HZWE} .
- 34. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

\overline{CE}_1	\overline{CE}_2	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode	Power
H	X ^[35]	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X ^[35]	L	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data out	Read	Active (I_{CC})
L	H	L	X	Data in	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Note

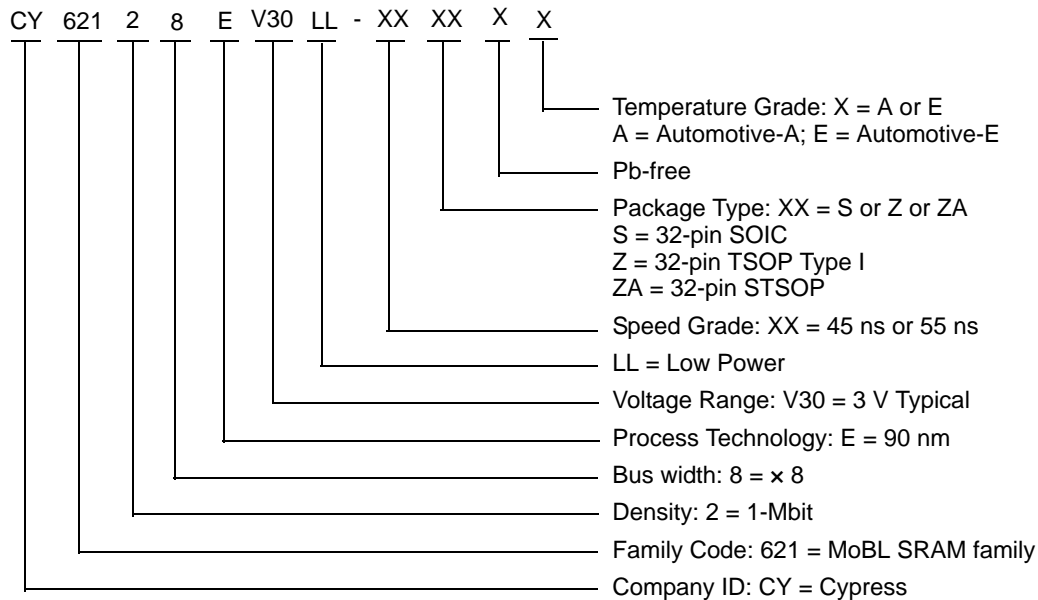
35. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128EV30LL-45SXA	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-A
	CY62128EV30LL-45ZXA	51-85056	32-pin TSOP Type I (Pb-free)	
	CY62128EV30LL-45ZAXA	51-85094	32-pin STSOP (Pb-free)	
55	CY62128EV30LL-55ZXE	51-85056	32-pin TSOP Type I (Pb-free)	Automotive-E
	CY62128EV30LL-55SXE	51-85081	32-pin 450-Mil SOIC (Pb-free)	

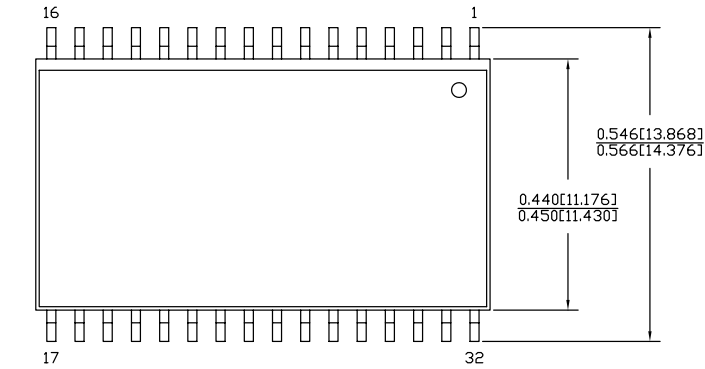
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

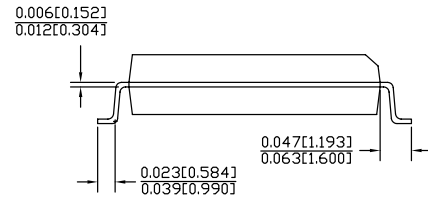
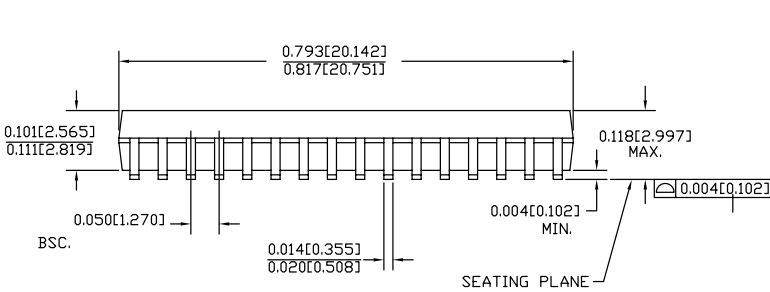
Figure 11. 32-pin SOIC (450 Mil) S32.45/SZ32.45 Package Outline, 51-85081



DIMENSIONS IN INCHES[MM] MIN. MAX.

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

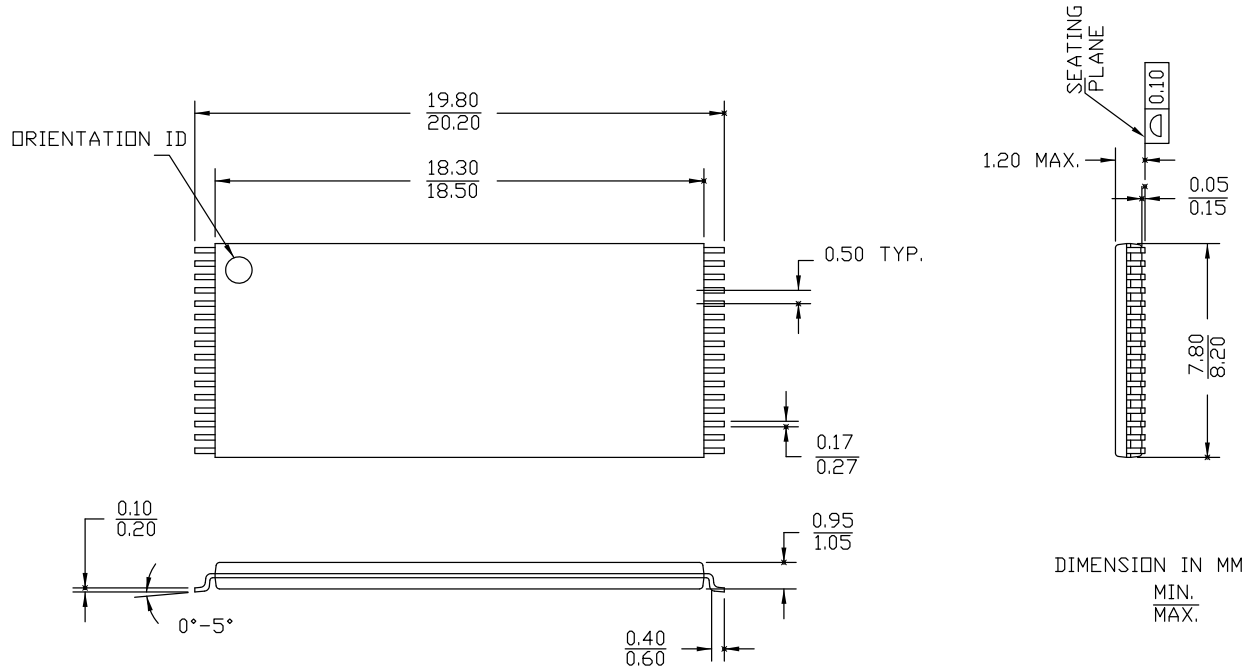
PART #	
S32.45	STANDARD PKG.
SZ32.45	LEAD FREE PKG.



51-85081 *E

Package Diagrams (continued)

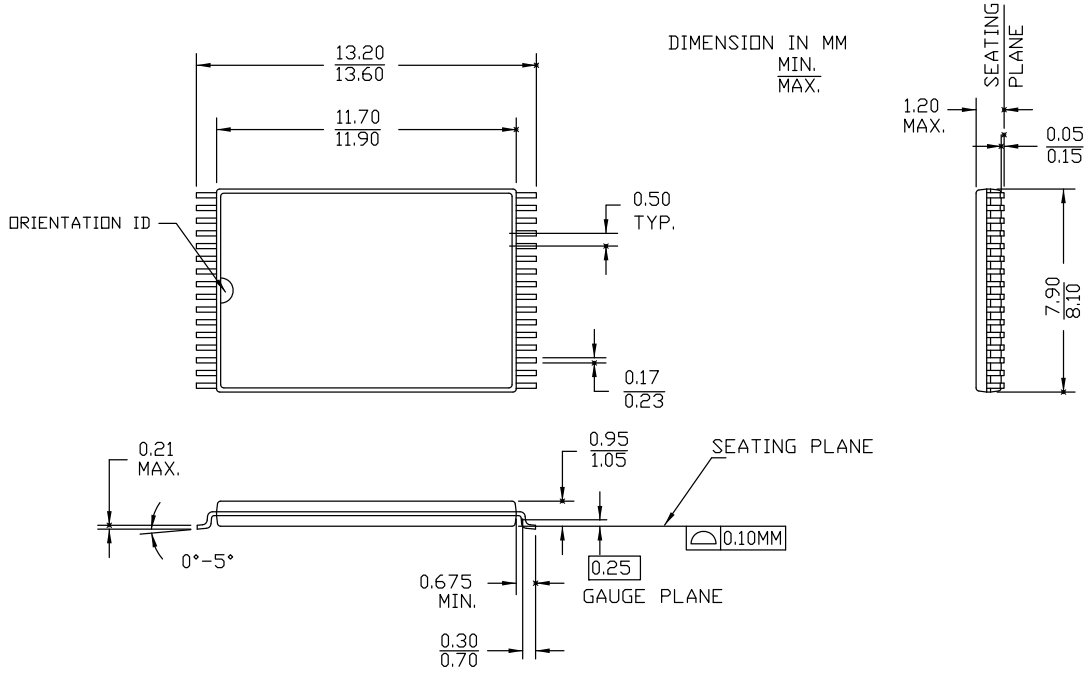
Figure 12. 32-pin TSOP I (8 x 20 x 1.0 mm) Z32R Package Outline, 51-85056



51-85056 *G

Package Diagrams (continued)

Figure 13. 32-pin Small TSOP (8 × 13.4 × 1.2 mm) ZA32 Package Outline, 51-85094



51-85094 *G

Acronyms

Acronym	Description
\overline{CE}	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
\overline{OE}	Output Enable
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
STSOP	Small Thin Small Outline Package
TSOP	Thin Small Outline Package
\overline{WE}	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62128EV30 MoBL [®] Automotive, 1-Mbit (128 K x 8) Static RAM				
Document Number: 001-65528				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	3115909	01/06/2011	RAME	New data sheet for Automotive SRAM parts. Created separate data sheet for Automotive SRAM parts from Document no. 38-05579 Rev. *H
*A	3288690	06/21/2011	RAME	Removed the Note "For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at http://www.cypress.com website." and its reference in Functional Description . Updated Electrical Characteristics (Test Conditions of I _{SB1} and I _{SB2} parameters). Updated Package Diagrams . Updated to new template.
*B	3543173	03/06/2012	TAVA	Updated Electrical Characteristics . Updated Switching Waveforms . Updated Package Diagrams .
*C	4582964	11/29/2014	VINI	Updated Maximum Ratings : Referred Notes 3, 4 in "Supply voltage to ground potential". Updated Switching Characteristics : Added Note 19 and referred the same note in "Write Cycle". Updated Switching Waveforms : Added Note 33 and referred the same note in Figure 10 . Updated Package Diagrams : spec 51-85081 – Changed revision from *D to *E. spec 51-85056 – Changed revision from *F to *G. spec 51-85094 – Changed revision from *F to *G. Updated to new template.
*D	4700035	03/25/2015	MEMJ	No technical updates. Completing Sunset Review.
*E	4725832	04/15/2015	PSR	Updated Functional Description : Added "For a complete list of related resources, click here ." at the end. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

psoc.cypress.com/solutions
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2011-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

单击下面可查看定价，库存，交付和生命周期等信息

[>>CYPRESS\(赛普拉斯\)](#)