SPIDER

SPI Driver for Enhanced Relay Control

TLE7237SL

SPI Driver for Enhanced Relay Control

Data Sheet

Rev. 1.1, 2011-04-05

Automotive Power

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AEC Qualified   RoHS

1 Overview

Features

- 8 bit SPI for diagnostics and control, providing daisy chain capability
- Very wide range for digital supply voltage
- Three configurable input pins offer complete flexibility for PWM operation
- Stable behavior at under voltage
- Green Product (RoHS compliant)
- AEC Qualified

PG-SSOP-24-5

Description

The TLE7237SL is an eight channel high-side and low-side power switch in PG-SSOP-24-5 package providing embedded protective functions. It is especially designed for standard relays and LEDs in automotive applications.

The output stages incorporate two low-side, four high-side and two auto configuring high-side or low-side switches.

A serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the load. For direct control, there are three input pins available.

The power transistors are built by N-channel power MOSFETs. The device is monolithically integrated in Smart Power Technology.

Type	Package	Marking
TLE7237SL	PG-SSOP-24-5	TLE7237SL

Table 1 Product Summary

Operating range power supply voltage	V_{bb}	5.5 … 28 V
Digital supply voltage	V_{DD}	3.0 … 5.5 V
Typical On-State resistance at 25 °C	$R_{DS(ON)}$	
high-side: 2 channels (Relay)		0.9 Ω
high-side: 2 channels (Generic, LED)		1.6 Ω
auto configuring: 2 channels (Relay, Supplies)		0.9 Ω
low-side: 2 channels (Relay)		0.9 Ω
Nominal load current (all channels active)	$I_{L(nom, min)}$	
Relay		260 mA
LED, Generic		130 mA
Over load switch off threshold	$I_{DS(OVL, min)}$	500 mA
Output leakage current per channel at 25 °C	$I_{DS(OFF, max)}$	1 µA
Drain to source clamping voltage	$V_{DS(CL, min)}$	41 V
Source to ground clamping voltage	$V_{bb(CL, max)}$	-40 V
SPI clock frequency	$f_{SCLK(max)}$	5 MHz

Protective Functions

- Over load and short circuit protection
- Thermal shutdown
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Latched diagnostic information via SPI
- Open load detection in OFF-state
- Over load detection in ON-state
- Over temperature

Applications

- Especially designed for driving relays and LEDs in automotive applications
- All types of resistive and inductive loads
- Suitable to switch 5 V power supply lines by auto configuring channels

Detailed Description

The TLE7237SL is an eight channel high-side and low-side relay switch providing embedded protective functions. The output stages incorporate two low-side switches (0.9 Ω per channel), four high-side switches (two channels with 0.9 Ω and two channels with 1.6 Ω) and two auto-configuring high-side or low-side switches (0.9 Ω per channel). The auto-configuring switches can be utilized in high-side or low-side configuration just by connecting the load accordingly. They are also suitable to switch a 5 V supply line in high-side configuration. Protective and diagnostic functions adjust automatically to the chosen configuration.

The 8 bit serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the loads. The SPI interface provides daisy chain capability in order to assemble multiple devices in one SPI chain by using the same number of micro-controller pins.

Furthermore, the TLE7237SL is equipped with three input pins that can be individually routed to the output control of each channel thus offering complete flexibility in design and PCB-layout. The input multiplexer is controlled via SPI.

The device provides full diagnosis of the load via open load, over load and short circuit detection. SPI diagnosis flags indicate latched fault conditions that may have occurred.

Each output stage is protected against short circuit. In case of over load, the affected channel switches off. There are temperature sensors available for each channel to protect the device against over temperature.

The device protects itself with a built in reverse polarity protection which prohibits intrinsic current flow through the logic during reverse polarity. However the output stages still incorporate a reverse diode where current can flow through during reverse polarity.

The power transistors are built by N-channel power MOSFETs. The inputs are ground referenced CMOS compatible. The device is monolithically integrated in Smart Power Technology.

2 Block Diagram

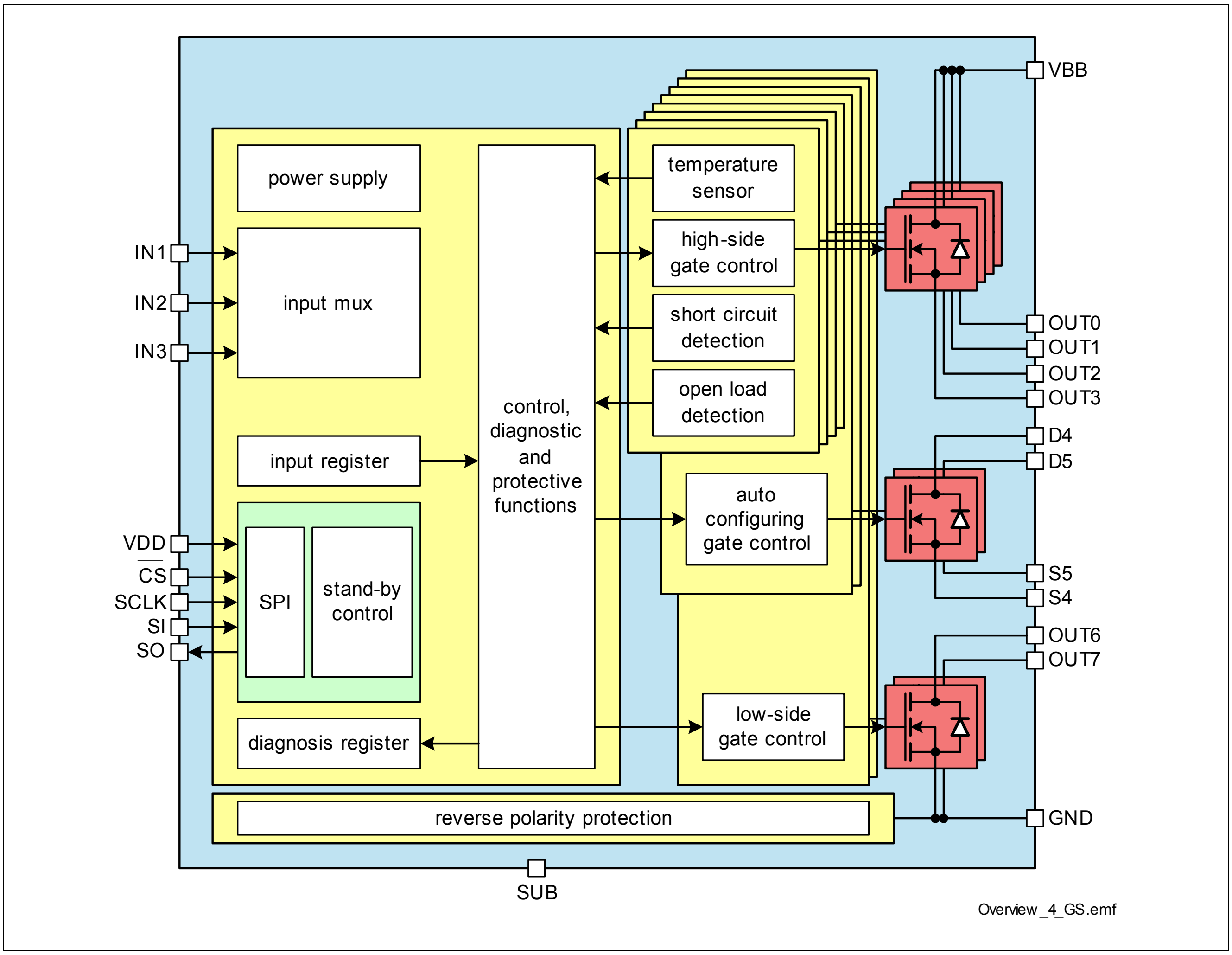

Figure 1 Block Diagram

2.1 Terms

Figure 2 shows all terms used in this data sheet.

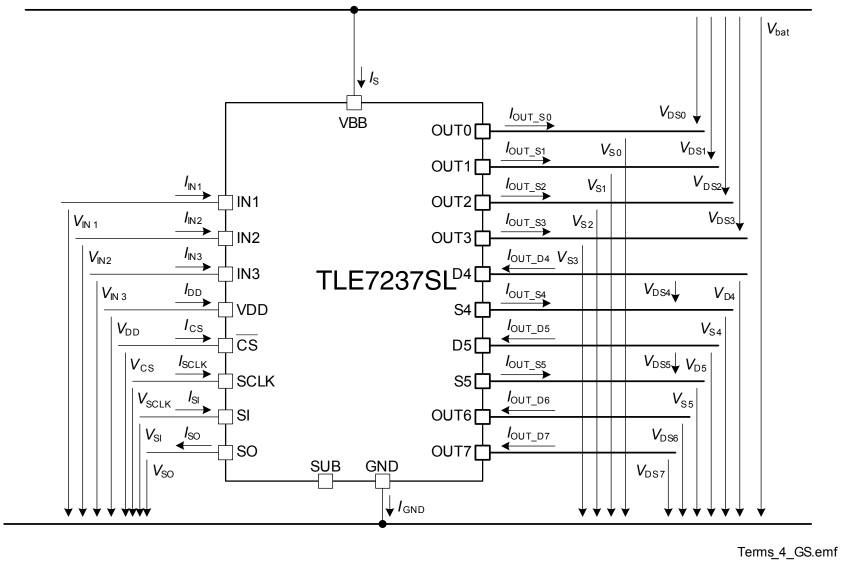

Figure 2 Terms

In all tables of the electrical characteristics is valid:

Channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} … V_{DS7}). In order to make the description of output currents easier, the load current I_{Out} is equivalent to the drain current I_{OUT_D} in low-side configuration and the source current I_{OUT_S} in high-side configuration.

All SPI register bits are marked as follows: `ADDR.PARAMETER (e.g. ICR01.INX1)`. In SPI register description, the values in bold letters (e.g. **0**) are default values.

3 Pin Configuration

3.1 Pin Assignment

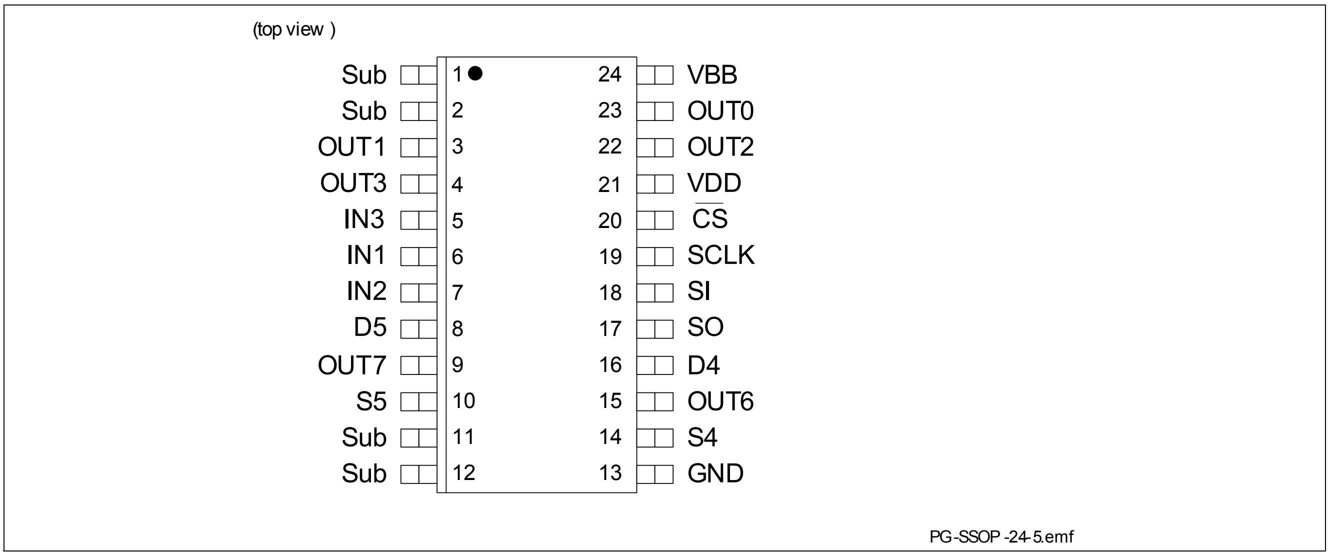

Figure 3 Pin Configuration PG SSOP24-5

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply			
21	VDD	-	Digital power supply
24	VBB	-	Power supply
13	GND	-	Digital, analog and power ground
1,2,11,12	SUB	-	Substrate pins for thermal connection. **To enable reverse polarity protection these pins must be floating**
Power Stages			
23	OUT0	O	Source of high side power transistor channel 0
3	OUT1	O	Source of high side power transistor channel 1
22	OUT2	O	Source of high side power transistor channel 2
4	OUT3	O	Source of high side power transistor channel 3
16	D4	O	Drain of auto configuring power transistor 4
14	S4	O	Source of auto configuring power transistor 4
8	D5	O	Drain of auto configuring power transistor 5
10	S5	O	Source of auto configuring power transistor 5
15	OUT6	O	Drain of low side power transistor channel 6
9	OUT7	O	Drain of low side power transistor channel 7
Inputs			
6	IN1	I	Input multiplexer input 1 pin (pull down)
7	IN2	I	Input multiplexer input 2 pin (pull down)
5	IN3	I	Input multiplexer input 3 pin (pull down)

Pin	Symbol	I/O	Function
SPI			
20	$\overline{CS}$	I	SPI Chip select (pull up)
19	SCLK	I	Serial clock
18	SI	I	Serial data in
17	SO	O	Serial data out

4 Electrical Characteristics

4.1 Absolute Maximum Ratings [1)]

Stresses above the ones listed here may affect device reliability or may cause permanent damage to the device. The values below are not considering combinations of different maximum conditions at one time

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Absolute Maximum Ratings[1)]

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
Power Supply						
4.1.1	Power supply voltage	V_{bb}	-40	40	V	-40V max. 2 minutes
4.1.2	Digital supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.3	Power supply voltage for short circuit protection (single pulse)	$V_{bat(SC)}$	0	28	V	–
Power Stages						
4.1.4	Load current	I_L			A	–
	channel 0, 1, 4, 5, 6, 7		-0.5	0.5		
	channel 2, 3		-0.25	0.25		
4.1.5	Voltage at power transistor	V_{DS}	–	41	V	–
4.1.6	Power transistor's source voltage	V_{Out_S}	-16	–	V	–
4.1.7	Power transistor's drain voltage	V_{Out_D}	–	41	V	–
4.1.8	Max. energy dissipation one channel single pulse for ch. 0, 1, 4, 5, 6, 7	E_{AS}			mJ	2)
			–	65		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.35 A
			–	50		$T_{j(0)}$ = 150 °C $I_{D(0)}$= 0.250 A
4.1.9	Maximum energy dissipation one channel repetitive pulses for ch. 0, 1, 4, 5, 6, 7	E_{AR}			mJ	2)
	$1 \cdot 10^4$ cycles		–	18		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.250 A
	$1 \cdot 10^6$ cycles		–	13		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.220 A
4.1.10	Max. energy dissipation one channel single pulse for ch. 2,3	E_{AS}			mJ	2)
			–	50		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.250 A
			–	30		$T_{j(0)}$ = 150 °C $I_{D(0)}$= 0.250 A

1) not subject to production test

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
Absolute Maximum Ratings[1)]						
4.1.11	Maximum energy dissipation one channel repetitive pulses for ch. 2,3	E_{AR}			mJ	2)
	$1 \cdot 10^4$ cycles		–	12		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.180 A
	$1 \cdot 10^6$ cycles		–	11		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.180 A
Logic Pins						
4.1.12	Voltage at input pins	V_{IN}	-0.3	V_{DD} + 0.3	V	3)
4.1.13	Voltage at chip select pin	V_{CS}	-0.3	V_{DD} + 0.3	V	3)
4.1.14	Voltage at serial clock pin	V_{SCLK}	-0.3	V_{DD} + 0.3	V	3)
4.1.15	Voltage at serial input pin	V_{SI}	-0.3	V_{DD} + 0.3	V	3)
4.1.16	Voltage at serial output pin	V_{SO}	-0.3	V_{DD} + 0.3	V	3)
Temperatures						
4.1.17	Junction Temperature	T_j	-40	150	°C	–
4.1.18	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.19	ESD susceptibility on all pins	V_{ESD}	-2	2	kV	HBM[4)]

1) not subject to production test
2) Pulse shape represents inductive switch off: $I_L(t) = I_L(0) * (1 - t / t_{pulse})$; $0 < t < t_{pulse}$
3) V_{DD} + 0.3 V < 5.5 V
4) ESD susceptibility, HBM according to EIA/JESD 22-A114

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range for Nominal Operation	$V_{bb(nom)}$	9	16	V	–
4.2.2	upper Supply Voltage Range for Extended Operation	$V_{bb(ext),up}$	16	28	V	Parameter Deviations possible
4.2.3	lower Supply Voltage Range for Extended Operation	$V_{bb(ext),low}$	5.5	9	V	Parameter Deviations possible
4.2.4	Junction Temperature	T_j	-40	150	°C	–
4.2.5	Digital supply turn-ON time	$t_{DD(ON)}$	15	–	µs	V_{DD} = 0V to 5V (linear)

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Thermal Resistance[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case, bottom	$R_{thJC,back}$	–	–	25	K/W	2)
4.3.2	Junction to Case, top	$R_{thJC,top}$	–	–	25	K/W	2)
4.3.3	Junction to Pin (1,2,11 or 12)	R_{thJPin}	–	–	17	K/W	2)
4.3.4	Junction to Ambient (1s0p, min. footprint)	$R_{thJA,min}$	–	90	–	K/W	3)
4.3.5	Junction to Ambient (1s0p+300mm^{2}Cu)	$R_{thJA,300}$	–	70	–	K/W	4)
4.3.6	Junction to Ambient (1s0p+600mm^{2}Cu)	$R_{thJA,600}$	–	65	–	K/W	5)
4.3.7	Junction to Ambient (2s2p)	$R_{thJA,2s2p}$	–	55	–	K/W	6)

1) Not subject to production test
2) Specified R_{thJSP} value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature). T_a = 85 °C. Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
3) Specified R_{thJA} value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with minimal footprint copper area and 70 µm thickness. T_a = 85 °C, Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
4) Specified R_{thJA} value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 300mm^2 and 70 µm thickness. T_a = 85 °C, Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
5) Specified R_{thJA} value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm^2 and 70 µm thickness. T_a = 85 °C, Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
6) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). T_a = 85 °C, Ch1 to Ch8 are dissipating 1 W power (0.125 W each).

5 Power Supply

The TLE7237SL is supplied by two supply voltages V_{bb} and V_{DD}. The V_{bb} supply line is connected to a battery feed and used by the power switches and by an integrated power supply for the register banks. There is an under voltage reset function implemented for the V_{bb} power supply, which is triggered if V_{bb} is below the undervoltage threshold. After start-up of the power supply, all SPI registers are reset to their default values and the device is in sleep mode (standby). Sending the SPI command CMD.WAKE = 1 switches the device to operation mode (ON), while a command CMD.STB = 1 send the device to sleep mode (standby) again. Please note that the device needs the time $t_{wu(Sleep)}$ to initialize itself. No SPI command should be send after changing the power state via CMD.WAKE = 1 before this time is elapsed. A SPI frame send during $t_{wu(Sleep)}$ could be ignored.

The V_{DD} supply line is used to power the circuitry related to the SPI shift register and for driving the SO line. As a result, the daisy chain function is available as soon as V_{DD} is provided in the specified range independent of V_{bb}.

A capacitor between pins V_{DD} and GND is recommended (especially in case of EMI disturbances).

Please see **Figure 14 "Application Diagram" on Page 34** for details.

The device provides a sleep mode (stand by) to minimize current consumption, which also resets the register banks. It is entered and left by dedicated SPI commands or by turning off the VDD supply.

The following table shows the operation modes depending on V_{bb}, V_{DD} .

Operation Modes				
VBB	0 V	0 V	12 V	12 V
VDD	0 V	5 V	0 V	5 V
Switches operating	-	-	✓	✓
SPI & daisy-chain	-	✓	-	✓
Register Banks	reset	reset	✓	✓
Diagnostic functions	-	-	✓	✓

5.1 Reset

There are several reset trigger implemented in the device. A reset switches off all channels and sets the registers to default values. After any kind of reset, the transmission error flag (TER) is set and the device is in sleep mode.

Under Voltage Reset:

During this device condition a read on SPI delivers the Standard Diagnostic Frame with a TER flag, if V_{DD} is above the under voltage threshold already, if not SPI is not working.
This under voltage reset is released when V_{DD} and V_{bb} supply voltage levels are above under voltage threshold.

Reset Command: There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as `CMD.RST` = 1, a reset is triggered.

5.2 Electrical Characteristics

Unless otherwise specified:
V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Power Supply V_{bb}							
5.2.1	Supply Voltage Range for Nominal Operation	$V_{bb(nom)}$	9		16	V	–
5.2.2	upper Supply Voltage Range for Extended Operation	$V_{bb(ext),up}$	16		28	V	Parameter Deviations possible
5.2.3	lower Supply Voltage Range for Extended Operation	$V_{bb(ext),low}$	5.5		9	V	R_L = 80 Ω V_{DS} < 1.5 V Parameter Deviations possible
5.2.4	Under voltage reset threshold	$V_{bb(UV)}$	–	–	5.5	V	V_{DD}= 0V
5.2.5	Operating current drawn from V_{bb}	$I_{S(ON)}$	–	–	15	mA	1) V_{bb} = 16 V
			–	–	12	mA	V_{bb} = 16 V all diagnosis off
5.2.6	Sleep mode operating current with disconnected loads (stand by)	$I_{S(Sleep)}$				µA	V_{bb} = 16 V AWK= 0
			–	–	10		T_j = 25 °C1)
			–	–	13		T_j = 85 °C 1)
			–	–	20		T_j = 150 °C
Digital Power Supply V_{DD}							
5.2.7	Logic supply voltage	V_{DD}	3.0	–	5.5	V	
5.2.8	Under voltage reset threshold	$V_{DD(PO)}$	–	–	3.0	V	
5.2.9	Logic supply current	$I_{DD(ON)}$	–	–	0.4	mA	f_{SCLK} = 0 Hz AWK= 1 V_{CS} = 0V
5.2.10	Logic supply current during VBB dropout	$I_{DD(DO)}$	–	3	5	mA	1) f_{SCLK} = 0 Hz V_{bb} < $V_{bb(UV)}$ AWK= 1 V_{CS} = 0V
5.2.11	Logic supply sleep mode current	$I_{DD(Sleep)}$				µA	V_{CS} = V_{DD} AWK = 0
			–	–	20		T_j = 25 °C1)
			–	–	20		T_j = 85 °C 1)
			–	–	40		T_j = 150 °C
Timings							
5.2.12	Sleep mode wake-up time	$t_{wu(Sleep)}$	–	–	200	µs	1)
5.2.13	V_{bb} under voltage reset delay time	$t_{bb(UVR)}$	–	–	1	µs	1)
5.2.14	V_{DD} under voltage reset delay time	$t_{DD(UVR)}$	–	–	1	µs	1)

1) Not subject to production test, specified by design.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected at V_{bb} = 13.5 V, V_{DD} = 5.0 V, T_j = 25 °C.

6 Power Stages

The TLE7237SL is an eight channel high-side and low-side relay switch. The power stages are built by N-channel vertical power MOSFET transistors. The gates of the high-side switches are controlled by charge pumps.

6.1 Input Circuit

There are three input pins available at TLE7237SL, which can be configured to be used for control of the output stages. The INXn parameter of the input configuration register provide following possibilities:

- channel is switched off
- channel is switched according to signal level at input pin IN1
- channel is switched according to signal level at input pin IN2or IN3
- channel is switched on

Figure 4 shows the input circuit of TLE7237SL.

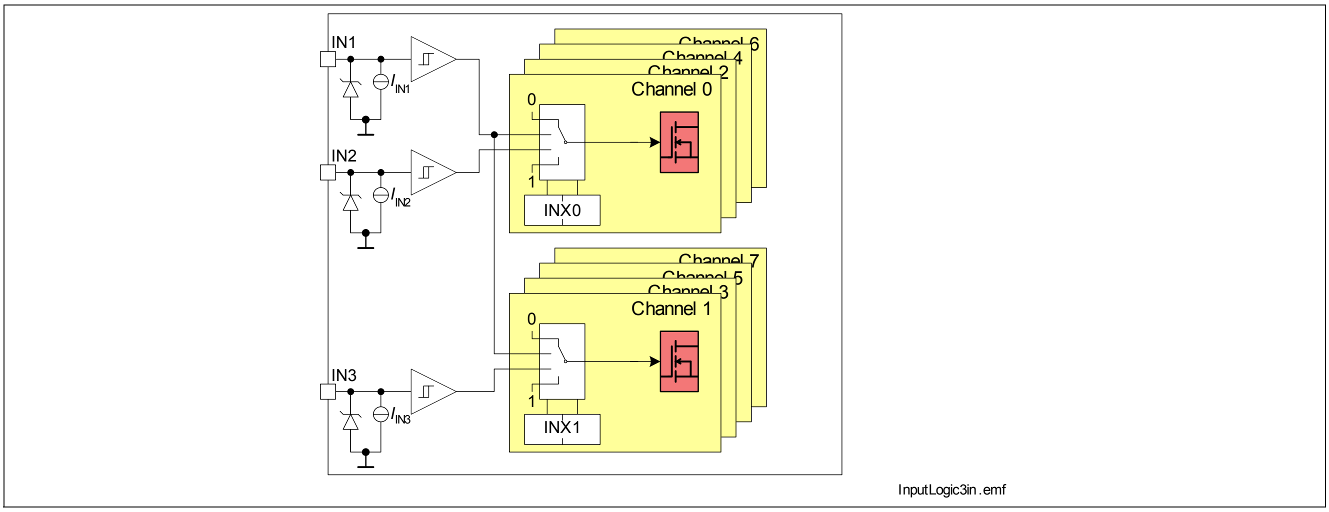

Figure 4 Input Multiplexer

The current sink to ground ensures that the channels switch off in case of open input pin. The zener diode protects the input circuit against ESD pulses.

6.2 Channels 4 and 5

The TLE7237SL provides two auto-configuring high-side or low-side switches (channels 4 and 5). They adjust the diagnostic and protective functions according their potentials at drain and source automatically.

In high-side configuration, the load is connected between ground and source of the power transistors (S4 or S5). The drain of the power transistors (D4 and D5) can be connected to any potential between GND-pin potential and VBB-pin potential. When the drain is connected to VBB, the channel behave like the other high side channels. The drain can also be connected to a 5 V power supply and the source pin will be utilized as switched 5 V supply line.

In low-side configuration, the source of the power transistors are to be connected to GND.

The configuration can be chosen for each of these channels individually, so it is feasible to connect one channel in low-side and the other in high-side configuration.

6.3 Inductive Output Clamp

When switching off inductive loads with low-side switches, the potential at pin OUT rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. For the high-side channels, the potential at pin OUT drops below ground potential to $V_{S(CL)}$. The voltage clamping is necessary to prevent destruction of the device, see **Figure 5** for details. Nevertheless, the maximum allowed load inductance is limited by the max. clamping energy E_{AR} see electrical characteristics **"E_{AR}" on Page 10**.

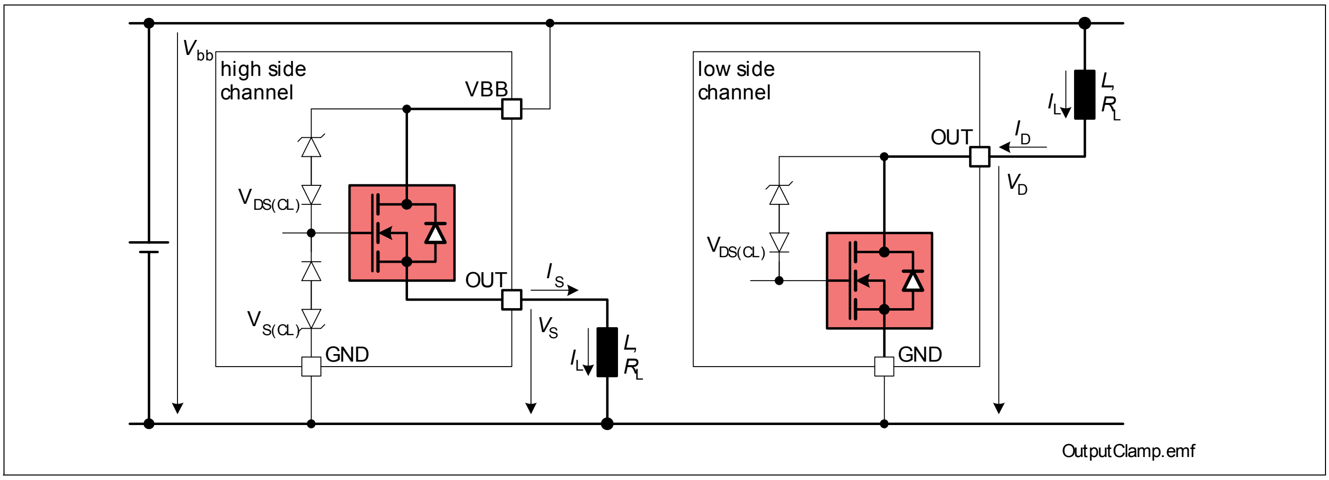

Figure 5 Output Clamp Implementation

Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the TLE7237SL. This energy can be calculated with following equations:

$$E = V_{DS(CL)} \cdot \left[\frac{V_{bb} - V_{DS(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_{bb} - V_{DS(CL)}}\right) + I_L\right] \cdot \frac{L}{R_L} \quad \textbf{Low-side} \quad (1)$$

$$E = (V_{bb} - V_{S(CL)}) \cdot \left[\frac{V_{S(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_{S(CL)}}\right) + I_L\right] \cdot \frac{L}{R_L} \quad \textbf{High-side} \quad (2)$$

These equations simplify under the assumption of $R_L = 0$:

$$E = \frac{1}{2} L I_L^2 \cdot \left(1 - \frac{V_{bb}}{V_{bb} - V_{DS(CL)}}\right) \quad \textbf{Low-side} \quad (3)$$

$$E = \frac{1}{2} L I_L^2 \cdot \left(1 - \frac{V_{bb}}{V_{S(CL)}}\right) \quad \textbf{High-side} \quad (4)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component.

6.4 Timing Diagrams

The power transistors are switched on and off with a dedicated slope via the `INX` bits of the serial peripheral interface (SPI). The switching times t_{ON} and t_{OFF} are designed equally.

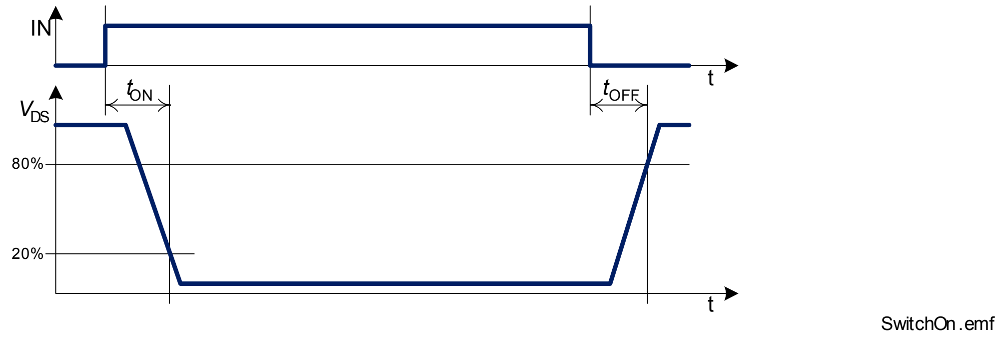

Figure 6 Switching a Resistive Load

In input mode, a high signal at the input pin is equivalent to a SPI ON command and a low signal to SPI OFF command respectively. Please refer to **Section 9.3** for details on SPI protocol.

6.5 Electrical Characteristics

Unless otherwise specified: V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C
typical values: V_{DD} = 5.0 V, V_{BAT} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Output Characteristics							
6.5.1	On-State resistance	$R_{DS(ON)}$				Ω	
	channel 0, 1, 4, 5, 6, 7		–	0.9	–		I_L = 220 mA T_j = 25 °C
			–	1.4	1.9		T_j = 150 °C
	channel 2, 3		–	1.6	–		I_L = 110 mA T_j = 25 °C
			–	2.6	3.9		T_j = 150 °C
6.5.2	Nominal load current	$I_{Out(nom)}$				mA	all channels on T_a = 100 °C $T_{j,max}$ = 150 °C based on R_{thja}
	channel 0, 1, 4, 5, 6, 7		260	380	–		[1]
	channel 2, 3		130	175	–		[1]
6.5.3	Output leakage current in sleep mode	$I_{Out(Sleep)}$	–	–	1	µA	V_{DS} = 13.5 V T_j = 25 °C[1]
			–	–	2		T_j = 85 °C [1]
			–	–	5		T_j = 150 °C
6.5.4	Output clamping voltage	$V_{OUT\_S(CL)}$	–	–	-16	V	–
		$V_{OUT\_DS(CL)}$	41	–	–	V	–
Input Characteristics (IN & LHI)							
6.5.5	L level	$V_{IN(L)}$	0	–	0.6	V	–
6.5.6	H level	$V_{IN(H)}$	1.8	–	5.5	V	–
6.5.7	Input voltage hysteresis	ΔV_{IN}	–	0.1	–	V	[1]
6.5.8	L-input pull-down current	$I_{IN(L)}$	1.5	–	–	µA	V_{IN} = 0.6 V [1]
6.5.9	H-input pull-down current	$I_{IN(H)}$	10	40	80	µA	V_{IN} = 5 V
Timings							
6.5.10	Turn-on time V_{DS} = 20% V_{bat}	t_{ON}				µs	V_{bb} = 13.5 V resistive load
	channel 0, 1,4,5		–	–	100		I_{DS}= 250 mA
	channel 2, 3		–	–	100		I_{DS}= 120 mA
	channel 6,7		–	–	100		I_{DS} = 250 mA
6.5.11	Turn-off time V_{DS} = 80% V_{bb}	t_{OFF}				µs	V_{bb} = 13.5 V resistive load
	channel 0, 1, 4, 5		–	–	100		I_{DS} = 250 mA
	channel 2, 3 (HS)		–	–	100		I_{DS} = 120 mA
	channel 6, 7 (LS)		–	–	100		I_{DS} = 250 mA

1) Not subject to production test, specified by design.

6.6 Command Description

Input Configuration Registers

ICR01 000_B

3	2	1	0
INX1		INX0	
rw		rw	

ICR23 001_B

3	2	1	0
INX3		INX2	
rw		rw	

ICR45 010_B

3	2	1	0
INX5		INX4	
rw		rw	

ICR67 011_B

3	2	1	0
INX7		INX6	
rw		rw	

Field	Bits	Type	Description
INXn n = 7 to 0	[3:2], [1:0]	rw	**Input Multiplexer Configuration Channel n** **00** Channel n is switched off 01 Channel n is switched by input 1 10 Channel n is switched by input 2 or 3 11 Channel n is switched on

7 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

7.1 Over Load Protection

The TLE7237SL is protected in case of over load or short circuit of the load. After time $t_{OFF(OVL)}$, the over loaded channel n switches off and the according diagnosis flag Dn is set. The channel can be switched on after clearing the protection latch by command CMD.CPL = 1. The CPL command clears itself with the next valid SPI communication frame. Please refer to **Figure 7** for details.

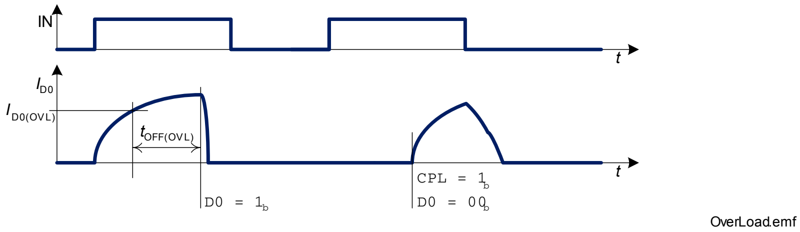

Figure 7 Shut Down at Over Load

7.2 Over Temperature Protection

A temperature sensor for each channel causes an overheated channel to switch off to prevent destruction. The according diagnosis flag is set. This flag is also set in OFF state, if the regarding channel temperature is too high.The channel can be only switched on after clearing the protection latch by SPI command CMD.CPL = 1. The CPL command clears itself with the next valid SPI communication frame. Please refer to **"Diagnostic Features" on Page 22** for information on diagnosis features.

7.3 ESD protection

There is a designed in protection against ESD disturbances up to the specified limit by using the defined model. Please see electrical characteristics **"ESD susceptibility on all pins" on Page 11**

7.4 Reverse Polarity Protection

There is a reverse polarity protection implemented in the TLE7237SL. This protection has to be divided into two parts. First the protection of the control circuits and second in the protection of the power transistors.

The control circuits are reverse polarity protected by protective measures in the ground connection. In case of reverse polarity, there is no current flow through the control circuits. To ensure this functionality, the GND pin and the substrate connections SUB must not be connected to the same potential. This means, the copper area dedicated for cooling should be connected at SUB and needs to be electrically isolated from GND.

The power transistors contain intrinsic body diodes that cause power dissipation. The reverse current through these intrinsic body diodes has to be limited by the connected loads. The over temperature and over load protection are not active during reverse polarity.

7.5 Loss of V_{bb}

In case of loss of V_{bb} connection in on-state, all inductances of the loads have to be demagnetized through the an additional path from V_{bb} to ground. Usually this path is given somewhere in the PCB circuitry, for example, as a suppressor diode like in the application diagram (see D1 in **Figure 14 "Application Diagram" on Page 34**).

7.6 Electrical Characteristics

Unless otherwise specified:
V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C
typical values: V_{DD} = 5.0 V, V_{BAT} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Over Load Protection							
7.6.1	Over load detection current at channel 0,1,4,5,6,7	$I_{Out(OVL)}$	0.5	–	1.0	A	
7.6.2	Over load detection current at channel 2,3	$I_{Out(OVL)}$	0.22	–	0.5	A	
7.6.3	Over load shut-down delay time	$t_{OFF(OVL)}$	–	–	60	µs	
Over Temperature Protection							
7.6.4	Thermal shut down temperature	$T_{j(SC)}$	150	170[1)]	–	°C	

1) Not subject to production test, specified by design

8 Diagnostic Features

The SPI of TLE7237SL provides diagnosis information about the device and about the load. The diagnosis information of the protective functions of channel n is latched in the diagnosis flags Dn. It is cleared by the SPI command CMD.CPL = 1. The CPL command clears itself with the next valid SPI communication frame.
The open load diagnosis of channel n is latched in the diagnosis flag OLn. This flag is cleared by reading the according diagnosis register.

Following table shows possible failure modes and the according protective and diagnostic action.

Failure Mode	Comment
Open Load	Diagnosis, when channel n is switched on: none Diagnosis, when channel n is switched off: according to voltage level at the output pin, flag OLn is set after time $t_{d(OL)}$. A diagnosis current can be enabled by SPI command DCCR.DCENn = 1.
Over Temperature	When over temperature occurs, the according diagnosis flag Dn is set. If the affected channel n was active it is switched off. The diagnosis flags are latched until they have been cleared by SPI command CMD.CPL = 1.
Over Load (Short Circuit)	When over load is detected at channel n, the affected channel is switched off after time $t_{OFF(OVL)}$ and the dedicated diagnosis flag Dn is set. The diagnosis flags are latched until they have been cleared by SPI command CMD.CPL = 1.

8.1 Electrical Characteristics

Unless otherwise specified:
V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C
typical values: V_{BAT} = 13.5 V, V_{DD} = 5.0 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
OFF State Diagnosis							
8.1.1	Open load diagnosis delay time	$t_{d(OL)}$	100	–	250	µs	–
High Side Channels 0,1,2,3							
8.1.2	Open load detection threshold voltage for Channel 0,1,2,3	$V_{D(OL0..3)}$	3	4	5	V	[1]
8.1.3	Output diagnosis current channel 0,1,2,3	$I_{L(DC0..3)}$	100	200	300	µA	measured at $V_{D(OL)}$ threshold
Configurable Channels 4,5							
8.1.4	Open load detection threshold voltage for Channel 4,5 in all configurations	$V_{D(OL4,5)}$	3	4	5	V	[1]
8.1.5	Output diagnosis current channel 4,5 in high side configuration	$I_{L(DCHS)}$	100	200	300	µA	measured at $V_{D(OL)}$ threshold
8.1.6	Output diagnosis current channel 4,5 in low side configuration	$I_{L(DCLS)}$	100	200	300	µA	measured at $V_{D(OL)}$ threshold
Low side Channels 6,7							
8.1.7	Open load detection threshold voltage for Channel 6,7	$V_{D(OL6,7)}$	3	4	5	V	[1]
8.1.8	Output diagnosis current channel 6,7	$I_{L(DC6,7)}$	100	200	300	µA	measured at VOL threshold
ON State Diagnosis (see also Protection in Chapter 7)							
8.1.9	Over load detection current at channel 0,1,4,5,6,7	$I_{L(OVL)}$	0.5	–	1.0	A	–
8.1.10	Over load detection current at channel 2,3	$I_{L(OVL)}$	0.22	–	0.5	A	–
8.1.11	Over load detection delay time at all channels	$t_{OFF(OVL)}$	–	–	60	µs	–

1) Open load detection voltages are referenced to ground

8.2 Command Description

Diagnosis Registers (read only, register bank RB = 1)

DR01 **00_B**

3	2	1	0
OL1	**D1**	**OL0**	**D0**
r	r	r	r

DR23 **01_B**

3	2	1	0
OL3	**D3**	**OL2**	**D2**
r	r	r	r

DR45 **10_B**

3	2	1	0
OL5	**D5**	**OL4**	**D4**
r	r	r	r

DR67 **11_B**

3	2	1	0
OL7	**D7**	**OL6**	**D6**
r	r	r	r

Field	Bits	Type	Description
Dn n = 7 to 0	2, 0	r	**Diagnostic Feedback of Channel n** **0** normal operation 1 over load or over temperature switch off occurred
OLn n = 7 to 0	3, 1	r	**Open Load Detection of Channel n** **0** normal operation 1 Open load at OFF-state occurred

CMD
Command Register **110_B**

3	2	1	0
Wake	**STB**	**RST**	**CPL**
r/w	r/w	r/w	r/w

Field	Bits	Type	Description
CPL	0	r/w	**please refer to Section 7 for description**
RST	1	r/w	**please refer to Section 5.1 for description**
STB	2	r/w	**please refer to Section 5 for description**
Wake	3	r/w	**please refer to Section 5 for description**

Diagnosis Current Configuration Register

DCCR0 100_B

3	2	1	0
DCEN3	**DCEN2**	**DCEN1**	**DCEN0**
r/w	r/w	r/w	r/w

DCCR1 101_B

3	2	1	0
DCEN7	**DCEN6**	**DCEN5**	**DCEN5**
r/w	r/w	r/w	r/w

Field	Bits	Type	Description
DCENn n = 7 to 0	3 to 0	r/w	**Diagnosis Current Enable Channel n** **0** Diagnosis current disabled 1 Diagnosis current enabled

9 Serial Peripheral Interface (SPI)

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the data rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. The interface provides daisy chain capability.

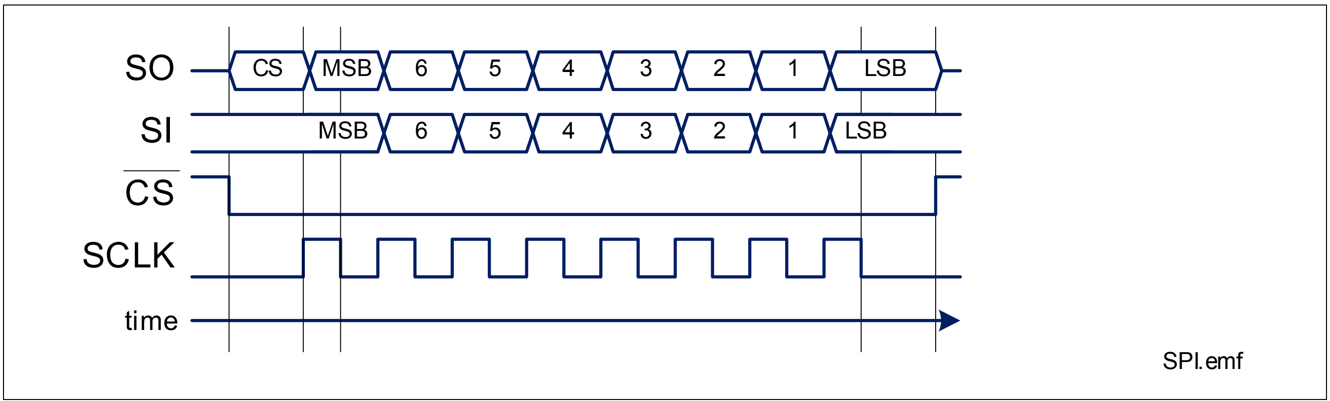

Figure 8 Serial Peripheral Interface

The SPI protocol is described in **Section 9.3**. It is reset to the default values after reset.

9.1 SPI Signal Description

$\overline{CS}$ - Chip Select: The system micro controller selects the TLE7237SL by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

$\overline{CS}$ High to Low transition:

- The diagnosis information is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (`TER`) and the signal level at pin SI. As a result, even in daisy chain configuration, a high signal indicates a faulty transmission. For details, please refer to **Figure 9**. This information stays available to the first rising edge of SCLK.

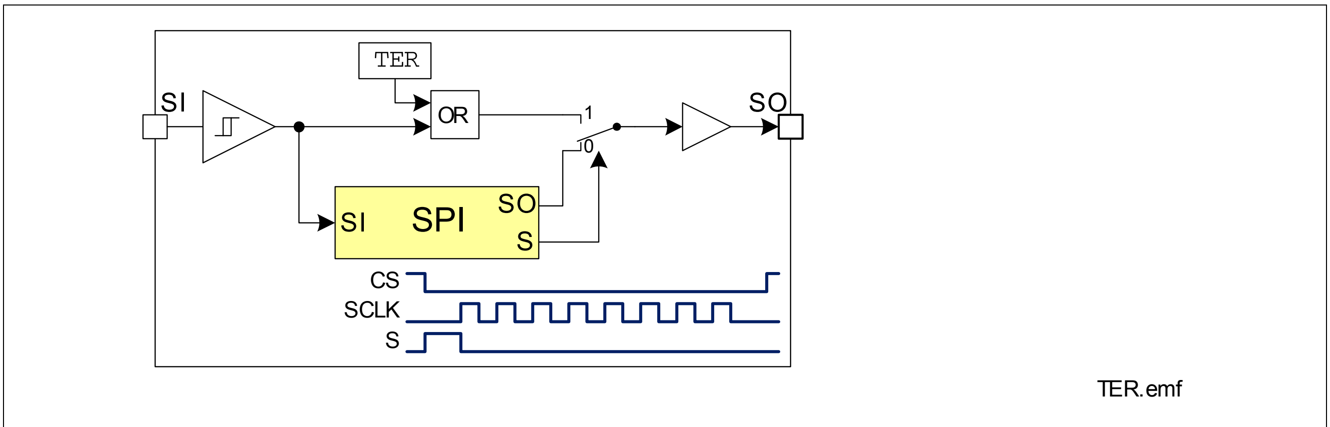

Figure 9 Transmission Error Flag on SO Line

CS Low to High transition:

- Command decoding is only done, when after the falling edge of CS exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected. In case of faulty transmission, the transmission error flag (TER) is set and the command is ignored.
- Data from shift register is transferred into the input matrix register.

SCLK - Serial Clock: This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select CS makes any transition.

SI - Serial Input: Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The 8 bit input data consist of two parts (control and data). Please refer to **Section 9.3** for further information.

SO Serial Output: Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CS pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 9.3** for further information.

9.2 Daisy Chain Capability

The SPI of TLE7237SL provides daisy chain capability. In this configuration several devices are activated by the same CS signal MCS. The SI line of one device is connected with the SO line of another device (see **Figure 10**), which builds a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK, which is connected to the SCLK line of each device in the chain.

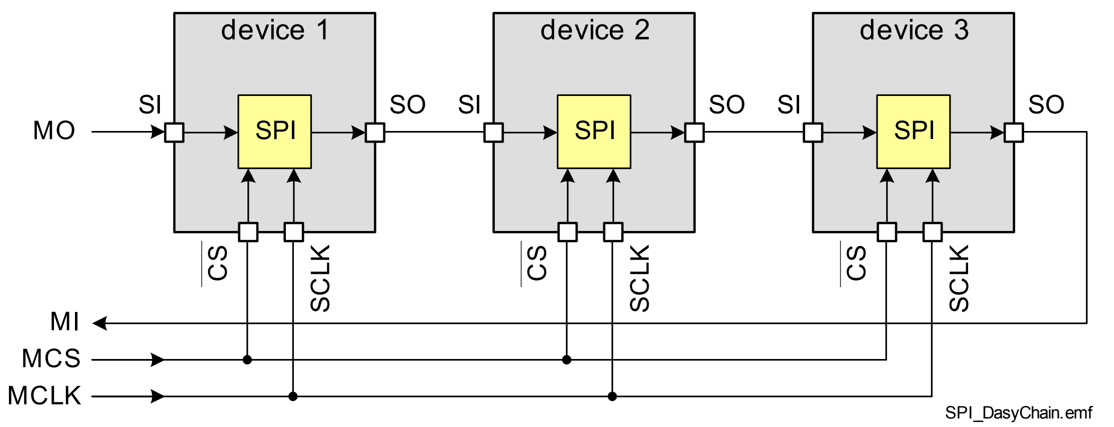

Figure 10 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out can be seen at SO. After 8 SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the CS line must go high to make the device accept the transferred data. In daisy chain configuration the data shifted out at device #1 has been shifted in to device #2. When using three devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the MCS line must go high (see **Figure 11**).

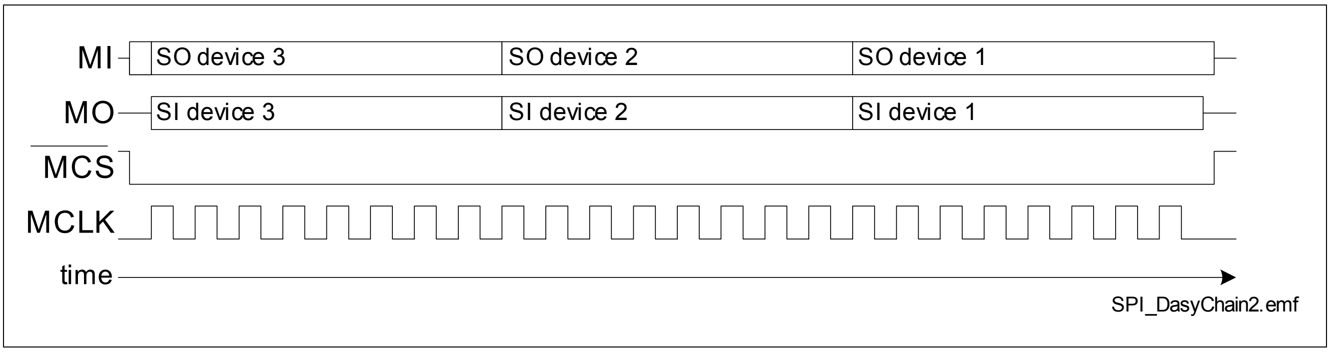

Figure 11 Data Transfer in Daisy Chain Configuration

9.3 SPI Protocol

The control and diagnosis function of the TLE7237SL is based on two register banks which are accessed via following SPI protocol. The control register bank contains eight registers (with 4 bit each) addressed by a 3 bit pointer. The diagnosis register bank contains four registers (with 4 bit each) addressed by a 2 bit pointer. An additional indication bit is available to differentiate between standard diagnosis information and data read from a register bank.

Control and Diagnosis Mode

	CS[1]	7	6	5	4	3	2	1	0
	Write Register Command								
SI		1	ADDR			DATA			
	Read Register Command								
SI		0	ADDR			x	x	0	RB
	Read Standard Diagnosis								
SI		0	x	x	x	x	x	1	x
	Standard Diagnosis								
SO	TER	0		AWK	0	D67	D45	D23	D01
	Second Frame of Read Command								
SO	TER	0	1	ADDR (Diagnosis)		DATA			
SO	TER	1	ADDR (Control)			DATA			

1) This bit is valid between $\overline{CS}$ hi -> lo and first SCLK lo -> hi transition.

Note: Reading a register needs two SPI frames. In the first frame the RD command is sent. In the second frame, the output at SPI signal SO will contain the requested information. Any command can be executed in the second frame.

Field	Bits	Type	Description
TER			**Transmission Error** 0 Previous transmission was successful (modulo 8 clocks received) **1** Previous transmission failed or first transmission after reset
RB	0		**Register Bank** 0 CONTR Control Register Bank 1 DIAG Diagnosis Register Bank (read only)
ADDR	6:4		**Address** Pointer to register for read and write command
DATA	3:0		**Data** Data written to or read from register selected by address ADDR

Standard Diagnosis:

Field	Bits	Type	Description
AWK	5		**Awake, Device active**
Dxy	3, 2, 1, 0		**Failure mode alert of channel x and y (Overtemp, Overload)**
OL	?		**common open load flag for all channels**

9.4 Register Overview

Control Register Bank

Name	Addr	3	2	1	0	default[1)]	type
ICR01	000_B	INX1		INX0		0_H	r/w
ICR23	001_B	INX3		INX2		0_H	r/w
ICR45	010_B	INX5		INX4		0_H	r/w
ICR67	011_B	INX7		INX6		0_H	r/w
DCCR0	100_B	DCEN3	DCEN2	DCEN1	DCEN0	0_H	r/w
DCCR1	101_B	DCEN7	DCEN6	DCEN5	DCEN4	0_H	r/w
CMD	110_B	WAKE	STB	RST	CPL[2)]	0_H	w
unused	111_B	–	–	–	–	0_H	–

1) The default values are set after V_{bb} power-on, STB-command and RST-command
All command bits are cleared at the end of transmission, respectively after execution
2) CPL bit needs a valid next SPI communication frame to be cleared

Input word (see Chapter 6.6 for detailed description)

Name	State	1	0
INX0 - INX7	**OFF**	**0**	**0**
	IN1	0	1
	IN2 or IN3	1	0
	ON	1	1

Diagnosis Register Bank (read only)

Name	Addr	3	2	1	0
DR01	000_B	OL1	D1	OL0	D0
DR23	001_B	OL3	D3	OL2	D2
DR45	010_B	OL5	D5	OL4	D4
DR67	011_B	OL7	D7	OL6	D6

9.5 Timing Diagrams

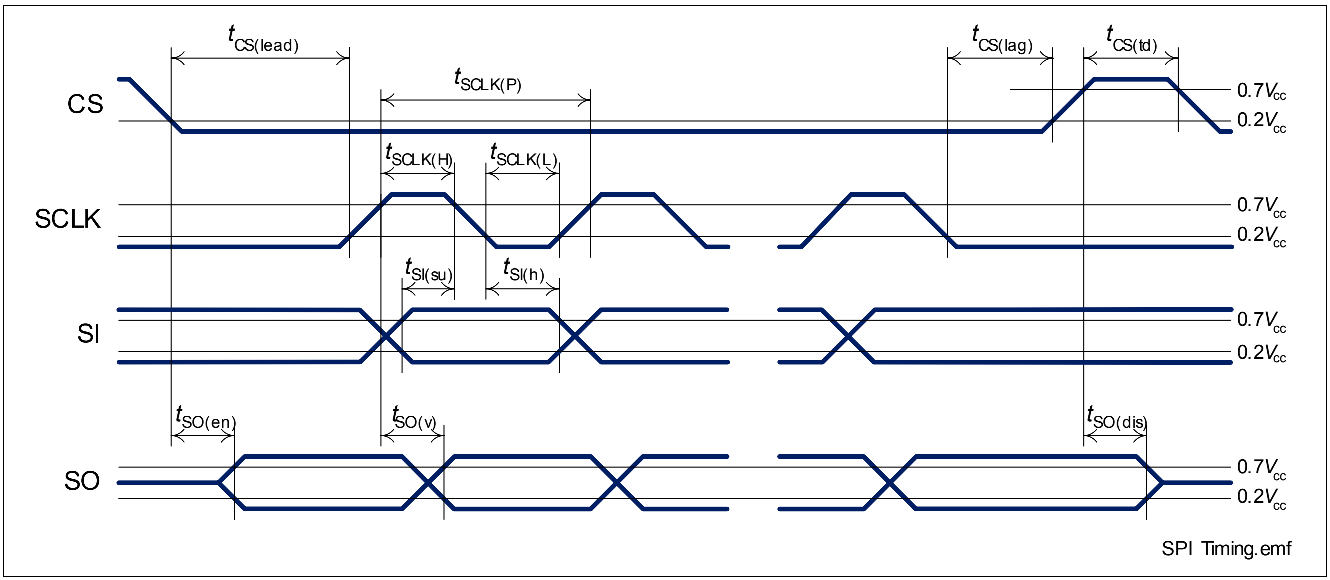

Figure 12 Timing Diagram

9.6 Electrical Characteristics

Unless otherwise specified: V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C
typical values: V_{DD} = 5.0 V, V_{BAT} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Input Characteristics ($\overline{CS}$, SCLK, SI)							
9.6.1	L level of pin $\overline{CS}$ SCLK SI	 $V_{CS(L)}$ $V_{SCLK(L)}$ $V_{SI(L)}$	0	–	0.2*V_{DD}	V	–
9.6.2	H level of pin $\overline{CS}$ SCLK SI	 $V_{CS(H)}$ $V_{SCLK(H)}$ $V_{SI(H)}$	0.5*V_{DD}	–	V_{DD}	V	–
9.6.3	L-input pull-up current through $\overline{CS}$	$I_{CS(L)}$	5	40	90	µA	V_{CS} = 0 V V_{DD} = 5 V
9.6.4	H-input pull-up current through $\overline{CS}$	$I_{CS(H)}$	2.5	–	–	µA	1) V_{DD} = 5 V V_{CS} = 0.5*V_{DD}
9.6.5	L-input pull-down current through pin SCLK SI	$I_{SCLK(L)}$ $I_{SI(L)}$	1.5	–	–	µA	1) V_{DD} = 5 V V_{SCLK} = V_{SI} = 0.2*V_{DD}
9.6.6	H-input pull-down current through pin SCLK SI	$I_{SCLK(H)}$ $I_{SI(H)}$	10	40	80	µA	1) V_{DD}= 5 V V_{SCLK} = V_{SI} = V_{DD}
Output Characteristics (SO)							
9.6.7	L level output voltage	$V_{SO(L)}$	0	–	0.4	V	I_{SO} = +2 mA
9.6.8	H level output voltage	$V_{SO(H)}$	V_{DD} - 0.4 V	–	V_{DD}		I_{SO} = -1.5 mA
9.6.9	Output tristate leakage current	$I_{SO(OFF)}$	-10	–	10	µA	V_{CS} = V_{DD}
Timings							
9.6.10	Serial clock frequency	f_{SCLK}	0	–	5	MHz	–
9.6.11	Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	–
9.6.12	Serial clock high time	$t_{SCLK(H)}$	50	–	–	ns	1)
9.6.13	Serial clock low time	$t_{SCLK(L)}$	50	–	–	ns	1)
9.6.14	Enable lead time (falling $\overline{CS}$ to rising SCLK)	$t_{CS(lead)}$	250	–	–	ns	1)
9.6.15	Enable lag time (falling SCLK to rising $\overline{CS}$)	$t_{CS(lag)}$	250	–	–	ns	1)
9.6.16	Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$)	$t_{CS(td)}$	250	–	–	ns	1)
9.6.17	Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	–	–	ns	1)
9.6.18	Data hold time (falling SCLK to SI)	$t_{SI(h)}$	20	–	–	ns	1)

Unless otherwise specified: V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C
typical values: V_{DD} = 5.0 V, V_{BAT} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
9.6.19	Output enable time (falling $\overline{CS}$ to SO valid)	$t_{SO(en)}$	–	–	200	ns	C_L = 20 pF [1)]
9.6.20	Output disable time (rising $\overline{CS}$ to SO tri-state)	$t_{SO(dis)}$	–	–	200	ns	C_L = 20 pF [1)]
9.6.21	Output data valid time with capacitive load	$t_{SO(v)}$	–	–	100	ns	C_L = 20 pF [1)]

1) Not subject to production test, specified by design.

10 Package Outlines

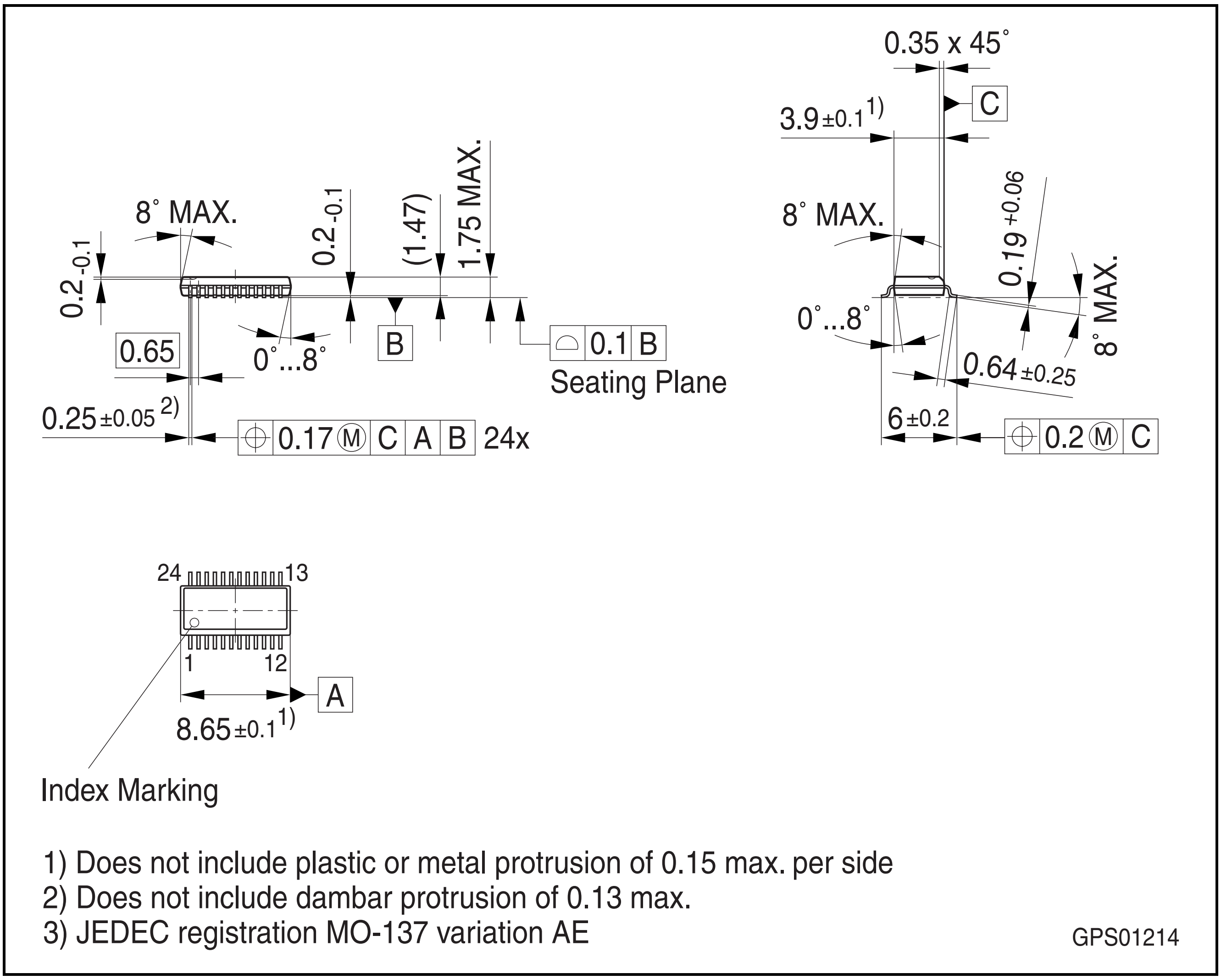

Figure 13 PG-SSOP 24-5 (Plastic Green Slim Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website: **http://www.infineon.com/packages**.

Dimensions in mm

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

Figure 14 shows a simplified application circuit. Vdd need to be externally reverse polarity protected.

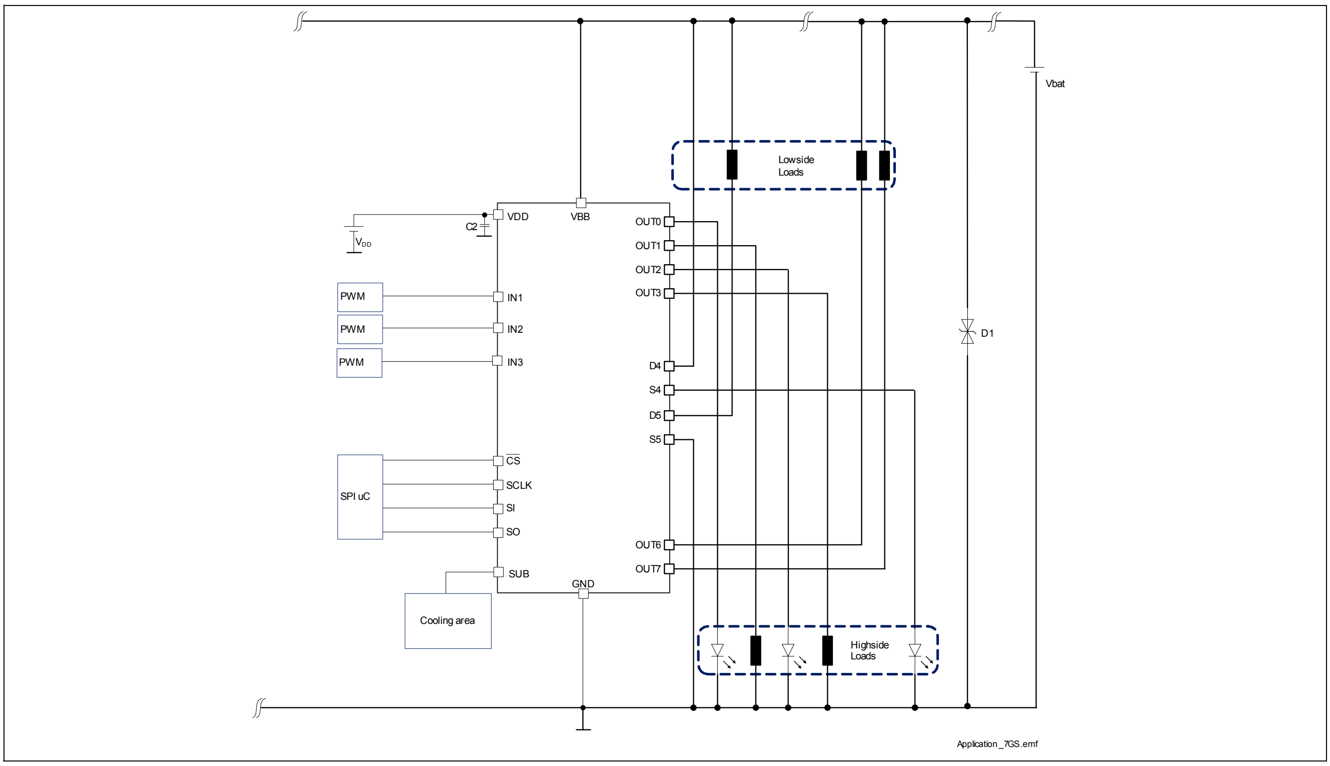

Figure 14 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

The circuit above shows a example of using this device in a automotive target application.

D1 is optional for loss of battery or loss of ground if no other circuit on this battery feed can limit the voltage to the max. rating of the device (-40 V) .

C2 is for EMC and to stabilize the digital driver, recommended value is 47nF.

There are no resistors to the µC needed due to the internal reverse polarity protection.

For further information you may contact **http://www.infineon.com/spider**

12 Revision History

Revision	Date	Changes
Rev. 1.1	2011-04-05	new parameter 4.2.5 on page 11 “Digital supply turn-ON time” added
Rev. 1.0	2010-02-18	Datasheet released

Edition 2011-04-05

Published by
Infineon Technologies AG
81726 Munich, Germany

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