2Pai Semi

3.75kVrms Isolated Single Channel Gate Driver

Data Sheet

Pai8211A

FEATURES

- **RoHS-compliant, NB SOIC-8 package**
- **6A peak source and sink drive current**
- **2.5V to 5.5V Input supply voltage**
- **Up to 33V Driver supply voltage**
  - **8V UVLO protection**
- **3.75kVrms isolation voltage**
- **150kV/us typical CMTI**
- **51ns typical propagation delay**
- **CMOS inputs**
- **Safety and regulatory approvals:**
  - **UL certificate number: (Pending)**
    - **3.75kVrms for 1 minute per UL 1577**
  - **VDE certificate number: (Pending)**
    - **DIN VDE V 0884-11:2017-01**
    - **V_{IORM} = 1200V peak**
  - **CQC certification per GB4943.1-2011:(Pending)**
- **Operating temperature range: -40°C to 125°C**

APPLICATIONS

- **Switched-Mode Power Supplies**
- **EV/HEV Inverters and DC/DC Converters**
- **Solar Inverters**
- **Motor Control**
- **UPS and PSU**

GENERAL DESCRIPTION

The Pai82xxxx is a 2PaiSemi isolated gate driver product family that provide outstanding performance characteristics by using 2PaiSemi ***iDivider®*** technology.

Intelligent voltage divider technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The Pai8211A is a 6A single-channel isolated gate driver with 3.75kVrms isolation voltage per UL 1577.

The Pai8211A provides a split output that controls the rise and fall times individually, which is flexible to solve EMI problems.

Low propagation delay, typical 51ns, is suitable for high efficiency switching power systems.

Wide output VCC operating range from 9.5V to 33V enables effective driving with Si or SiC MOSFET and IGBT power switches. Integrated UVLO protection ensures output held at low under abnormal conditions. The input VCC operates from 2.5V to 5.5V, which supports most digital controllers.

Compared to an optocoupler, Pai8211A has lower propagation delay, lower part-to-part skew, higher operating temperature and higher CMTI. It is very convenient to control MOSFET/IGBT gate drive across isolation barrier or with level shifting.

FUNCTIONAL BLOCK DIAGRAMS

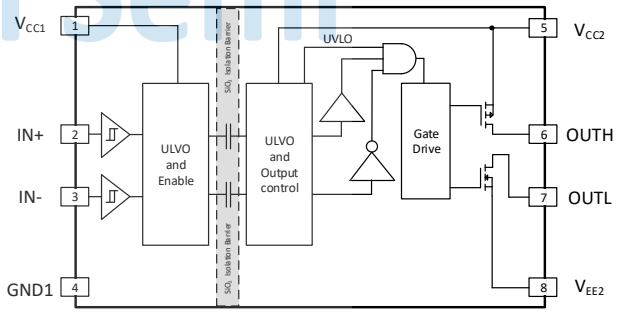

Figure1. Pai8211A Functional Block Diagrams

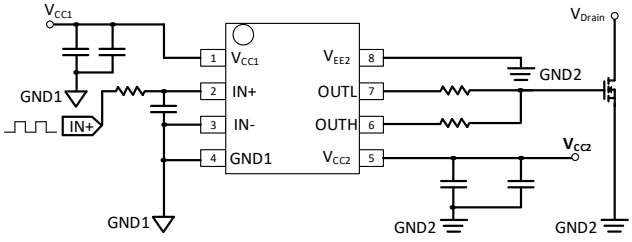

Figure2. Pai8211A Typical Application Circuit

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PIN CONFIGURATIONS AND FUNCTIONS

Table1. Pai8211A Pin Function Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	V_{CC1}	P	Input Power Supply
2	IN+	I	Positive Input
3	IN-	I	Negative Input
4	GND1	G	Input Ground
5	V_{CC2}	P	Output Power Supply
6	OUTH	O	Pull High Output
7	OUTL	O	Pull Low Output
8	V_{EE2}	G	Output Ground

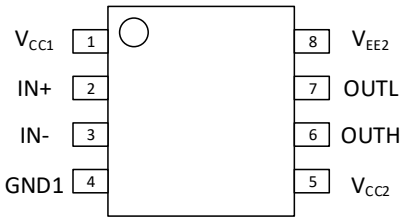

Figure3. Pai8211A Pin Configuration

SPECIFICATIONS

Absolute Maximum Ratings

Table2. Pai8211A Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

DESCRIPTION		MIN	MAX	UNIT
V_{CC1}	Input supply voltage (reference to GND1)	-0.3	7	V
IN+, IN-	Signal input voltage	-0.3	V_{CC1}+0.3	V
V_{CC2}	Output supply voltage (reference to V_{EE2})	-0.3	36	V
OUTH, OUTL	Gate driver output voltage	V_{EE2}-0.3	V_{CC2}+0.3	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

ESD Rating

Table3. Pai8211A ESD Ratings

DESCRIPTION		Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-6000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-2000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Table4. Pai8211A Recommended Operating Conditions

DESCRIPTION		MIN	MAX	UNIT
V_{CC1}	Input supply voltage	2.5	5.5	V
V_{In+}/ V_{In-}	Input voltage	0	V_{CC1}	V
V_{CC2}	Output supply voltage	9.5	33	V
T_A	Ambient temperature	-40	125	°C

Truth Table

Table5. Pai8211A Truth Table

V_{CC1}	IN+	IN-	V_{CC2}	OUTH	OUTL
above UVLO	L(1) or floating	X	above UVLO	Hi-Z	L
above UVLO	H	H or floating	above UVLO	Hi-Z	L
above UVLO	H	L	above UVLO	H	Hi-Z
X	X	X	below UVLO	Hi-Z	L
below UVLO	X	X	X	Hi-Z	L

(1) L=Logic Low, H= Logic High, X=H, L or floating, Hi-Z= High impedance.

Thermal Information

Table6. Pai8211A NB SOIC-8 Thermal Information

PACKAGE THERMAL RATINGS	Rating	UNIT
$R_{\theta JA}$ Junction-to-Ambient thermal resistance	110	°C/W
Ψ_{JT} Junction–to-top characterization parameter	18	°C/W

Supply Power Ratings

Table7. Pai8211A Supply Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D Maximum power dissipation on input and output	V_{CC1} = 5 V, V_{CC2} = 15 V, f = 1.8MHz,50% duty cycle, square wave, 2.2nF load			1.14	W
P_{D1} Maximum input power dissipation				0.01	W
P_{D2} Maximum output power dissipation				1.13	W

Electrical Specifications

Table8. Pai8211A Electrical Specifications

V_{CC1} = 2.5V_{DC}±3% or 3.3V_{DC}±10% or 5V_{DC}±10%, 0.1uF capacitor from V_{CC1} to GND1, V_{CC2} = 15V_{DC}±10%, 1uF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} =1nF. T_A = –40°C to 125°C

(Unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS					
I_{VCC1} V_{CC1} quiescent current			0.8		mA
I_{VCC2} V_{CC2} quiescent current			1.8		mA
SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS					
$V_{UV+(VCC1)}$	V_{CC1} Undervoltage Rising Threshold	2.10	2.25	2.40	V
$V_{UV-(VCC1)}$	V_{CC1} Undervoltage Falling Threshold	2.00	2.10	2.20	V
$V_{HYS(VCC1)}$	V_{CC1} UVLO threshold hysteresis		0.15		V
$V_{UV+(VCC2)}$	V_{CC2} Undervoltage Rising Threshold		8.4	9.4	V
$V_{UV-(VCC2)}$	V_{CC2} Undervoltage Falling Threshold	7.1	7.8		V
$V_{HYS(VCC2)}$	V_{CC2} UVLO threshold hysteresis		0.6		V
INPUT					
V_{INH} Input rising threshold			0.50*V_{CC1}	0.60*V_{CC1}	V
V_{INL} Input falling threshold		0.30*V_{CC1}	0.35*V_{CC1}		V
V_{HYS}			0.15*V_{CC1}		
OUTPUTS					
I_{OH}/I_{OL} Peak source and sink current	C_{LOAD} = 0.22uF, with external current limiting resistors, 1kHz switching frequency	6	10		A
V_{OH} High-level output voltage (V_{CC2}-V_{OUTH})	I_{OUTH}= –20 mA		100		mV
V_{OL} Low level output voltage (V_{OUTH}-V_{OUTL})	I_{OUTL} = 20mA		7.5		mV
TIMING					
t_{PLH} Propagation delay, high[1] t_{PHL} Propagation delay, low[1]	C_{LOAD} = 1.8nF		51 51	65 65	ns
t_{PWD} Pulse Width Distortion	C_{LOAD} = 1.8nF		1	10	ns
t_r Rise time[2] t_f Fall time[2]	C_{LOAD} = 1.8nF		8 7	15 12	ns
CMTI	Common-mode transient immunity[3]		150		kV/us

(1) t_{PLH} = low-to-high propagation delay time, t_{PHL} = high-to-low propagation delay time. See Figure21.

(2) t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal，t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal. See Figure20.

(3) See Figure24 for Common-mode transient immunity (CMTI) measurement.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Insulation Specifications

Table9. Pai8211A Insulation Specifications

PARAMETER	SYMBOL	VALUE	UNIT	TEST CONDITIONS/COMMENTS
Rated Dielectric Insulation Voltage		3750	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	⩾4	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	⩾4	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		⩾21	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

Package Specifications

Table10. Pai8211A Package Specifications

PARAMETER	SYMBOL	TYPICAL VALUE	UNIT	TEST CONDITIONS/COMMENTS
Resistance (Input to Output)[1]	R_{I-O}	10^{11}	Ω	
Capacitance (Input to Output)[1]	C_{I-O}	1.5	pF	@1MHz
Input Capacitance[2]	C_I	3	pF	@1MHz

(1) The device is considered a 2-terminal device; SOIC-8 Pin 1 - Pin 4 are shorted together as the one terminal, and SOIC-8 Pin 5 - Pin 8 are shorted together as the other terminal.

(2) Testing from the input signal pin to ground.

Regulatory Information

Table11. Pai8211A Regulatory Information

The Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

UL	VDE	CQC
Recognized under UL 1577 Component Recognition Program[1]	DIN VDE V 0884-11:2017-01[2]	Certified under CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750V rms Isolation Voltage	Basic insulation, V_{IORM} = 1200V peak, V_{IOSM} =5000V peak	Basic insulation at 500V rms (707V peak) working voltage
File (pending)	File (pending)	File (pending)

(1) In accordance with UL 1577, each Pai8211A is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec.

(2) In accordance with DIN V VDE V 0884-11, each Pai8211A is proof tested by applying an insulation test voltage ≥ 1800V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-11 approval.

VDE Insulation Characteristics

Table12. VDE Insulation Characteristics

DESCRIPTION	TEST CONDITIONS/COMMENTS	SYMBOL	CHARACTERISTIC	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			 I to IV I to III I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive peak isolation voltage		V_{IORM}	1200	V peak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.5 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	1800	V peak
Input to Output Test Voltage, Method A After Environmental Tests Subgroup 1 After Input and/or Safety Test Subgroup 2 and Subgroup 3	 V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	 1440 1440	 V peak V peak
Highest Allowable Overvoltage		V_{IOTM}	5300	V peak
Surge Isolation Voltage Basic	Basic insulation, 1.2/50 µs combination wave, VTEST = 1.3 × VIOSM (qualification)[1]	V_{IOSM}	5000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure5)			
Maximum safety Temperature		T_S	150	°C
Maximum Power Dissipation at 25°C		P_S	1.14	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

(1) In accordance with DIN V VDE V 0884-11, Pai8211A is proof tested by applying a surge isolation voltage 6500V.

TYPICAL CHARACTERISTIC

V_{CC1}=2.5V_{DC}±3% or 3.3V_{DC}±10% or 5V_{DC}±10%, 0.1uF capacitor from V_{CC1} to GND1, V_{CC2} = 15V_{DC}±10%, 1uF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} =1nF. T_A = –40°C to 125°C (Unless otherwise noted).

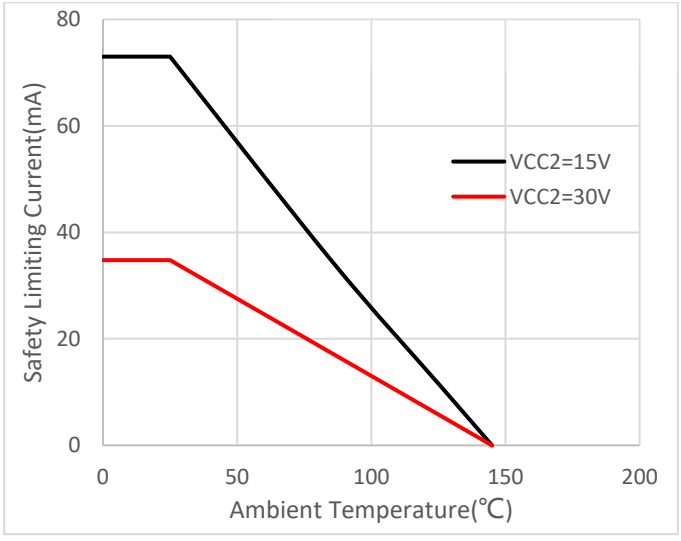

Figure4. Thermal Derating Curve for Limiting Current with Ambient Temperature per VDE

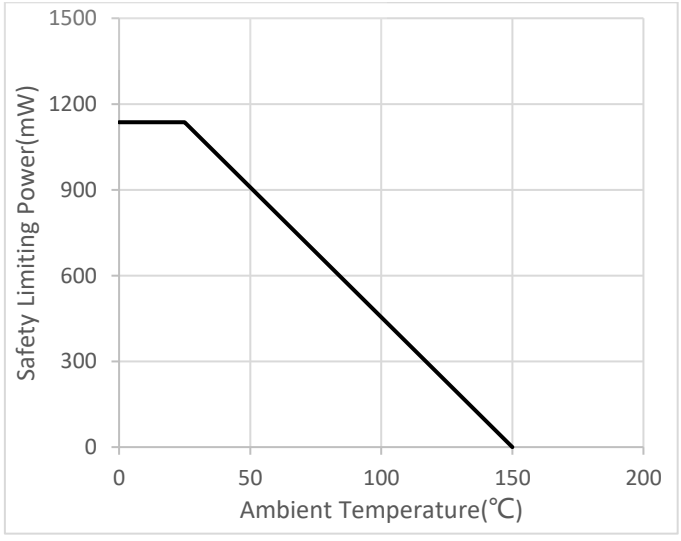

Figure5. Thermal Derating Curve for Limiting Power with Ambient Temperature per VDE

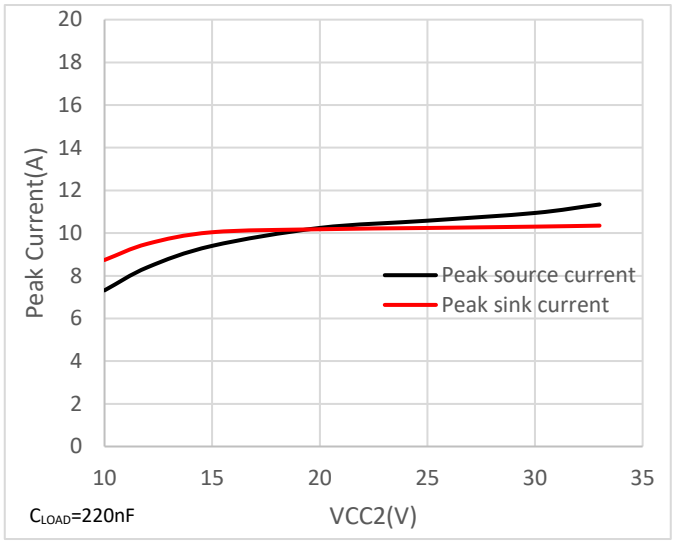

Figure6. Output High Drive Current vs V_{CC2}

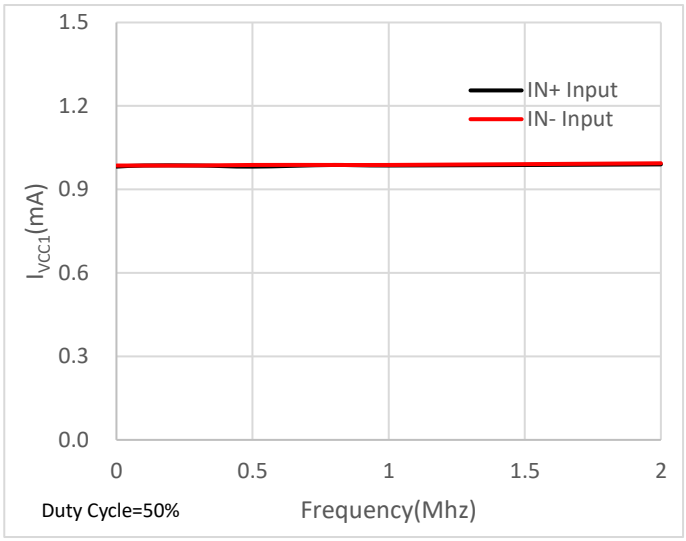

Figure7. I_{VCC1} Supply Current vs Input Frequency

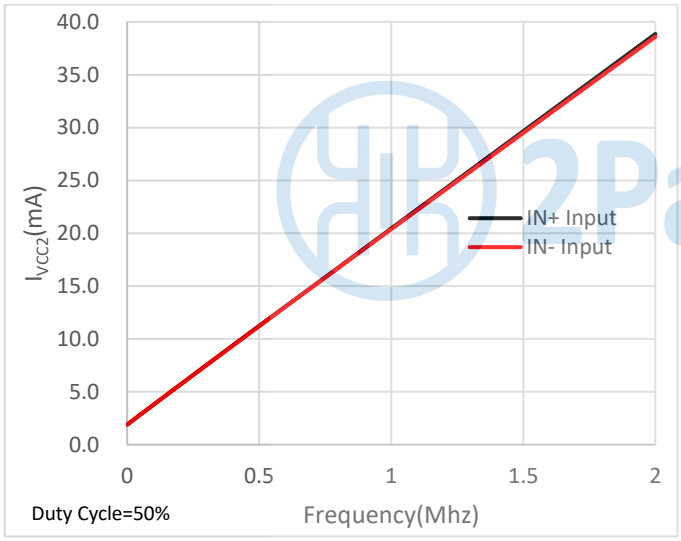

Figure8. I_{VCC2} Supply Current vs Input Frequency

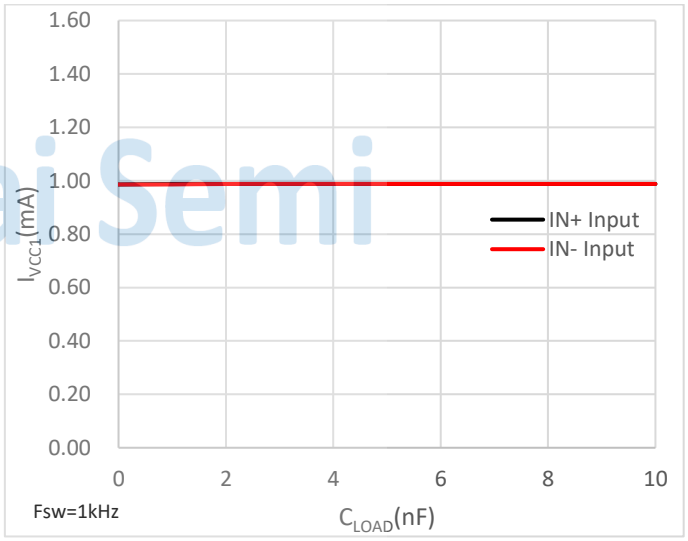

Figure9. I_{VCC1} Supply Current vs Load Capacitance

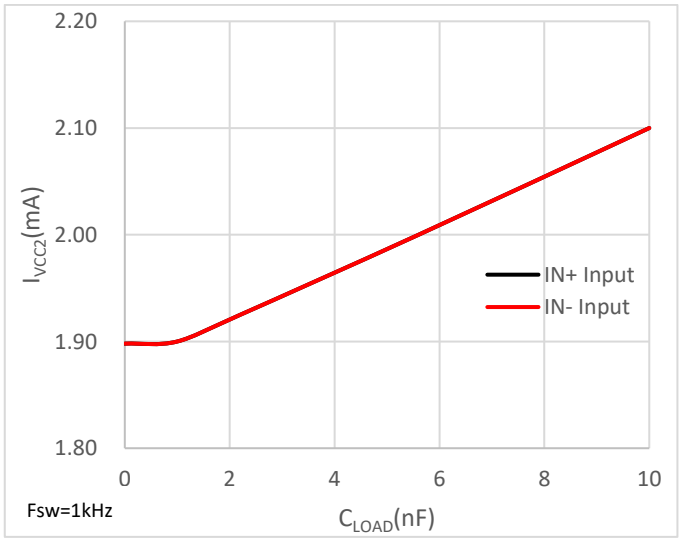

Figure10. I_{VCC2} Supply Current vs Load Capacitance

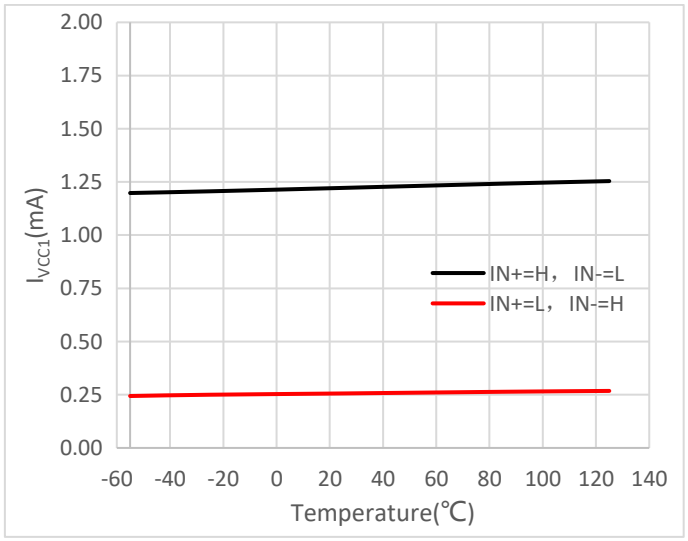

Figure11. I_{VCC1} Supply Current vs Ambient Temperature

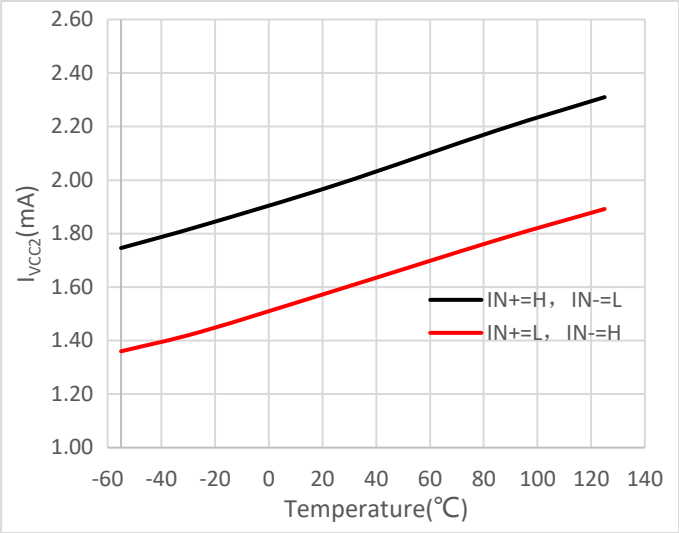

Figure12. I_{VCC2} Supply Current vs Ambient Temperature

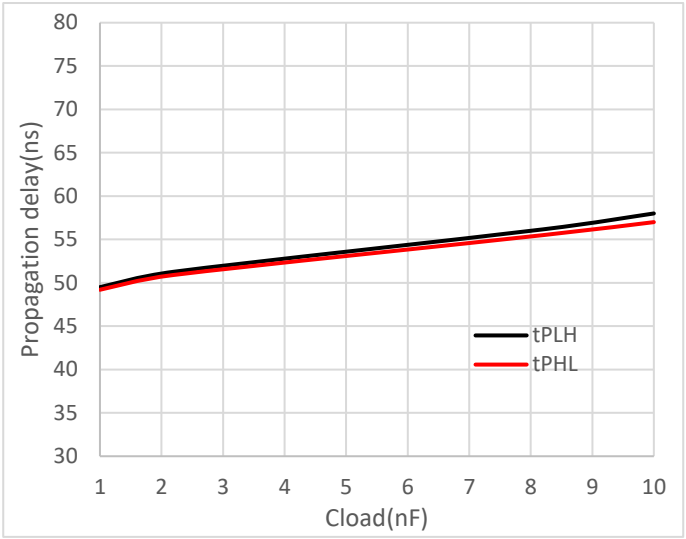

Figure13. Propagation Delay vs Load Capacitance

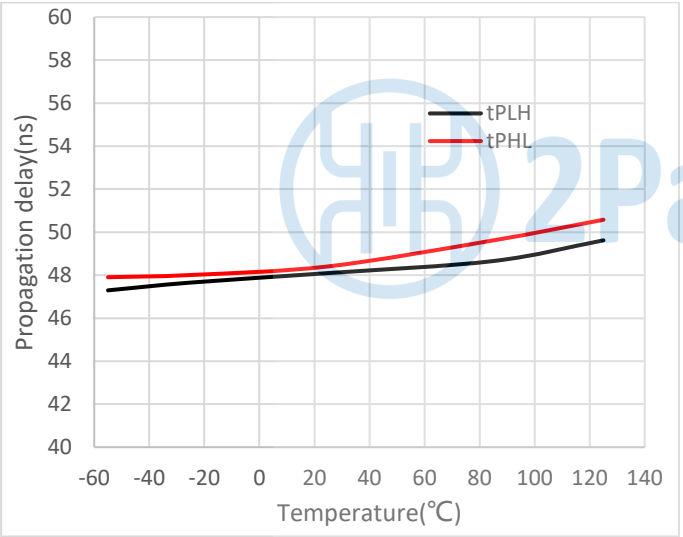

Figure14. Propagation Delay vs Ambient Temperature

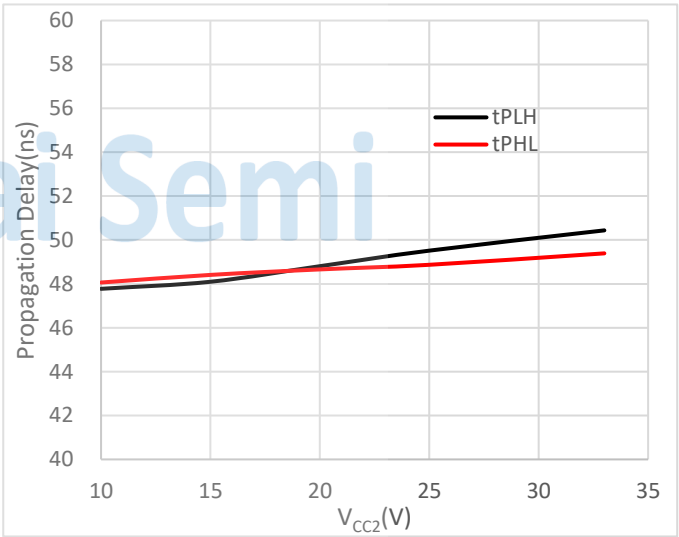

Figure15. Propagation Delay vs V_{CC2}

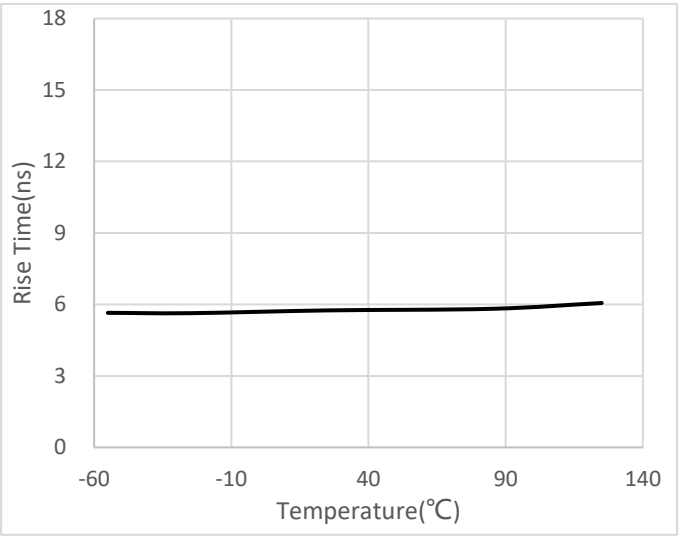

Figure16. Rise Time vs Ambient Temperature

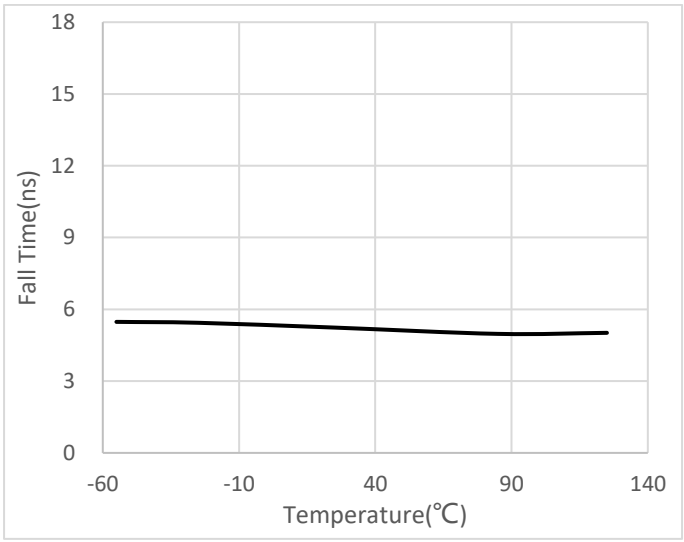

Figure17. Fall Time vs Ambient Temperature

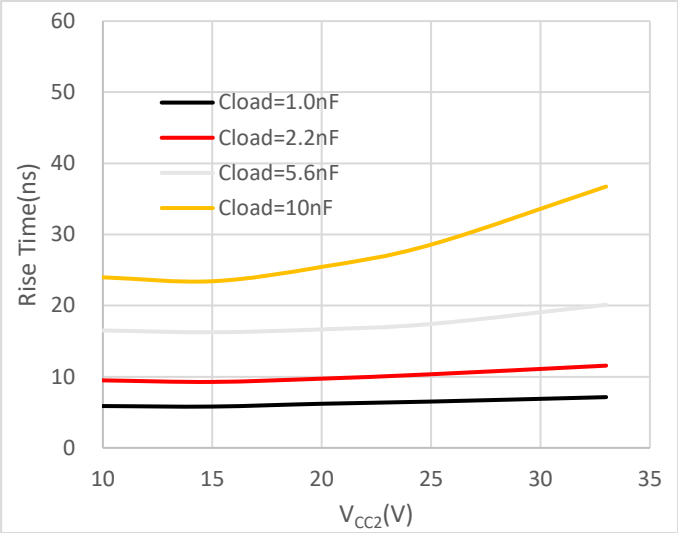

Figure18. Rise Time vs C_{LOAD} and V_{CC2}

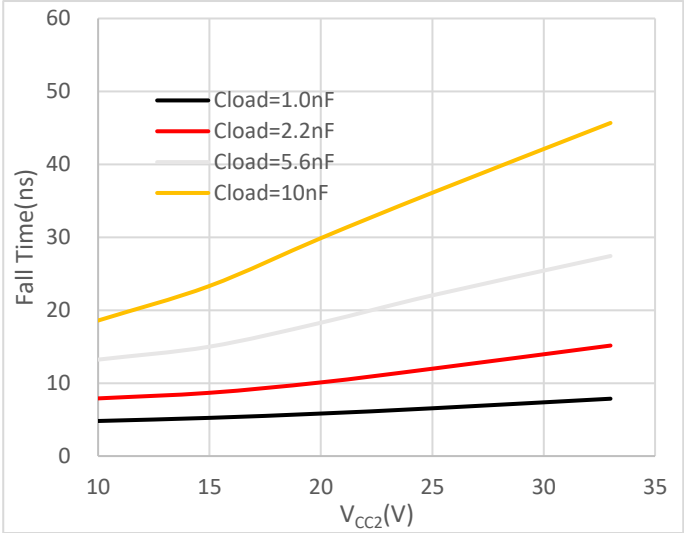

Figure19. Fall Time vs C_{LOAD} and V_{CC2}

TIMING TEST INFORMATION

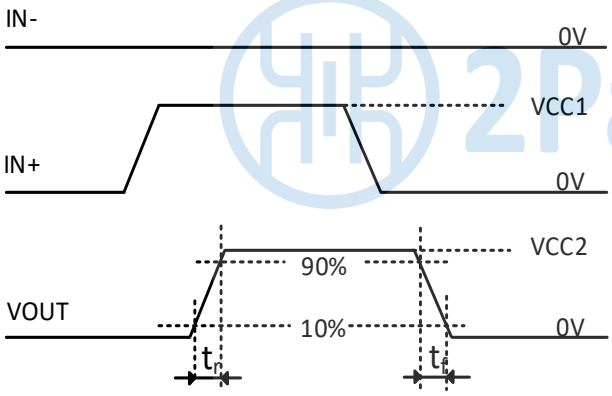

Figure20. Transition time waveform measurement

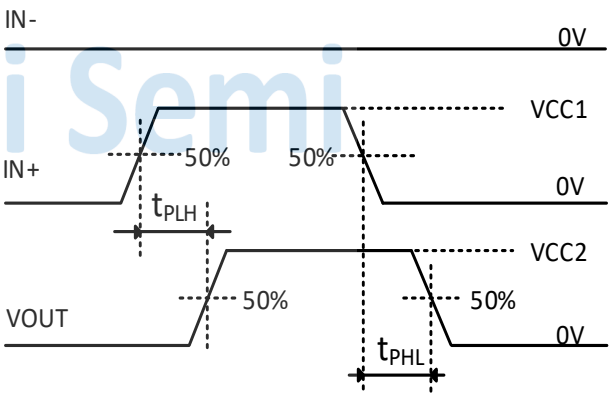

Figure21. Propagation delay time waveform measurement

APPLICATIONS INFORMATION

Typical Application

The circuit figure below is a typical application for driving IGBTS.

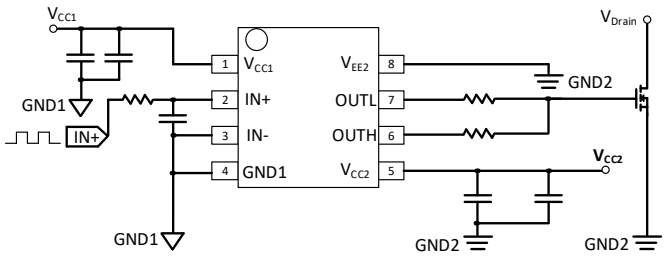

Figure22A. typical application circuit-IN+ Input

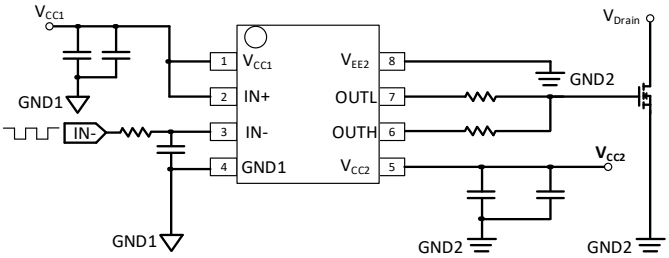

Figure22B. typical application circuit-IN- Input

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{CC1} and GND1 and between V_{CC2} and V_{EE2}. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value between V_{CC1} and GND1 is between 0.1 μF and 1μF, bypass capacitor value between V_{CC2} and V_{EE2} is between 1 μF and 10 μF. Additional 100nF capacitor in parallel with the isolator device bypass capacitor is recommended for high frequency filtering.

To avoid large negative transients on the VEE2 pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

Avoid reducing the isolation capability, keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

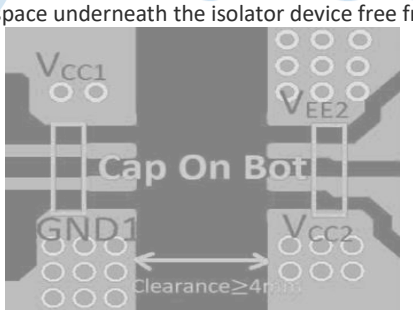

Figure23. Layout example

CMTI MEASUREMENT

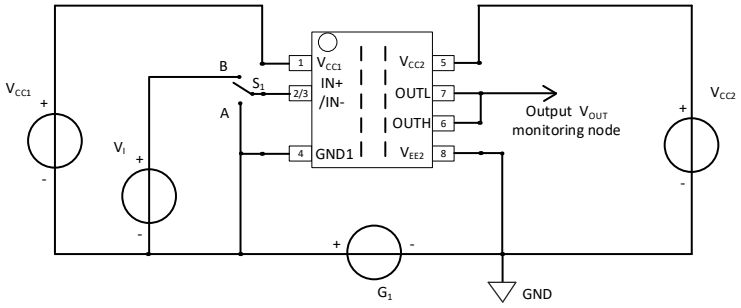

Figure24. Common-mode transient immunity (CMTI) measurement

To measure the Common-Mode Transient Immunity (CMTI) of Pai82xxxx isolated gate driver under specified common-mode pulse magnitude (VCM) and specified slew rate of the common-mode pulse (dVCM/dt) and other specified test or ambient conditions, The common-mode pulse generator (G1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (VCM),such that the maximum common-mode slew rates (dVCM/dt) can be applied to Pai82xxxx isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground V_{EE2} of Pai82xxxx isolated gate driver, with positive transients as well as negative transients.

Pai82xxxx 系列隔离驱动器的共模瞬变抗扰度(CMTI)需要在指定的共模脉冲幅度(V_{CM})和指定的共模脉冲压摆率(dV_{CM}/dt)以及其他指定的测试或环境条件下测量。共模脉冲发生器(G1)能提供指定幅度快速上升/下降和持续时间的共模脉冲，最大共模电压转换率(dV_{CM}/dt)可以用于 Pai82xxxx 隔离驱动器的 CMTI 测量。共模脉冲施加在 Pai82xxxx 隔离驱动器的一侧接地 GND_1 和另一侧接地 V_{EE2} 之间，并且应能够提供正向瞬变和负向瞬变。

OUTLINE DIMENSIONS

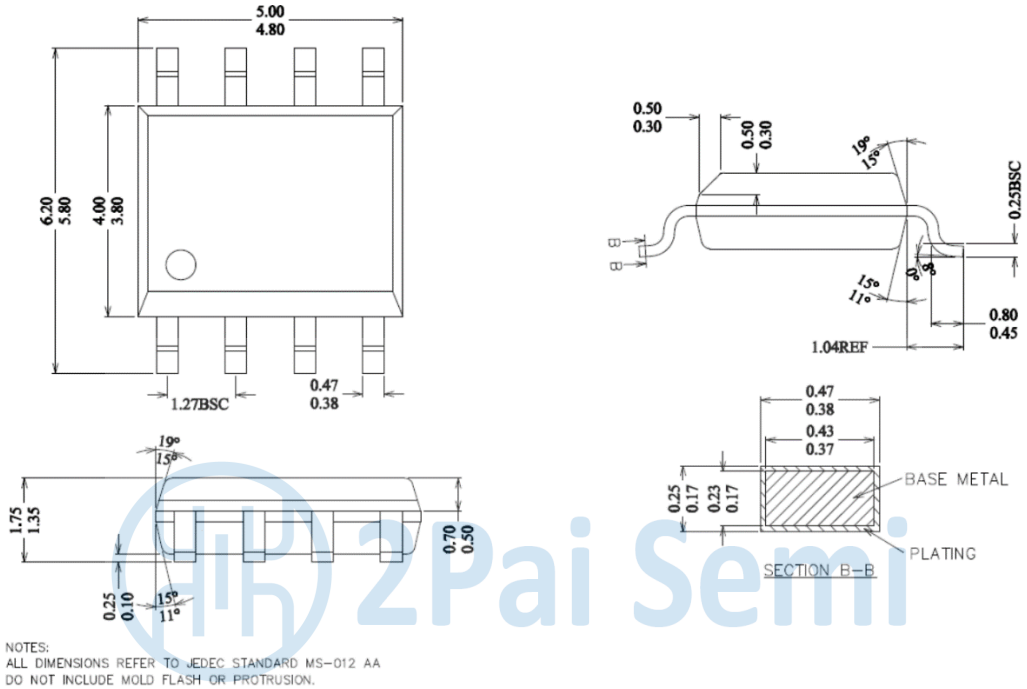

Figure25. 8-Lead Narrow Body SOIC [NB SOIC-8] *Outline Package–dimension unit(mm)*

LAND PATTERNS

8-Lead Narrow Body SOIC [NB SOIC-8]

The figure below illustrates the recommended land pattern details for the Pai82xxxx in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

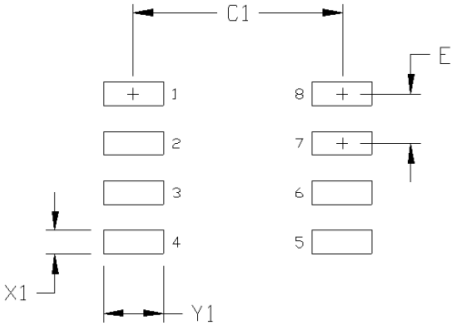

Figure26. 8-Lead Narrow Body SOIC [NB SOIC-8] Land Pattern

Table13. NB SOIC-8 Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	5.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.55	mm

(1) This land pattern design is based on IPC -7351.

(2) All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

REEL INFORMATION

8-Lead Narrow Body SOIC [NB SOIC-8]

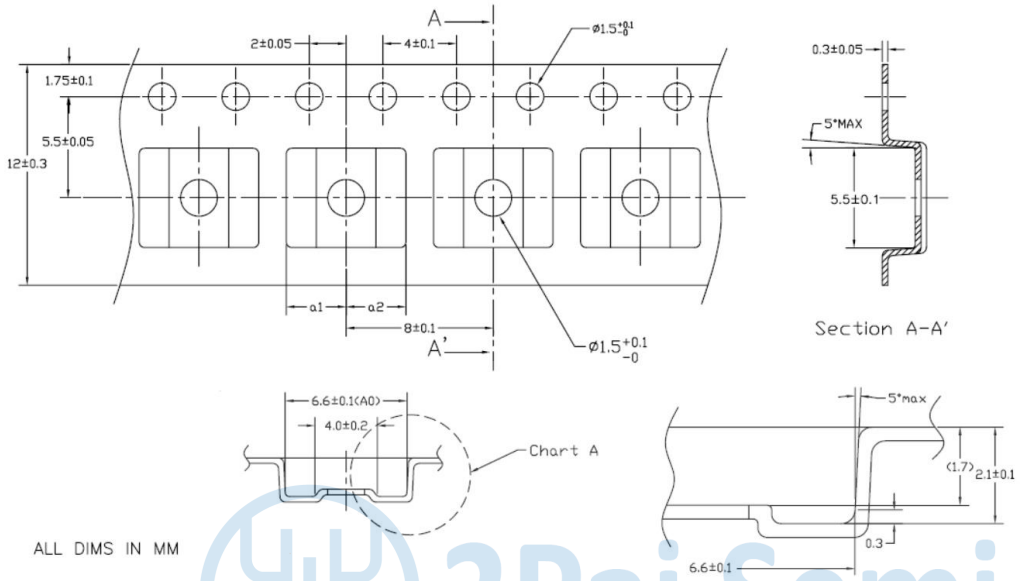

Figure27. 8-Lead Narrow Body SOIC [NB SOIC-8] Reel Information–*dimension unit(mm)*

ORDERING GUIDE

Table14. Ordering Guide

Model Name	Temperature Range	No. of Outputs	Output Current(A)	Isolation Rating (kV rms)	Package	MSL Peak Temp [1]	MOQ/ Quantity per reel[2]
Pai8211A-SR	−40 to 125°C	1	6	3.75	NB SOIC-8	Level-3-260C-168 HR	4000

(1) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(2) MOQ, minimum ordering quantity.

REVISION HISTORY

Revision	Date	Page	Change Record
1.0	2021/08/12	All	Initial version

单击下面可查看定价，库存，交付和生命周期等信息

>>2pai semi(荣湃半导体)