Features

- **Universal: Dual Low-Side, Dual High-Side or Half-Bridge Driver**
- **Operating Temperature Range –40 to +125°C**
- **Switching Parameters:**
  - **5-ns Maximum Delay Matching**
  - **8-ns Maximum Pulse-Width Distortion**

  Pai825XB/C/E：
  - **19-ns Typical Propagation Delay**
  - **10-ns Minimum Pulse Width**

  Pai825XA/D/F：
  - **90-ns Typical Propagation Delay**
  - **50-ns Minimum Pulse Width**
- **Common-Mode Transient Immunity (CMTI)**

  Pai825XB/C/E：100kV/us

  Pai825XA/D/F：300kV/us
- **Isolation Barrier Life >40 Years**
- **4-A Peak Source, 8-A Peak Sink Output**
- **TTL and CMOS Compatible Inputs**
- **3V to 5.5V Input VCCI Range to Interface with Both Digital and Analog Controllers**
- **Up to 25V VDD Output Drive Supply**
- **Fast Disable for Power Sequencing**
- **Safety-Related Certifications: (Pending)**
  - **5000V_{PK} Basic Isolation per DIN V VDE V 0884-11:2017-01**
  - **5kV_{RMS} Isolation for 1 Minute per UL 1577**
  - **CSA Certification per IEC 60950-1, IEC 62368-1, IEC 61010-1 and IEC 60601-1 End Equipment Standards**
  - **CQC Certification per GB4943.1-2011**
- **RoHS-compliant, NB SOIC-16 and WB SOIC-14**

Applications

- **HEV and BEV Battery Chargers**
- **Isolated Converters in DC-DC and AC-DC Power Supplies**
- **Server, Telecom, IT and Industrial Infrastructures**
- **Motor Drive and DC-to-AC Solar Inverters**
- **LED Lighting**
- **Inductive Heating**
- **Uninterruptible Power Supply (UPS)**

General Description

The Pai8252X/Pai8253X are the dual-channel isolated gate drivers based on *iDivider®* technology of 2Pai Semi. It has a source peak current of 4A and a sink peak current of 8A. The maximum switching frequency can reach 5MHz. It is suitable for gate drive of MOSFET, IGBT and SiC MOSFET.

The input side is isolated from the two output sides by an isolation barrier that can withstand 5kV_{RMS} isolation voltage, and the typical common-mode transient immunity (CMTI) capability is 300kV/us. The internal functional isolation between the two secondary side drivers allows a maximum operating voltage of 1200V_{DC}.

Every driver can be configured as two low-side drivers or two high-side drivers. A disable pin shuts down both outputs simultaneously when it is set high and allows normal operation when left open or grounded. As a fail-safe measure, primary-side logic failures force both outputs low.

Each device accepts VDD supply voltages up to 25V. A wide input VCCI range from 3V to 5.5V makes the driver suitable for interfacing with both analog and digital controllers. All the supply voltage pins have under voltage lock-out (UVLO) protection.

Functional Block Diagram

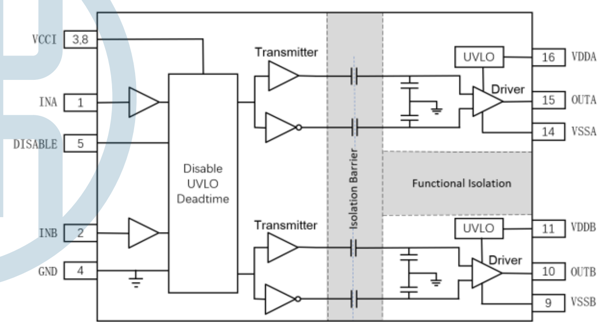

Fig 1. Functional Block Diagram

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021-50850681

http://www.rpsemi.com/

1. Pin Configurations and Functions

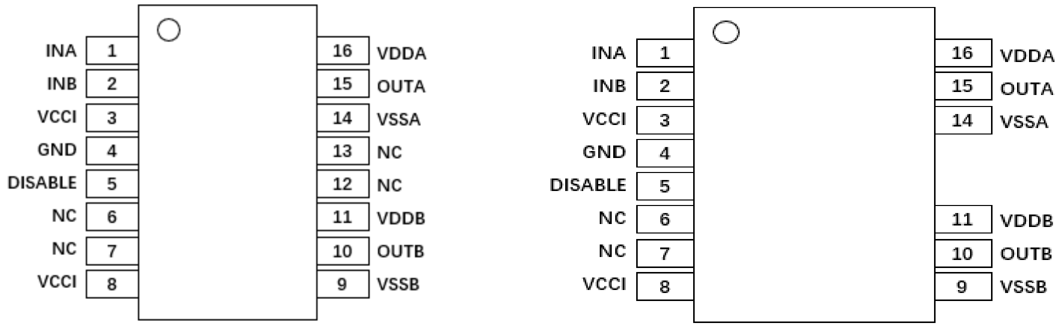


Fig 2. Pin Configuration

Table 1. Pin Function Descriptions

PIN NAME	NB SOIC-16	WB SOIC-14	DESCRIPTION
INA	1	1	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
INB	2	2	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
VCCI	3,8	3,8	Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible.
GND	4	4	Primary-side ground reference. All signals in the primary side are referenced to this ground.
DISABLE	5	5	Disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open. If this pin is not used, it is recommended to ground this pin to obtain better noise immunity. When connecting to a microcontroller, use a low ESR/ESL capacitor of approximately 1nF to bypass the DIS pin.
NC	6,7,12,13	6,7	No Internal connection.
VSSB	9	9	Ground for secondary-side driver B. Ground reference for secondary side B channel.
OUTB	10	10	Output of driver B. Connect to the gate of the B channel FET or IGBT.
VDDB	11	11	Secondary-side power for driver B. Locally decoupled to VSSB using low ESR/ESL capacitor located as close to the device as possible.
VSSA	14	14	Ground for secondary-side driver A. Ground reference for secondary side A channel.
OUTA	15	15	Output of driver A. Connect to the gate of the A channel FET or IGBT.
VDDA	16	16	Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible.

2. Specifications

2.1.Absolute Maximum Ratings

Table 2.Absolute Maximum Ratings (1)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input power supply voltage	VCCI to GND	–0.6	7	V
Driver bias supply	VDDA-VSSA, VDDB-VSSB	–0.4	30	V
Input signal voltage	INA, INB, DIS to GND	–0.6	VCCI+0.5	V
Input signal voltage	INA, INB Transient for 50ns	–5	VCCI+0.5	V
Output signal voltage	OUTA to VSSA, OUTB to VSSB	–0.4	VDDA+0.5, VDDB+0.5	V
Output signal voltage	OUTA to VSSA, OUTB to VSSB, Transient for 200 ns	–2	VDDA+0.5, VDDB+0.5	V
Channel to channel voltage	VSSA-VSSB, VSSB-VSSA NB SOIC-16 Package	–1500	1500	V
	VSSA-VSSB, VSSB-VSSA WB SOIC-14 Package	–1500	1500	V
Junction temperature, T_J (2)	T_J	–40	150	℃
Storage temperature, T_{stg}	T_{stg}	–65	150	℃

1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2) To maintain the recommended operating conditions for T_J, see the Thermal Information.

2.2.ESD Caution

ESD(Electrostatic Discharge) Sensitive device

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

2.3.Recommended Operating Conditions

Table 3.Over operating free-air temperature range (unless otherwise noted)

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VCCI	VCCI Input supply voltage	3	5.5	V
VDDA-VSSA, VDDB-VSSB	Driver output bias supply---6V Version	6.5	25	V
	Driver output bias supply---9V Version	9.2	25	V
	Driver output bias supply---12V Version	13.7	25	V
VIA-GND, VIB-GND, DISABLE-GND,	Input voltage	0	V_{CCI}	V
VOA-VSSA, VOB-VSSB	Output voltage	0	VDDA/VDDB	V
VSSA-VSSB/VSSA-GND/VSSB-GND	Channel to channel working voltage	-1200	1200	V
t_{INA}, t_{INB}	B/C/E Valid pulse width	10	/	ns
	A/D/F Valid pulse width	50	/	ns
T_A	Ambient Temperature under Bias	-40	125	℃
T_J	Junction Temperature	-40	130	°C

2.4.Thermal Information

Table 4.Thermal Information

SYMBOL	PARAMETER	TYP		Unit
		NB SOIC-16	WB SOIC-14	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105	101	°C/W

2.5.Power Ratings

Table 5.Thermal Information

VCCI = 3.3 V, Pai825XA/B/C/D VDDA/B = 12 V, Pai825XE/F VDDA/B = 15 V INA/B = 3.3 V, 2MHz 50% duty cycle square wave 1nF load

SYMBOL	PARAMETER	VALUE		UNIT
		NB SOIC-16	WB SOIC-14	
PD	Power dissipation	0.703	0.703	W
PDI	Power dissipation by transmitter side	0.003	0.003	W
PDA, PDB	Power dissipation by each driver side	0.35	0.35	W

3. Insulation Specifications

Table 6.Insulation Specifications

PARAMETER	DESCRIPTION	TEST CONDITIONS	VALUE		UNIT
			NB SOIC-16	WB SOIC-14	
CLR	External clearance	Shortest pin-to-pin distance through air	> 4	> 8	mm
CPG	External creepage	Shortest pin-to-pin distance across the package surface	> 4	> 8	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 10.5 µm)	>21	>21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 400	> 400	V
Material group	Material group	According to IEC 60664-1	II	II	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤150 VRMS	I-IV	I-IV	
		Rated mains voltage ≤ 300 VRMS	I-III	I-IV	
		Rated mains voltage ≤ 600 VRMS	I-II	I-IV	
		Rated mains voltage ≤ 1000 VRMS	/	I-III	

Table 7.DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01

PARAMETER	DESCRIPTION	TEST CONDITIONS	VALUE		UNIT
			NB SOIC-16	WB SOIC-14	
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1200	1200	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave)	848	848	V_{RMS}
		DC voltage	1200	1200	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 sec (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	4242	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	5000	5000	V_{PK}

PARAMETER	DESCRIPTION	TEST CONDITIONS	VALUE		UNIT
			NB SOIC-16	WB SOIC-14	
q_{pd}	Apparent charge	Method a, After Input/Output safety test subgroup 2/3. $V_{ini} = V_{IOTM}$, $t_{ini} = 60s$; $V_{pd(m)} = 1.2 X V_{IORM}$, $t_m = 10s$	<5	<5	pC
		Method a, After environmental tests subgroup 1. $V_{ini} = V_{IOTM}$, $t_{ini} = 60s$; $V_{pd(m)} = 1.3 X V_{IORM}$, $t_m = 10s$	<5	<5	pC
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$; $t_{ini} = 1s$; $V_{pd(m)} = 1.5 * V_{IORM}$, $t_m = 1s$	<5	<5	pC
C_{IO}	Barrier capacitance, input to output	$V_{IO} = 0.4 \sin(2\pi ft)$, f =1 MHz	1.2	1.2	pF
R_{IO}	Isolation resistance, input to output	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	> 10^{11}	Ω
		V_{IO} = 500 V at T_S =150°C	> 10^{9}	> 10^{9}	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

Table 8.UL 1577

PARAMETER	DESCRIPTION	TEST CONDITIONS	VALUE		UNIT
			NB SOIC-16	WB SOIC-14	
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 sec.(qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 sec (100% production)	3000	5000	V_{RMS}

3.1.Safety-Related Certifications

Table 9.Safety-Related Certifications (Pending)

REGULATORY	NB SOIC-16	WB SOIC-14
CQC	Certified according to GB 4943.1-2011 Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate 660 V_{RMS} maximum working voltage. File（Pending）	Certified according to GB 4943.1-2011 Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate 660 V_{RMS} maximum working voltage. File（Pending）
UL	Recognized under UL 1577 Component Recognition Program Single protection, 3000V_{RMS} File（Pending）	Recognized under UL 1577 Component Recognition Program Single protection, 5000V_{RMS} File（Pending）
VDE	Certified according to DIN V VDE V 0884-11:2017-01, and DIN EN 60950-1 (VDE 0805 Teil 1):2014-08 V_{IOTM} =4242V_{PK}; V_{IORM} =1200V_{PK}; V_{IOSM} =5000 V_{PK} File（Pending）	Certified according to DIN V VDE V 0884-11:2017-01, and DIN EN 60950-1 (VDE 0805 Teil 1):2014-08 V_{IOTM} =7071V_{PK}; V_{IORM} =1200V_{PK}; V_{IOSM} =5000 V_{PK} File（Pending）

3.2.Safety-Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

Table 10.Safety-Limiting Values

SYMBOL	PARAMETER	TEST CONDITIONS	SIDE	MAX		UNIT
				NB SOIC-16	WB SOIC-14	
I_S	Safety output supply current	$R_{\theta JA}$ = 101℃/W, VDDA/B = 12 V, T_A = 25°C, T_J = 150°C	Driver A Driver B	50	50	mA
		$R_{\theta JA}$ =101℃/W, VDDA/B = 25 V, T_A = 25℃, T_J = 150℃	Driver A Driver B	24	24	mA
P_S	Safety supply power	$R_{\theta JA}$ = 101℃/W, T_A = 25℃, T_J = 150℃	TOTAL	1200	1200	mW
T_S	Safety temperature[1]			150	150	°C

1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

4. Truth table

Table 11.Truth table

INPUT		DISABLE	VCCI/VDDA/VDDB Condition			OUTPUT	
INA	INB		VCCI	VDDA	VDDB	VOA	VOB
L	L	L or Left Open	Powered	Powered	Powered	L	L
L	H	L or Left Open	Powered	Powered / Unpowered	Powered	L	H
H	L	L or Left Open	Powered	Powered	Powered / Unpowered	H	L
H	H	L or Left Open	Powered	Powered	Powered	H	H
X[1]	X[1]	H	Powered	Powered	Powered	L	L
L	L	L or Left Open	Unpowered	Powered	Powered	L	L

Notes：
1) "X" means L, H or left open.

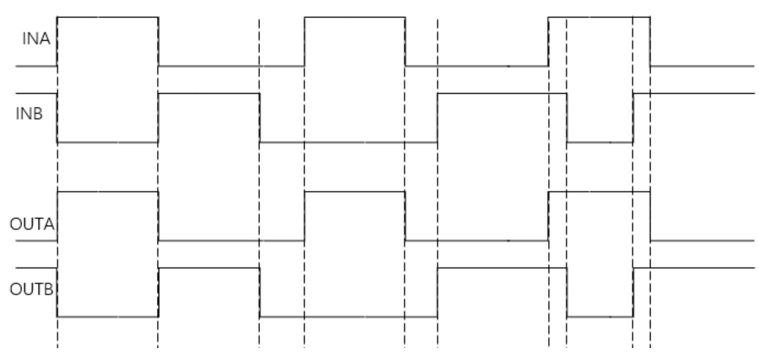


Fig 3.Input/Output Timing Diagram

5. Specifications

5.1.Electrical Characteristics

Table 12.ELECTRICAL CHARACTERISTICS

VCCI = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, Pai825XA/B/C/D VDDA = VDDB = 12 V, Pai825XE/F VDDA = VDDB = 15V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, T_A = −40 to +125℃, (unless otherwise noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VCCI}	VCCI quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		0.5	1.1	mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB quiescent current	V_{INA} = 0 V, V_{INB} = 0 V		0.9	1.5	mA
I_{VCCI}	VCCI operating current	VINA, VINB input signal f = 500 kHz, 50% duty cycle, each channel load capacitance 100 pF ± 20%, including the input capacitance of the measuring instrument.		0.9		mA
I_{VDDA}, I_{VDDB}	VDDA and VDDB operating current			2.2		mA
V_{VCCI_ON}	VCCI UVLO Rising threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	VCCI UVLO Falling threshold		2.35	2.5	2.65	V
V_{VCCI_HYS}	UVLO Threshold hysteresis			0.2		V
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold---9V Version (Pai8252A/C, Pai8253A/C)		8.3	8.7	9.2	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold---9V Version (Pai8252A/C, Pai8253A/C)		7.8	8.2	8.7	V
V_{VDDA_HYS} V_{VDDB_HYS}	UVLO Threshold hysteresis---9V Version (Pai8252A/C, Pai8253A/C)			0.5		V
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold---6V Version (Pai8252B/D, Pai8253B/D)		5.7	6.1	6.5	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold---6V Version (Pai8252B/D, Pai8253B/D)		5.4	5.8	6.2	V
V_{VDDA_HYS} V_{VDDB_HYS}	UVLO Threshold hysteresis---6V Version (Pai8252B/D, Pai8253B/D)			0.3		V
V_{VDDA_ON}, V_{VDDB_ON}	UVLO Rising threshold---12V Version (Pai8253E/F)		11.9	12.8	13.7	V
V_{VDDA_OFF}, V_{VDDB_OFF}	UVLO Falling threshold---12V Version (Pai8253E/F)		10.9	11.8	12.7	V
V_{VDDA_HYS} V_{VDDB_HYS}	UVLO Threshold hysteresis---12V Version (Pai8253E/F)			1.0		V
V_{INAH}, V_{INBH}, V_{DISH}	Input high threshold voltage		1.6	1.8	2	V
V_{INAL}, V_{INBL}, V_{DISL}	Input low threshold voltage		0.8	1	1.2	V
V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}	Input threshold hysteresis			0.8		V
V_{INA}, V_{INB}	Negative transient, ref to GND, 50 ns pulse	Not production tested, bench test only	−5			V
I_{OA+}, I_{OB+}	Pai8253A/B/C/D/E/F Peak output source current	C_{VDD} = 10 µF, C_{LOAD} = 0.68 µF, f= 100Hz, bench measurement		4		A
	Pai8252A/B/C/D Peak output source current			2		
I_{OA-}, I_{OB-}	Pai8253 A/B/C/D/E/F Peak output sink current			8		A
	Pai8252 A/B/C/D Peak output sink current			4		
R_{OHA}, R_{OHB}	Output resistance at high state	I_{OUT} = –10 mA, TA = 25°C, R_{OHA}, R_{OHB} do not represent drive pull-up performance. See t_{RISE} in Switching Characteristics and Output Stage for details.		1		Ω
R_{OLA}, R_{OLB}	Output resistance at low state	IOUT = 10 mA, TA = 25°C		0.4		Ω
V_{OHA}, V_{OHB}	Output voltage at high state	VDDA, VDDB = 15 V, IOUT = –10 mA, TA = 25°C		14.99		V
V_{OLA}, V_{OLB}	Output voltage at low state	VDDA, VDDB = 15 V, IOUT = 10 mA, TA = 25°C		4		mV

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{JF}	Junction Temperature Shutdown, Falling Edge			140		°C
T_{JR}	Junction Temperature Shutdown, Rising Edge			150		°C

5.2. Switching Characteristics

Table 13.Switching Characteristics

VCCI = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, Pai825XA/B/C/D VDDA = VDDB = 12 V, Pai825XE/F VDDA = VDDB = 15V, 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, no load, TA = –40°C to +125°C, (unless otherwise noted).

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	C_{OUT} = 1.8 nF		7	18	ns
t_f	Output fall time	C_{OUT} = 1.8 nF		8	12	ns
t_{PWmin}	Minimum pulse width	Output off for less than minimum, C_{OUT} = 0 pF		10	20	ns
t_{PDHL}	Pai825XB/C/E Propagation delay from INx to OUTx falling edges[1]		14	19	30	ns
t_{PDLH}	Pai825XB/C/E Propagation delay from INx to OUTx rising edges[1]		14	19	30	ns
t_{PWD}	Pai825XB/C/E Pulse width distortion $\|t_{PDLH} – t_{PDHL}\|$[1]				5	ns
t_{PDHL}	Pai825XA/D/F Propagation delay from INx to OUTx falling edges[1]		60	90	150	ns
t_{PDLH}	Pai825XA/D/F Propagation delay from INx to OUTx rising edges[1]		60	90	150	ns
t_{PWD}	Pai825XA/D/F Pulse width distortion $\|t_{PDLH} – t_{PDHL}\|$[1]				8	ns
t_{DM}	Propagation delays matching between VOUTA, VOUTB	f = 100 kHz			5	ns
$\|CM_H\|$	Pai825XB/C/E High-level common-mode transient immunity[1]	INA and INB both are tied to VCCI; V_{CM}=1000V;		100		kV/us
$\|CM_L\|$	Pai825XB/C/E Low-level common-mode transient immunity[1]	INA and INB both are tied to GND; V_{CM}=1000V;		100		kV/us
$\|CM_H\|$	Pai825XA/D/F High-level common-mode transient immunity[1]	INA and INB both are tied to VCCI; V_{CM}=1000V;	300			kV/us
$\|CM_L\|$	Pai825XA/D/F Low-level common-mode transient immunity[1]	INA and INB both are tied to GND; V_{CM}=1000V;	300			kV/us
t_{SD}	Pai825XB/C/E Shutdown Time from Disable True[1]				40	ns
$t_{RESTART}$	Pai825XB/C/E Restart Time from Disable False[1]				40	ns
t_{SD}	Pai825XA/D/F Shutdown Time from Disable True[1]				150	ns
$t_{RESTART}$	Pai825XA/D/F Restart Time from Disable False[1]				150	ns
t_{START}	Device Start-up Time	Time from VDD_ = VDD_UV+ to VOA, VOB = VIA, VIB			100	µs

1) "X" in part number means Ipk. 2 for 2A/4A, 3 for 4A/8A

5.3.Insulation Characteristics Curves

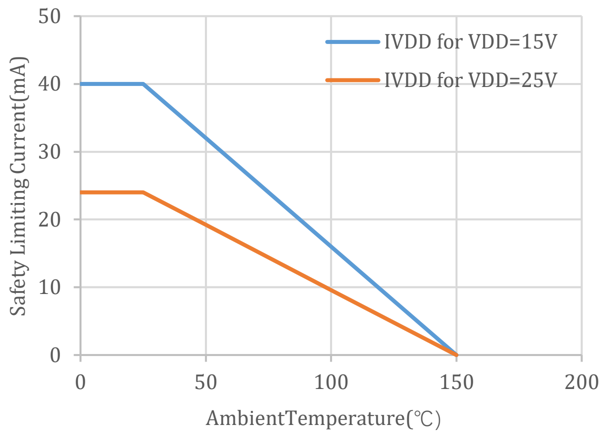


Fig 4.Thermal Derating Curve for Limiting Current Per VDE

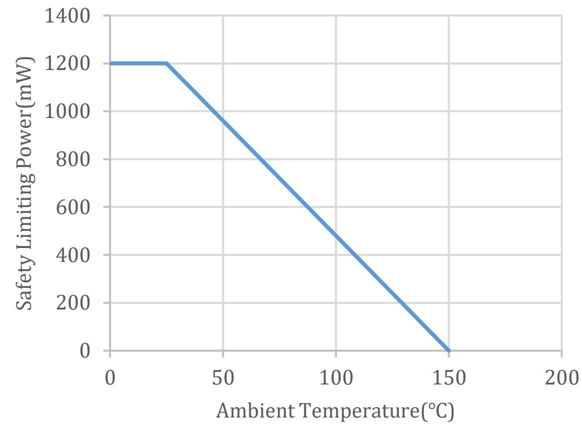


Fig 5.Thermal Derating Curve for Limiting Power Per VDE

5.4.Typical Characteristics

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load, unless otherwise noted.

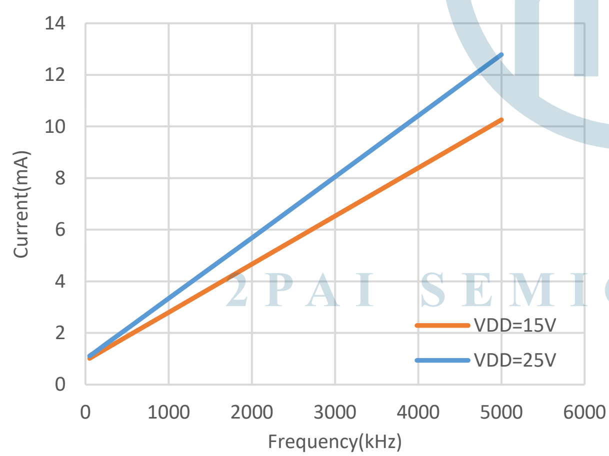


Fig 6.Per Channel Current ($I_{VDDA/B}$) (No load)

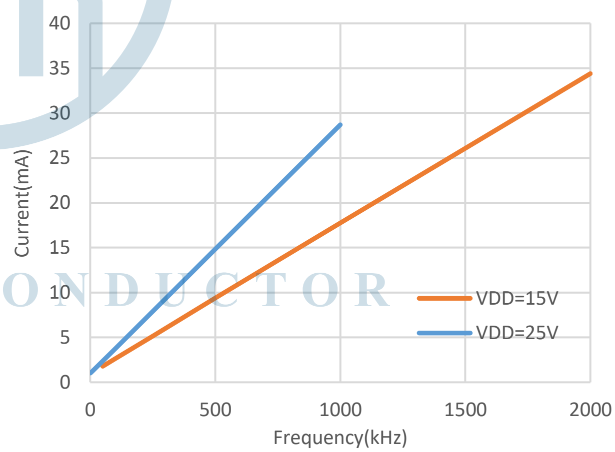


Fig 7.Per Channel Current ($I_{VDDA/B}$) (1nF Load)

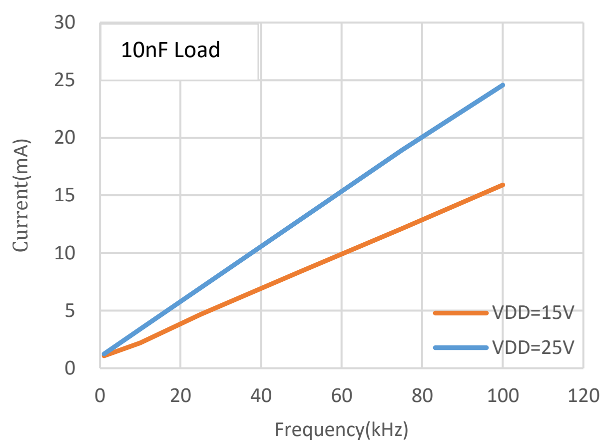


Fig 8.Per Channel Current ($I_{VDDA/B}$) (10nF Load)

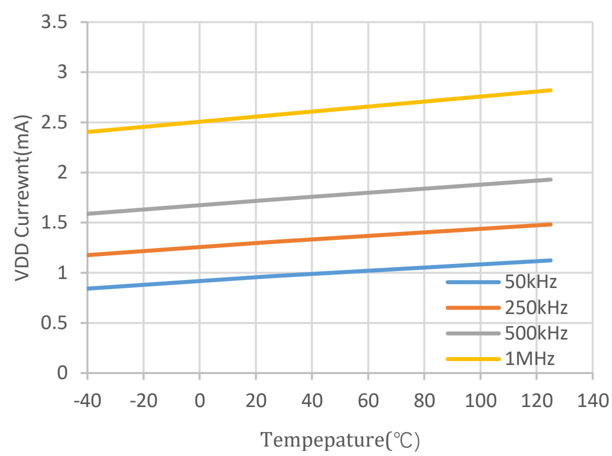


Fig 9. Per Channel Current ($I_{VDDA/B}$) (No Load)

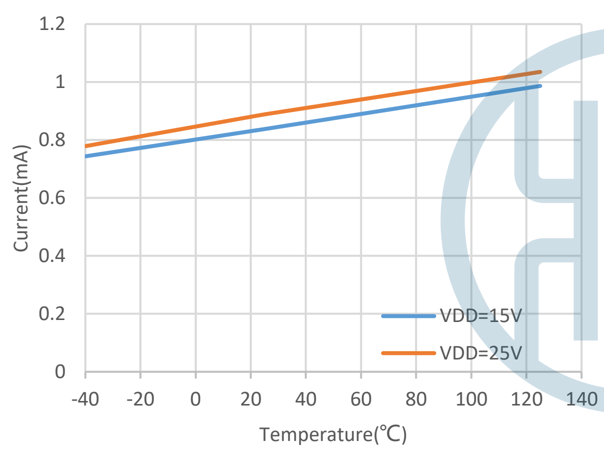


Fig 10.Per Channel Quiescent Current ($I_{VDDA/B}$)

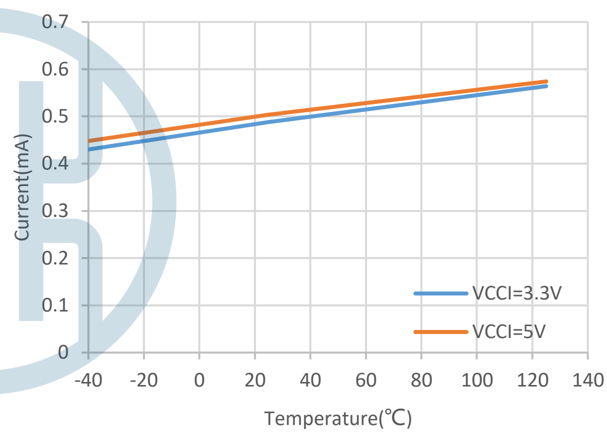


Fig 11.I_{VCCI} Quiescent Current

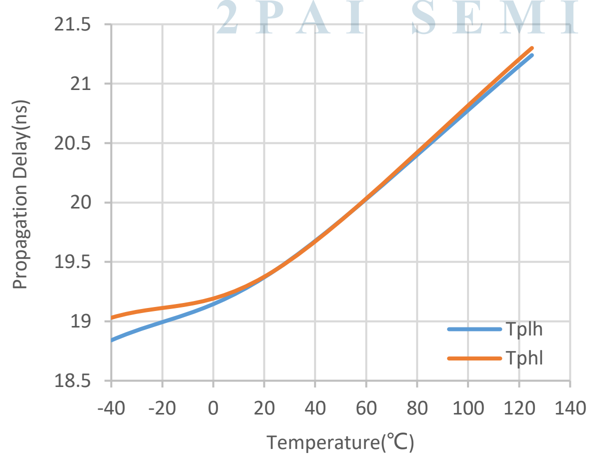


Fig 12.Pai8253B/C/E Propagation Delay

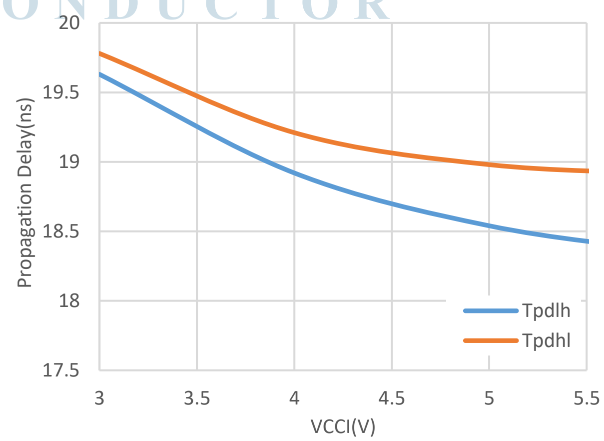


Fig 13.Pai8253B/C/E Propagation Delay

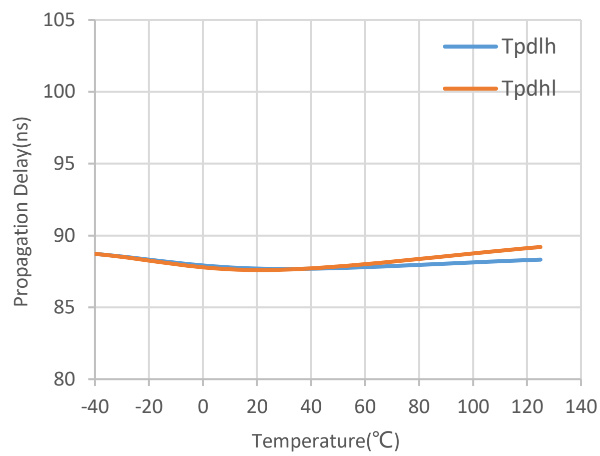


Fig 14.Pai8253A/D/F Propagation Delay

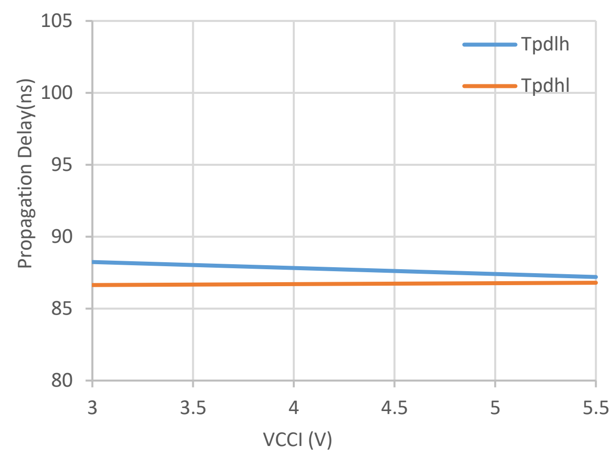


Fig 15.Pai8253A/D/F Propagation Delay

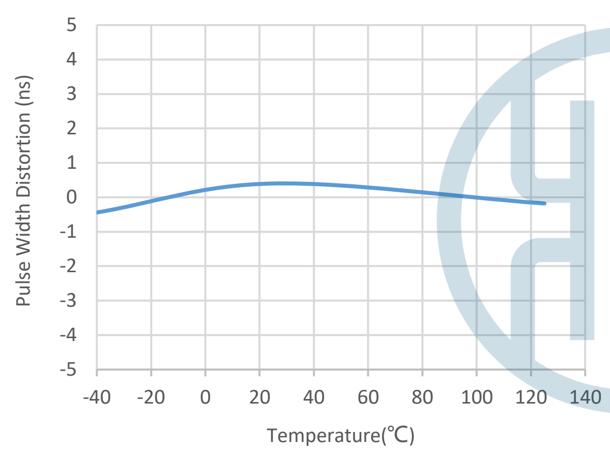


Fig 16.Pulse Width Distortion

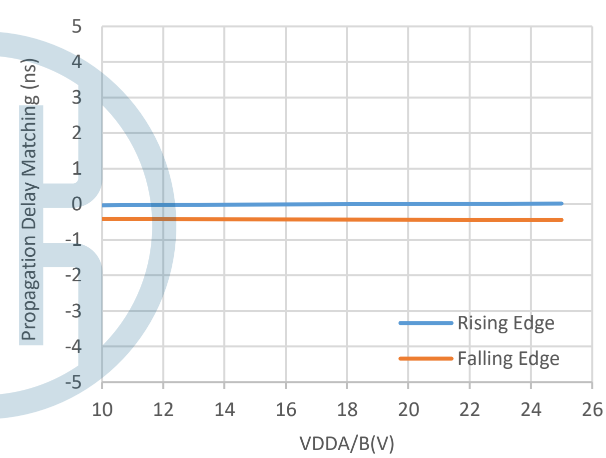


Fig 17.Propagation Delay Matching (t_{DM})

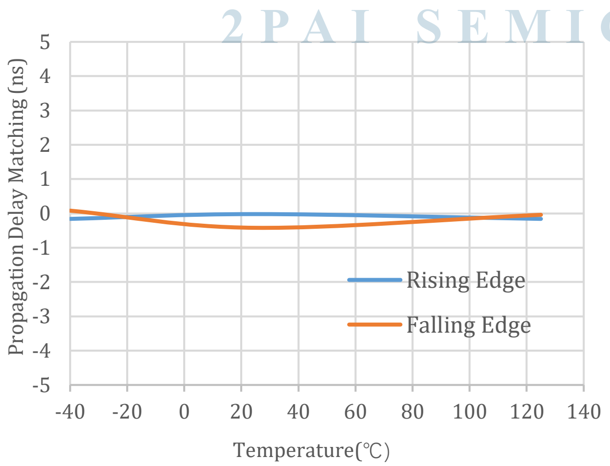


Fig 16.Propagation Delay Matching (t_{DM})

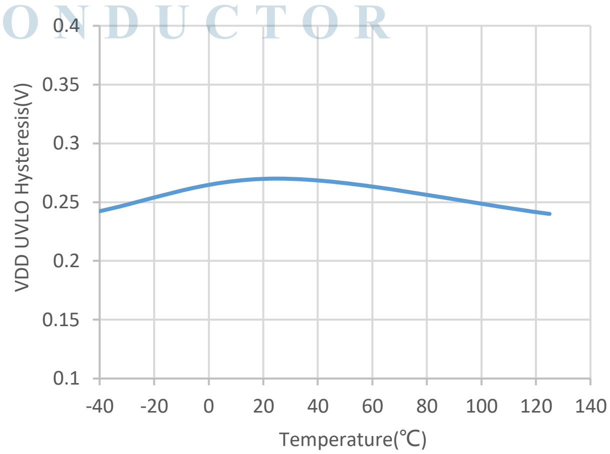


Fig 19.VDD 6-V UVLO Hysteresis

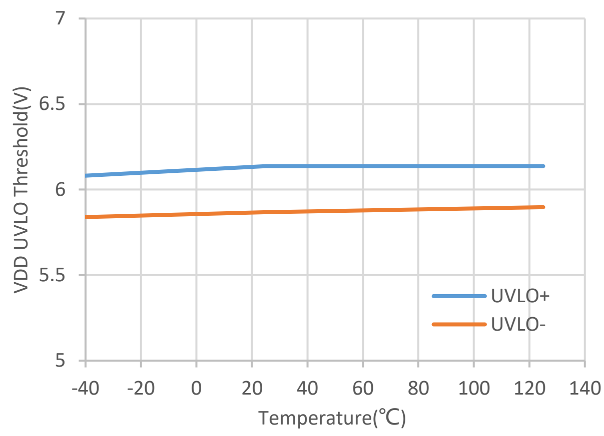


Fig 20.VDD 6-V UVLO Threshold vs. Temperature

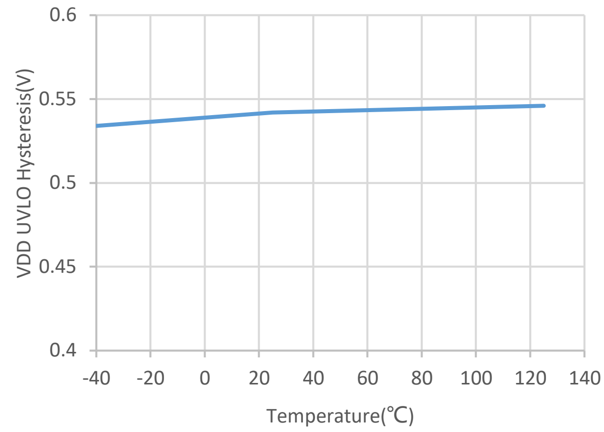


Fig 21.VDD 9-V UVLO Hysteresis

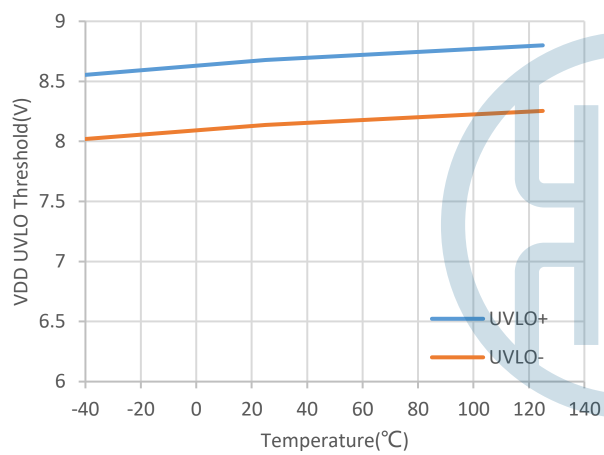


Fig 22.VDD 9-V UVLO Threshold vs. Temperature

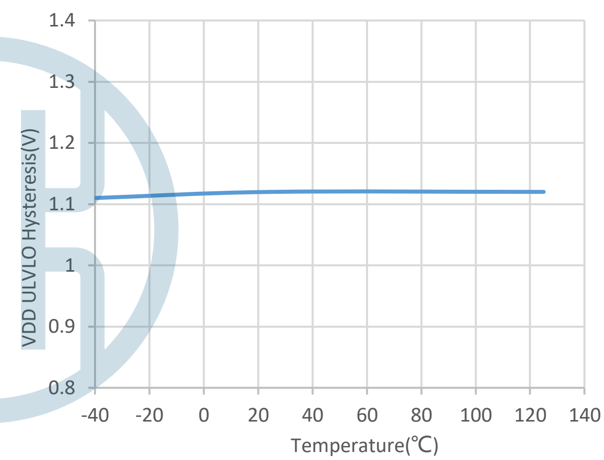


Fig 23.VDD 12-V UVLO Hysteresis

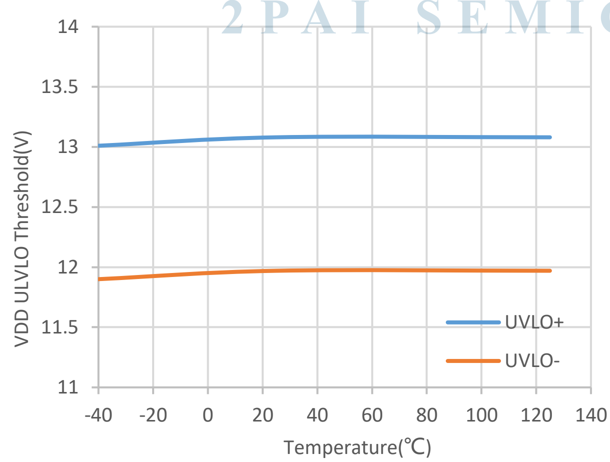


Fig 24.VDD 12-V UVLO Threshold vs. Temperature

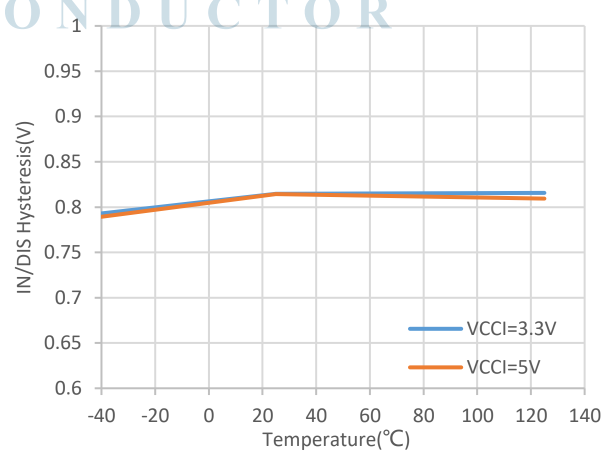


Fig 25.IN/DIS Hysteresis

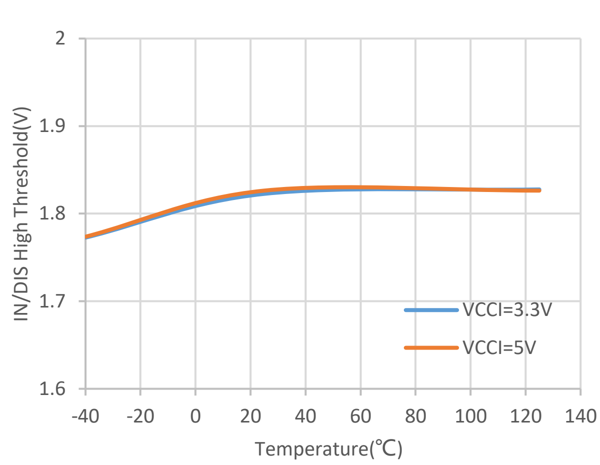


Fig 26.IN/DIS High Threshold (rise)

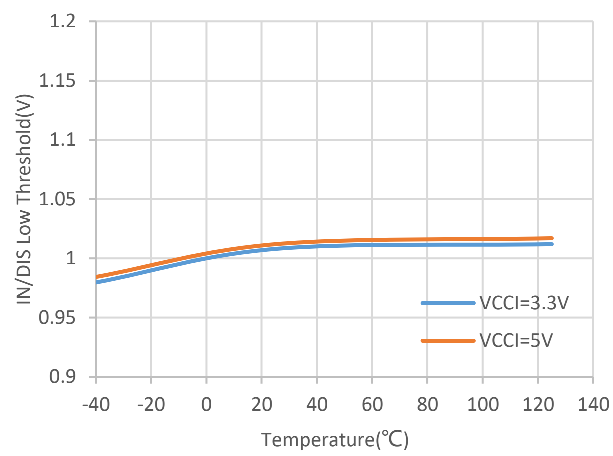


Fig 27.IN/DIS Low Threshold (fall)

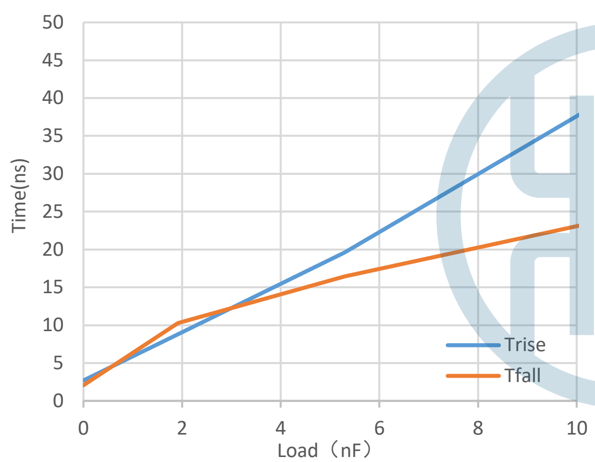


Fig 28.Rising and Falling Time

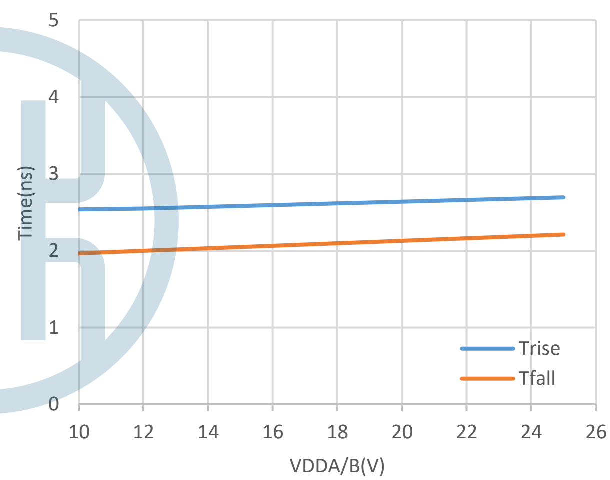


Fig 29.Rise/Fall Time

6. Parameter Measurement Information

6.1.Propagation Delay Matching and Pulse Width Distortion

Fig shows how to calculate pulse width distortion(t_{PWD})and delay matching (t_{DM}) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase.

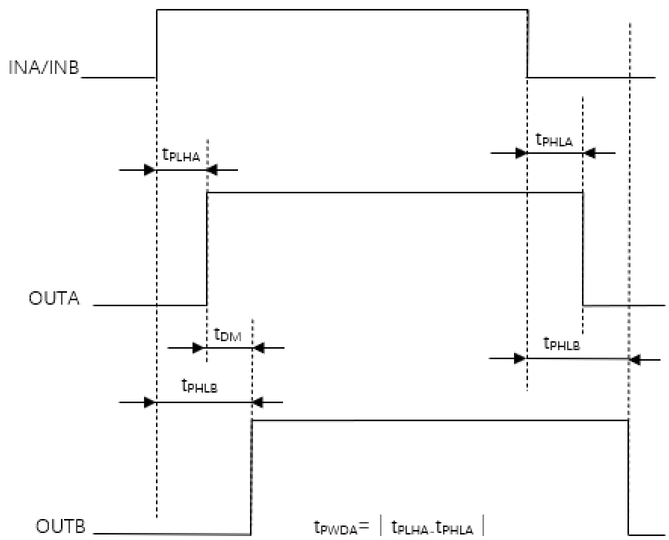


Fig 30.Overlapping inputs, Dead Time Disable

6.2.Rising and Falling Time

Fig shows the criteria for measuring rising (t_r) and falling (t_f) times.

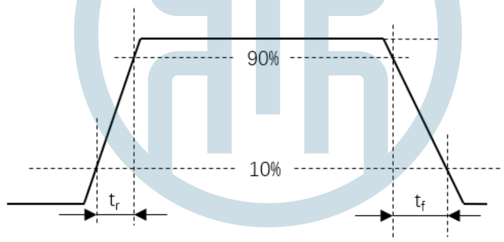


Fig 31.Rising and Falling Time Criteria

6.3.Input and Disable Response Time

Fig shows the response time of the disable function. It is recommended to bypass using a 1nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance.

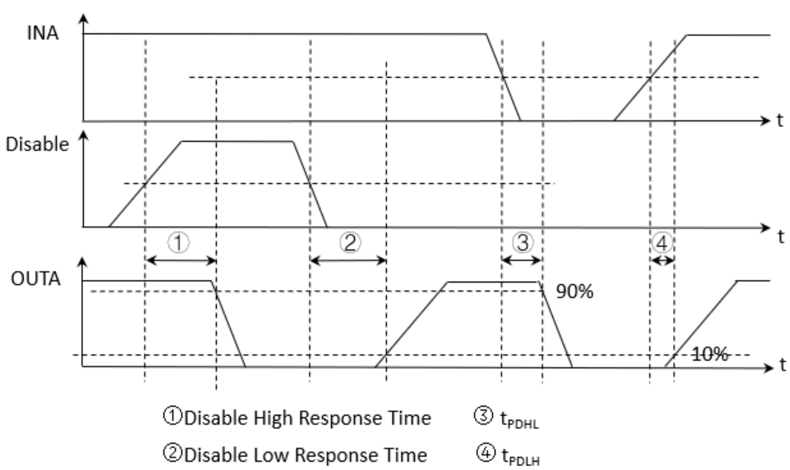


Fig 32.Disable Pin Timing

6.4.Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+\ to\ OUT}$ for VCCI UVLO (typically 40us) and $t_{VDD+\ to\ OUT}$ for VDD UVLO (typically 45us). It is recommended to consider proper margin before launching PWM signal after the driver's VCCI and VDD bias supply is ready. Fig 33 and Fig 34 show the power up UVLO delay timing diagram for VCCI and VDD.

If INA or INB are active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until $t_{VCCI+\ to\ OUT}$ or $t_{VDD+\ to\ OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is <1µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

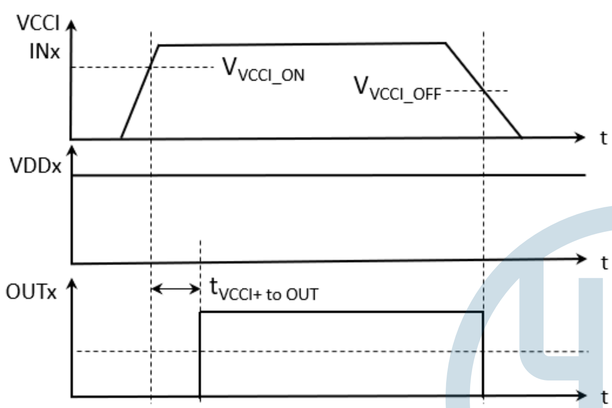


Fig 33.VCCI Power-up UVLO Delay

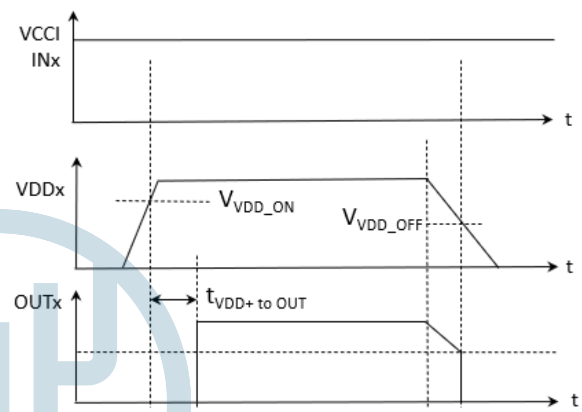


Fig 34.VDDA/B Power-up UVLO Delay

6.5.CMTI Testing

Fig is a simplified diagram of the CMTI test configuration.

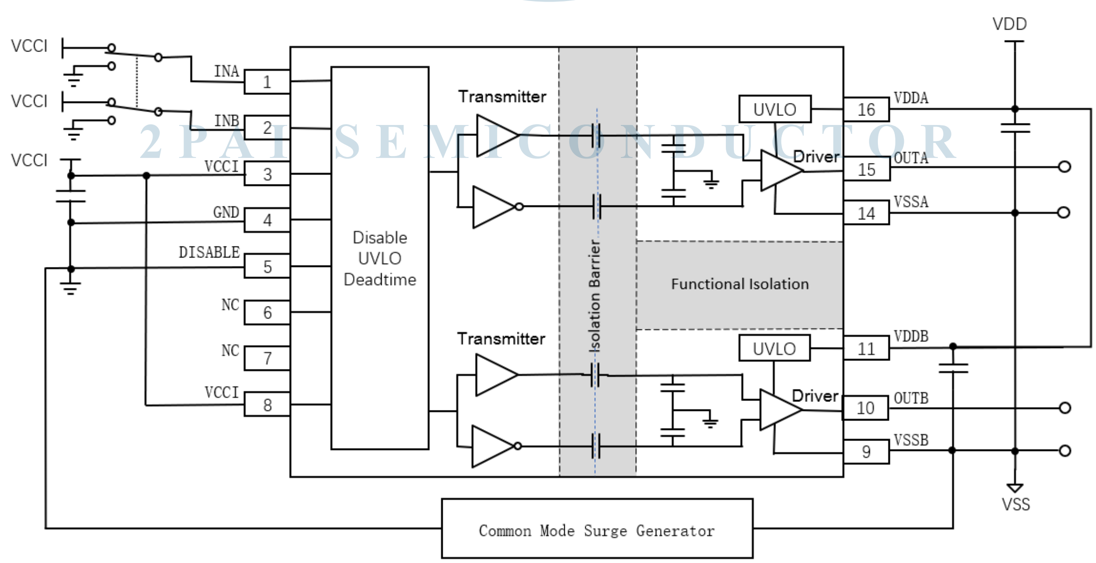


Fig 35.simplified CMTI test setup

7. Detailed Description

7.1.Overview

The Pai8252X/Pai8253X are flexible dual-channel gate drivers. The Pai8252X/Pai8253X have many functions that can make it well integrated with the control circuit and protect the drove devices, such as DISABLE function and undervoltage lockout (UVLO) function. When the input remains open or the input pulse width is insufficient, Pai8252X/Pai8253X keeps its output low.

7.2.Feature Description

7.2.1. VDD, VCCI, and Under Voltage Lock Out (UVLO)

The Pai8252X/Pai8253X have under-voltage protection (UVLO) function in primary and secondary side. When the VDD voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the effected output low, regardless of the status of the input pins (INA and INB).

Table 14. Pai8252X/Pai8253X VCCI UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L

Table 15. VDDA/B UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDDA/B -VSSA/B < V_{VDD_ON} during device start up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L
VDDA/B -VSSA/B < V_{VDD_OFF} after device start up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L

7.2.2. Input and Output Logic Table

Table 16.INPUT/OUTPUT Logic Table (Assume VCCI, VDDA, VDDB are powered up.)

INPUTS		DISABLE	OUTPUTS	
INA	INB		OUTA	OUTB
L	L	L or Left Open	L	L
L	H	L or Left Open	L	H
H	L	L or Left Open	H	L
H	H	L or Left Open	H	H

INPUTS		DISABLE	OUTPUTS	
INA	INB		OUTA	OUTB
Left Open	Left Open	L or Left Open	L	L
X[1]	X[1]	H	L	L

(1) "X" means L, H or left open.

7.3.Disable Function

Setting the DISABLE pin high shuts down both outputs simultaneously. Grounding (or left open) the DISABLE pin allows the Pai8252X/Pai8253X to operate normally. The DISABLE response time is as fast as propagation delay. The DISABLE pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to ground if the DISABLE pin is not used to achieve better noise immunity, and it is recommended to bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance.

8. Typical Application

Note: The information in this section is for reference only, and 2Pai Semi does not guarantee its accuracy or completeness.

8.1.Solution with bootstrap circuits on secondary side and without negative shutdown voltage

Fig shows a reference design in which the Pai8252X/Pai8253X is set as a typical half-bridge drive configuration. In this design, only one independent power supply is required on the secondary side, but there is no negative voltage shutdown feature. This solution is suitable for small and medium power scenarios.

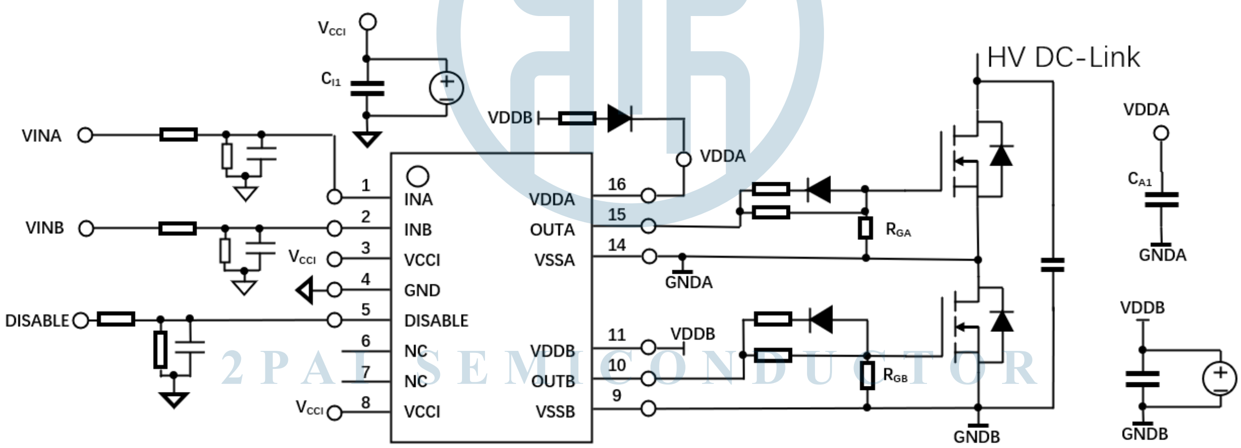


Fig 36.Solution with bootstrap circuits on secondary side and without negative shutdown voltage

8.2. Enhance anti-interference ability solutions with Single power supply and bootstrap circuits for the secondary side

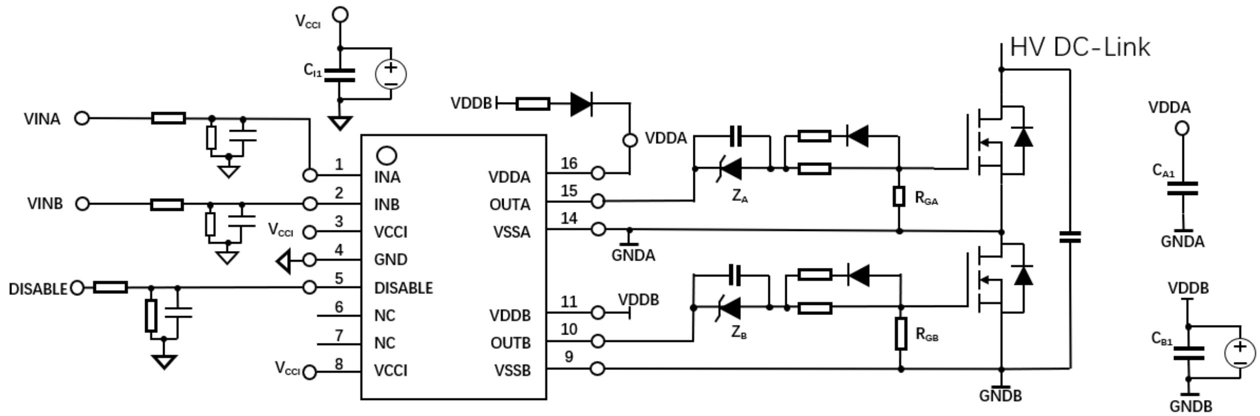


Fig 37.Enhance anti-interference ability solutions with Single power supply and bootstrap circuits for the secondary side

The solution shows in Fig 37 is an improved solution. Only one independent power supply is needed on the secondary side. By adding a Zener diode in the gate drive loop to construct a negative turn-off voltage, the anti-interference ability of the gate is enhanced. This solution has the following limitations:

1) The negative gate bias is not only determined by the Zener diode, but also depends on the duty cycle, which means that when the negative bias duty cycle changes, the negative turn-off voltage will also change.
2) The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means that the low-side switch must be turned on for enough time in each switching cycle.

8.3. Solution with two independent power supplies on the secondary side and a negative turn-off voltage constructed through the Zener diode

When parasitic inductances are introduced by non-ideal PCB layout and long package leads, there would be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

Fig shows the example with negative bias turn-off on the channel A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply VA is equal to 25 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 20 V.

The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration.

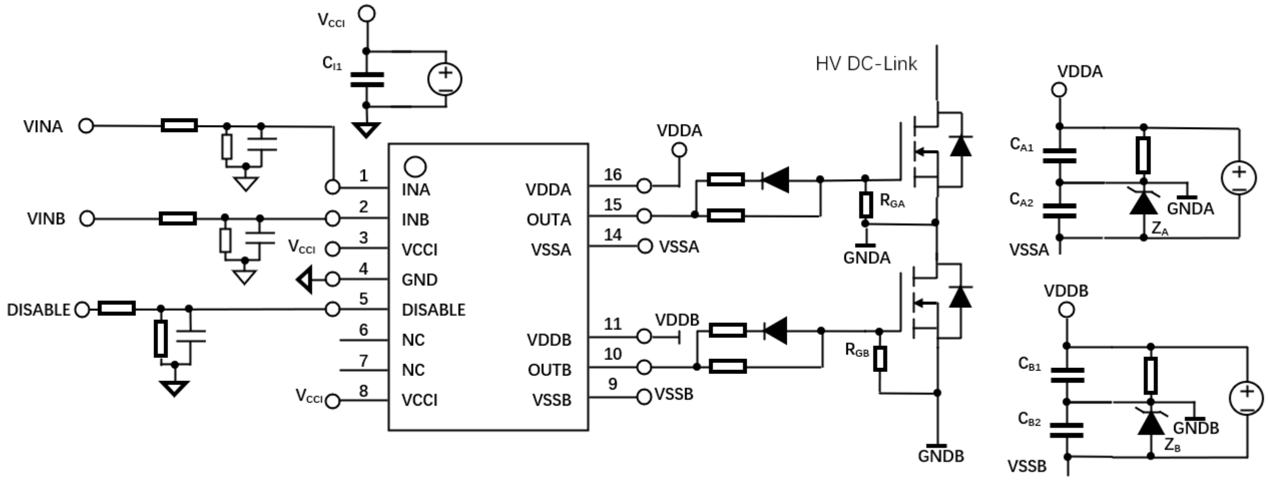


Fig 38.Negative Bias with Zener Diode on Iso-Bias Power Supply Output

8.4.Solution with two independent/four-way power supplies on the secondary side and a negative shutdown voltage

Fig 39 shows a solution with two independent power supplies on the secondary side and a negative turn-off voltage.

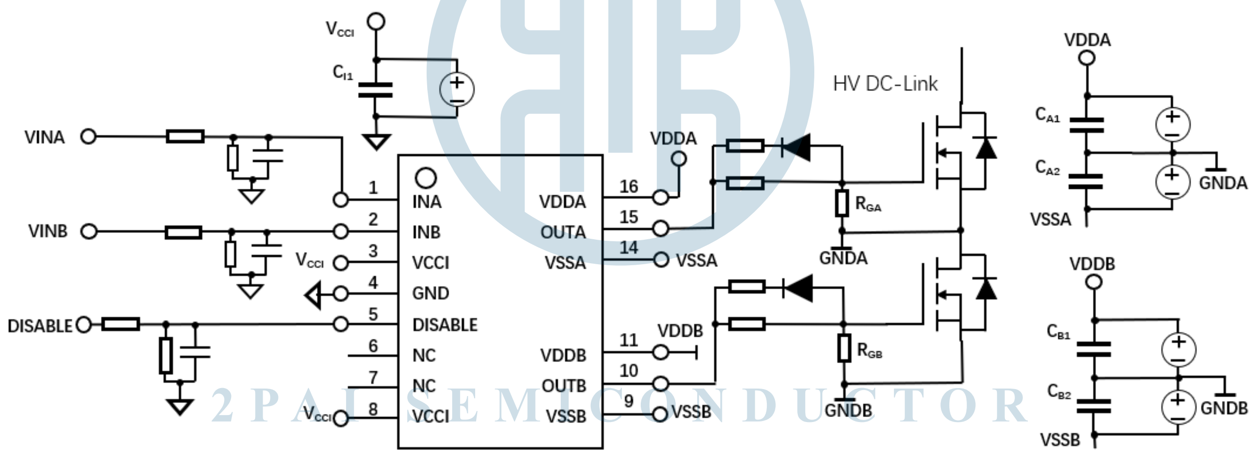


Fig 39.Negative Bias with Two Iso-Bias Power Supplies

9. Outline Dimensions

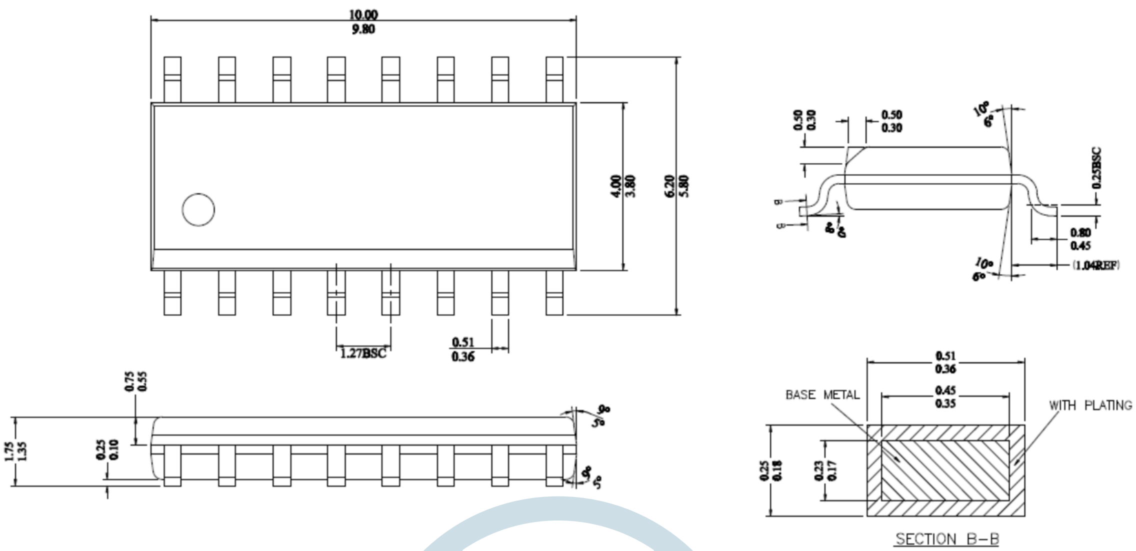
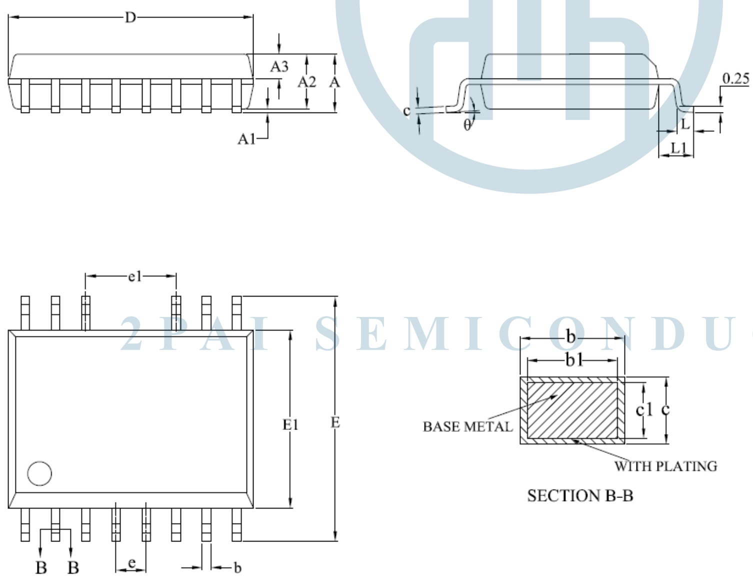


Fig 40.NB SOIC-16 Outline Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.43
b1	0.34	0.37	0.40
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
e1	3.81BSC		
L	0.55	—	0.85
L1	1.40REF		
θ	0	—	8°

Fig 41.WB SOIC4 Outline Package

10. Land Patterns

The Fig 42 illustrates the recommended land pattern details for the Pai8252X/Pai8253X in a 16-pin SOIC package. The table lists the values for the dimensions shown in the illustration.

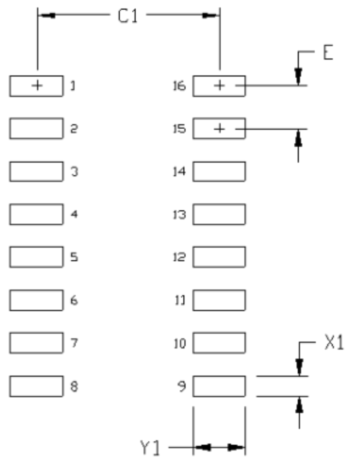


Fig 42.16-Lead SOIC [NB SOIC-16] Land Pattern

Table 17.16-Lead SOIC [NB SOIC-16] Land Pattern Dimensions

DIMENSION	FEATURE	PARAMETER	UNIT
C1	Pad column spacing	5.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.55	mm

Note：
1.This land pattern design is based on IPC -7351
2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

The Fig illustrates the recommended land pattern details for the Pai8252X/Pai8253X in a 14-pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

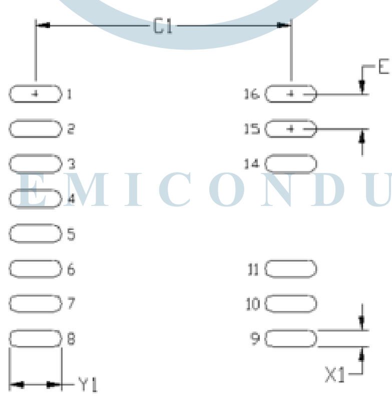


Fig 43.14-Lead Wide Body SOIC [WB SOIC-14] Land Pattern

Table 18.14-Lead Wide Body SOIC [WB SOIC-14] Land Pattern Dimensions

DIMENSION	FEATURE	PARAMETER	UNIT
C1	Pad column spacing	9.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.90	mm

Note：
1.This land pattern design is based on IPC -7351
2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

11. Top Marking

Fig 44.Top Marking

Line 1	PaiXXXXX=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXX, no special meaning

12. Reel Information

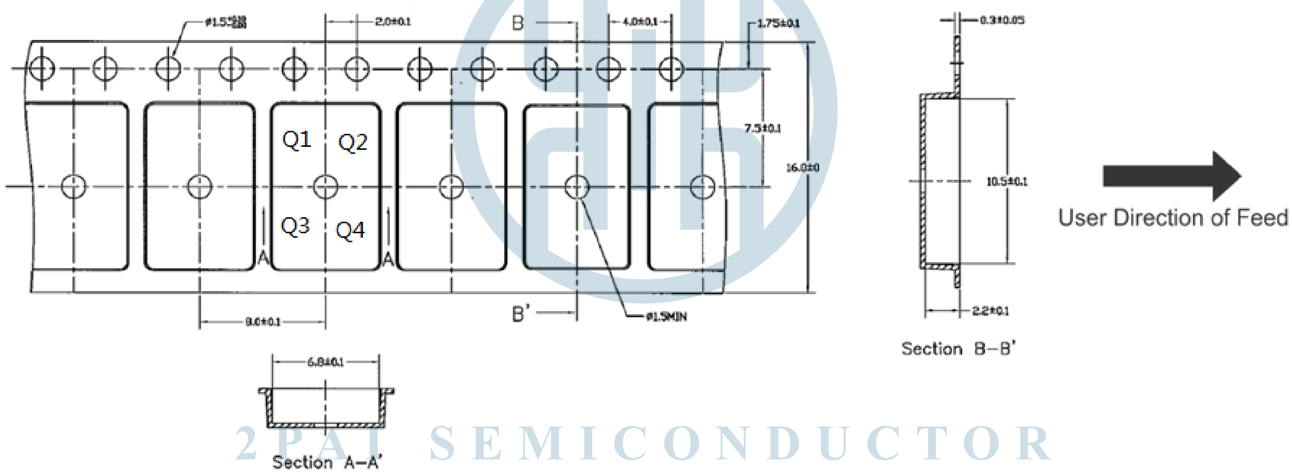
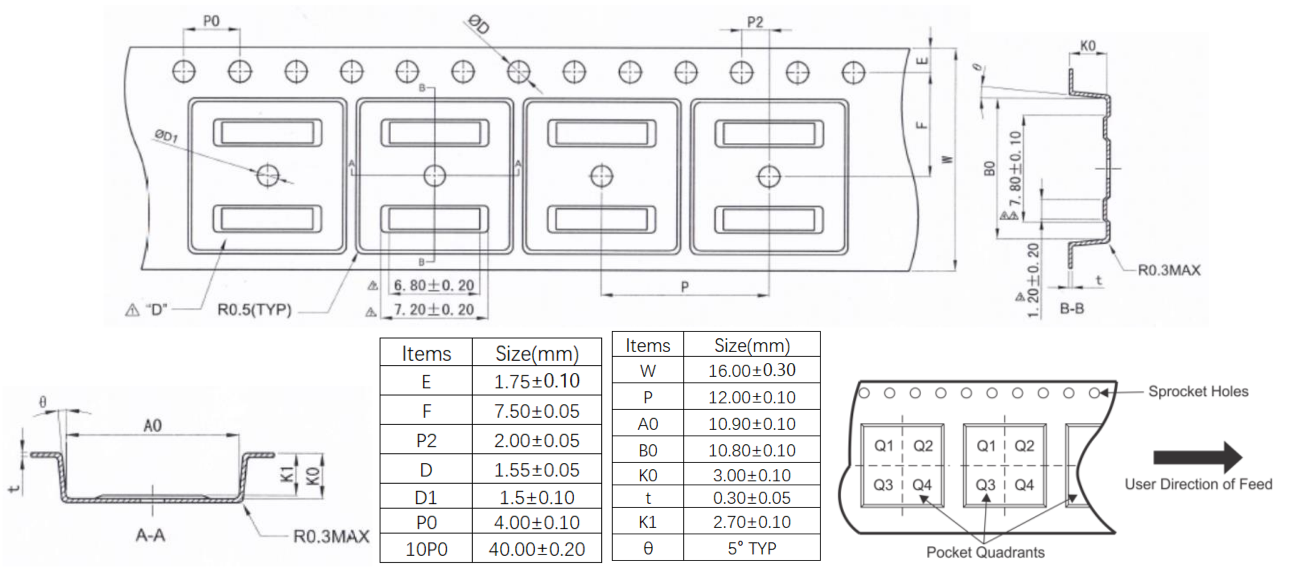


Fig 45.NB SOIC-16 Reel Information–dimension unit(mm)

Note：The Pin 1 of the chip is in the quadrant Q1



Items	Size(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5±0.10
P0	4.00±0.10
10P0	40.00±0.20

Items	Size(mm)
W	16.00±0.30
P	12.00±0.10
A0	10.90±0.10
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70±0.10
θ	5° TYP

Fig 46.WB SOIC-14 Reel Information

Note：The Pin1 of the chip is in the quadrant Q1

13. Ordering Guide

Table 19.Ordering Guide

Model Name	Temperature Range	Peak Current	Rec. VDD Supply Min.	Isolation Rating	Package	MSL Peak Temp [1]	Quantity per reel
Pai8252A-WR	−40~125°C	2A/4A	9.2V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8252B-WR	−40~125°C	2A/4A	6.5V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8252C-WR	−40~125°C	2A/4A	9.2V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8252D-WR	−40~125°C	2A/4A	6.5V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8252A-S1R	−40~125°C	2A/4A	9.2V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8252B-S1R	−40~125°C	2A/4A	6.5V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8252C-S1R	−40~125°C	2A/4A	9.2V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8252D-S1R	−40~125°C	2A/4A	6.5V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253A-WR	−40~125°C	4A/8A	9.2V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253B-WR	−40~125°C	4A/8A	6.5V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253C-WR	−40~125°C	4A/8A	9.2V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253D-WR	−40~125°C	4A/8A	6.5V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253E-WR	−40~125°C	4A/8A	13.7V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253F-WR	−40~125°C	4A/8A	13.7V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253A-S1R	−40~125°C	4A/8A	9.2V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253B-S1R	−40~125°C	4A/8A	6.5V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253C-S1R	−40~125°C	4A/8A	9.2V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253D-S1R	−40~125°C	4A/8A	6.5V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253E-S1R	−40~125°C	4A/8A	13.7V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253F-S1R	−40~125°C	4A/8A	13.7V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500

Pai8252AQ-WR[2]	−40~125°C	2A/4A	9.2V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8252BQ-WR[2]	−40~125°C	2A/4A	6.5V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8252CQ-WR[2]	−40~125°C	2A/4A	9.2V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8252DQ-WR[2]	−40~125°C	2A/4A	6.5V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8252AQ-S1R[2]	−40~125°C	2A/4A	9.2V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8252BQ-S1R[2]	−40~125°C	2A/4A	6.5V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8252CQ-S1R[2]	−40~125°C	2A/4A	9.2V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8252DQ-S1R[2]	−40~125°C	2A/4A	6.5V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253AQ-WR[2]	−40~125°C	4A/8A	9.2V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253BQ-WR[2]	−40~125°C	4A/8A	6.5V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253CQ-WR[2]	−40~125°C	4A/8A	9.2V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253DQ-WR[2]	−40~125°C	4A/8A	6.5V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253EQ-WR[2]	−40~125°C	4A/8A	13.7V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253FQ-WR[2]	−40~125°C	4A/8A	13.7V	5.0kVrms	WB SOIC-14	Level-2-260°C	1500
Pai8253AQ-S1R[2]	−40~125°C	4A/8A	9.2V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253BQ-S1R[2]	−40~125°C	4A/8A	6.5V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253CQ-S1R[2]	−40~125°C	4A/8A	9.2V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253DQ-S1R[2]	−40~125°C	4A/8A	6.5V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253EQ-S1R[2]	−40~125°C	4A/8A	13.7V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500
Pai8253FQ-S1R[2]	−40~125°C	4A/8A	13.7V	3.0kVrms	NB SOIC-16	Level-2-260°C	2500

Note：

1. MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
2. AEC-Q100 qualified for automotive application

14. Important Notice and Disclaimer

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15. Revision History

Revision	Date	Page	Change Record
Rev.0.1	2022-04-08	All	Initial version
Rev.1.0	2022-10-10	All	Update Pai8252X and NB SOIC-16 information
		Page 8	Update CMTI TYP 300kV/us to MIN 300kV/us
		Page 23	Update MSL3 to MSL2（Table 19）