Reinforced Insulation 5.7kV$_{RMS}$ 200Mbps Dual-Channel Digital Isolators

Data Sheet

Pai120E7x/121E7x/122E7x

FEATURES

- High data rate: 200Mbps
- High common-mode transient immunity: 100kV/μs Typical
- High robustness to radiated and conducted noise
- Low propagation delay: 14ns typical
- 5.7kV$_{RMS}$ isolation voltage
- High ESD rating:
  - ESDA/JEDEC JS-001-2017
  - Human body model (HBM) ±8kV
- Safety and regulatory approvals：
  - UL certificate number: E494497
    - 5.7kV$_{RMS}$ for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE certificate number: 40056491
    - DIN VDE V 0884-17:2021-10
    - V_{IORM} =2121V_{peak}
    - V_{IOSM} =6250V_{peak}
    - 10000V_{peak} surge isolation voltage approved
  - CQC certification per GB4943.1-2022
- 2.5V to 5.5V level translation
- AEC-Q100 qualification
- Wide temperature range: -40°C to 125°C
- RoHS-compliant, WB SOIC-8 and WB SOIC-16 package

APPLICATIONS

- General-purpose multichannel isolation
- Industrial field bus isolation
- Isolation Industrial automation systems
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control

GENERAL DESCRIPTION

The Pai1xxxxx is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using maturated standard semiconductor CMOS technology and 2PaiSemi ***iDivider®*** technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The Pai12xE7x isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 5.7kV$_{RMS}$ and the data rate from DC up to 200Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 2.5V to 5.5V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

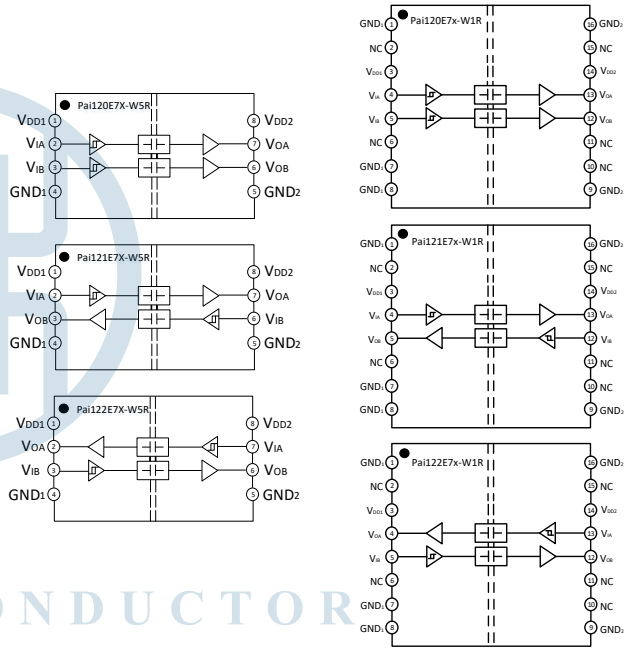

Figure 1.Pai120E7x/121E7x/122E7x Functional Block Diagram

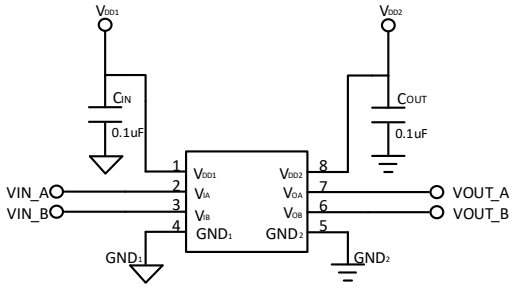

Figure 2.Pai120E7x Typical Application Circuit

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PIN CONFIGURATIONS AND FUNCTIONS

Table 1.Pai120E7x-W5R Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

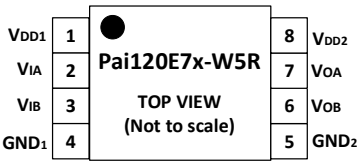


Figure 3.Pai120E7x-W5R Pin Configuration

Table 2.Pai121E7x-W5R Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{OB}	Logic Output B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{IB}	Logic Input B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

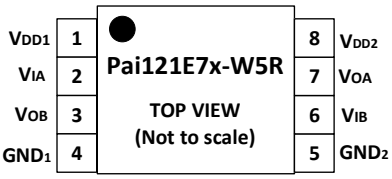


Figure 4. Pai121E7x-W5R Pin Configuration

Table 3.Pai122E7x-W5R Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

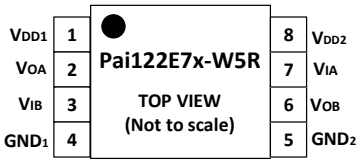


Figure 5.Pai122E7x-W5R Pin Configuration

Table 4. Pai120E7x-W1R Pin Function Descriptions

Pin No.	Name	Description
1, 7, 8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No connect.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	V_{IA}	Logic Input A.
5	V_{IB}	Logic Input B.
6	NC	No Connect.
9, 16	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V_{OB}	Logic Output B.
13	V_{OA}	Logic Output A.
14	V_{DD2}	Supply Voltage for Isolator Side 2.
15	NC	No Connect.

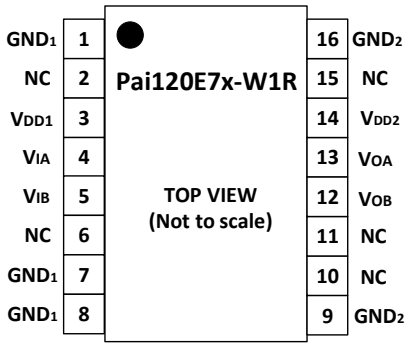


Figure 6. Pai120E7x-W1R Pin Configuration

Table 5. Pai121E7x-W1R Pin Function Descriptions

Pin No.	Name	Description
1, 7, 8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No Connect.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	V_{IA}	Logic Input A.
5	V_{OB}	Logic Output B.
6	NC	No Connect.
9, 16	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V_{IB}	Logic Input B.
13	V_{OA}	Logic Output A.
14	V_{DD2}	Supply Voltage for Isolator Side 2.
15	NC	No Connect.

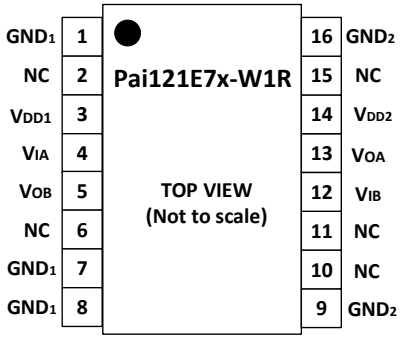


Figure 7. Pai121E7x-W1R Pin Configuration

Table 6. Pai122E7x-W1R Pin Function Descriptions

Pin No.	Name	Description
1, 7, 8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No Connect.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	V_{OA}	Logic Output A.
5	V_{IB}	Logic Input B.
6	NC	No Connect.
9, 16	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V_{OB}	Logic Output B.
13	V_{IA}	Logic Input A.
14	V_{DD2}	Supply Voltage for Isolator Side 2.
15	NC	No Connect.

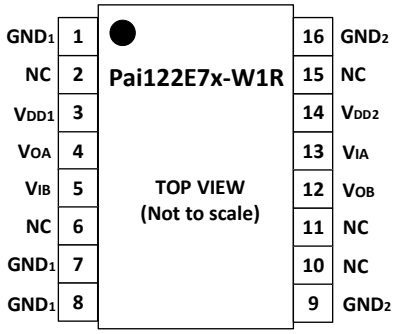


Figure 8. Pai122E7x-W1R Pin Configuration

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.Absolute Maximum Ratings[4]

Parameter	Rating
Supply Voltages (V_{DD1}-GND_1, V_{DD2}-GND_2)	−0.5V ~ +7.0V
Input Voltages (V_{IA}, V_{IB})[1]	−0.5V ~ V_{DDx} +0.5V
Output Voltages (V_{OA}, V_{OB})[1]	−0.5V ~ V_{DDx} +0.5V
Average Output Current per Pin[2] Side 1 Output Current (I_{O1})	−10mA ~ +10mA
Average Output Current per Pin[2] Side 2 Output Current (I_{O2})	−10mA ~ +10mA
Common-Mode Transients Immunity [3]	−250kV/μs ~ +250kV/μs
Storage Temperature (T_{ST}) Range	−65°C ~ +150°C
Ambient Operating Temperature (T_A) Range	−40°C ~ +125°C

Notes:

1. V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.
2. See **错误!未找到引用源。** for the maximum rated current values for various temperatures.
3. See **错误!未找到引用源。** for Common-mode transient immunity (CMTI) measurement.
4. Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 8.Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx} [1]	2.5		5.5	V
High Level Input Signal Voltage	V_{IH}	0.6*V_{DDx}[1]		V_{DDx}[1]	V
Low Level Input Signal Voltage	V_{IL}	0		0.3*V_{DDx}[1]	V
High Level Output Current	I_{OH}	-6			mA
Low Level Output Current	I_{OL}			6	mA
Data Rate		0		200	Mbps
Junction Temperature	T_J	-40		150	°C
Ambient Operating Temperature	T_A	-40		125	°C

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

TRUTH TABLES

Table 9.Pai120E7x/Pai121E7x/Pai122E7x Truth Table

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	Default Low V_{Ox} Output[1]	Default High V_{Ox} Output[1]	Test Conditions /Comments
Low	Powered[2]	Powered[2]	Low	Low	Normal operation
High	Powered[2]	Powered[2]	High	High	Normal operation
Open	Powered[2]	Powered[2]	Low	High	Default output
Don't Care[4]	Unpowered[3]	Powered[2]	Low	High	Default output[5]
Don't Care[4]	Powered[2]	Unpowered[3]	High Impedance	High Impedance	Power loose[6]

Notes:

[1] V_{Ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.

[2] Powered means V_{DDx}≥ 2.4 V

[3] Unpowered means V_{DDx} < 1.90V

[4] Input signal (V_{Ix}) must be in a low state to avoid powering the given V_{DDI}[1] through its ESD protection circuitry.

[5] If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1us. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 20us.

[6] If the V_{DDO} goes into unpowered status, the channel outputs will change to high impedance after around 1us. If the V_{DDO} goes into powered status, the channel outputs the input status logic signal after around 20us.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 10. Pai12xE7x Switching Specifications

Typical values are measured at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			5	ns	Within pulse width distortion (PWD) limit
Maximum Data Rate		200			Mbps	Within PWD limit
Propagation Delay Time[1]	t_{pHL}, t_{pLH}		13	16	ns	@ 5V_{DC} supply
			14	18.5	ns	@ 3.3V_{DC} supply
			16	20	ns	@ 2.5V_{DC} supply
Pulse Width Distortion	PWD		0.3	3.0	ns	The max different time between t_{pHL} and t_{pLH}@ 5V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
			0.4	3.0	ns	The max different time between t_{pHL} and t_{pLH}@ 3.3V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
			0.2	3.0	ns	The max different time between t_{pHL} and t_{pLH}@ 2.5V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Part to Part Propagation Delay Skew	t_{PSK}		0	4	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ $5V_{DC}$ supply
			0	4.5	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ $3.3V_{DC}$ supply
			0	5.5	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ $2.5V_{DC}$ supply
Channel to Channel Propagation Delay Skew	t_{CSK}		0	2	ns	The max amount propagation delay time differs between any two output channels in the single device @ $5V_{DC}$ supply.
			0	2	ns	The max amount propagation delay time differs between any two output channels in the single device @ $3.3V_{DC}$ supply
			0	2	ns	The max amount propagation delay time differs between any two output channels in the single device @ $2.5V_{DC}$ supply
Output Signal Rise/Fall Time[4]	t_r/t_f		1.5		ns	See *Figure 13*.
Dynamic Input Supply Current per Channel	$I_{DDI (D)}$		10		μA /Mbps	Inputs switching, 50% duty cycle square wave, $C_L + C_p$ = 10pF @ $5V_{DC}$ Supply
Dynamic Output Supply Current per Channel	$I_{DDO (D)}$		110		μA /Mbps	
Dynamic Input Supply Current per Channel	$I_{DDI (D)}$		10		μA /Mbps	Inputs switching, 50% duty cycle square wave, $C_L + C_p$ = 10pF @ $3.3V_{DC}$ Supply
Dynamic Output Supply Current per Channel	$I_{DDO (D)}$		70		μA /Mbps	
Dynamic Input Supply Current per Channel	$I_{DDI (D)}$		10		μA /Mbps	Inputs switching, 50% duty cycle square wave, $C_L + C_p$ = 10pF @ $2.5V_{DC}$ Supply
Dynamic Output Supply Current per Channel	$I_{DDO (D)}$		50		μA /Mbps	
Common-Mode Transient Immunity[3]	CMTI		100		kV/μs	$V_{IN} = V_{DDx}$[2] or 0V, V_{CM} = 1000V.
Jitter			180		ps p-p	See the Jitter Measurement section
			30		ps rms	
ESD(HBM - Human body model)	ESD		±8		kV	

Notes:

[1] t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See *Figure 14*.

[2] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[3] See *Figure 17* for Common-mode transient immunity (CMTI) measurement.

[4] t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

Table 11.DC Specifications

Typical values are measured at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rising Input Signal Voltage Threshold	V_{IT+}		$0.5*V_{DDx}$[1]	$0.6*V_{DDx}$[1]	V	
Falling Input Signal Voltage Threshold	V_{IT-}	$0.3*V_{DDX}$[1]	$0.35*V_{DDX}$[1]		V	
High Level Output Voltage	V_{OH} [1]	$V_{DDx} - 0.1$	V_{DDx}		V	−20 μA output current
		$V_{DDx} - 0.2$	$V_{DDx} - 0.1$		V	−2 mA output current

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Low Level Output Voltage	V_{OL}		0	0.1	V	20 µA output current
			0.1	0.2	V	2 mA output current
Input Current per Signal Channel	I_{IN}	−10	0.5	10	µA	0 V ≤ Signal voltage ≤ V_{DDx}[1]
V_{DDx}[1] Undervoltage Rising Threshold	V_{DDxUV+}	2.00	2.25	2.40	V	
V_{DDx}[1] Undervoltage Falling Threshold	V_{DDxUV-}	1.90	2.15	2.20	V	
V_{DDx}[1] Hysteresis	V_{DDxUVH}		0.10		V	

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Table 12.Quiescent Supply Current
Typical values are measured at T_A = 25°C, unless otherwise noted.

Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
Pai120E7x	$I_{DD1(Q)}$	0.27	0.36	0.66	mA	$5V_{DC}$	VI=0V for Pai12xEx0
	$I_{DD2(Q)}$	1.03	1.41	2.05	mA		VI=5V for Pai12xEx1
	$I_{DD1(Q)}$	1.42	1.82	2.30	mA		VI=5V for Pai12xEx0
	$I_{DD2(Q)}$	1.38	1.83	2.57	mA		VI=0V for Pai12xEx1
	$I_{DD1(Q)}$	0.25	0.33	0.47	mA	$3.3V_{DC}$	VI=0V for Pai12xEx0
	$I_{DD2(Q)}$	1.00	1.38	2.00	mA		VI=3.3V for Pai12xEx1
	$I_{DD1(Q)}$	1.46	1.80	2.26	mA		VI=3.3V for Pai12xEx0
	$I_{DD2(Q)}$	1.31	1.74	2.43	mA		VI=0V for Pai12xEx1
	$I_{DD1(Q)}$	0.19	0.29	0.45	mA	$2.5V_{DC}$	VI=0V for Pai12xEx0
	$I_{DD2(Q)}$	0.97	1.37	1.98	mA		VI=2.5V for Pai12xEx1
	$I_{DD1(Q)}$	1.31	1.68	2.23	mA		VI=2.5V for Pai12xEx0
	$I_{DD2(Q)}$	1.27	1.72	2.39	mA		VI=0V for Pai12xEx1
Pai121E7x	$I_{DD1(Q)}$	0.57	0.79	1.16	mA	$5V_{DC}$	VI=0V for Pai12xEx0
	$I_{DD2(Q)}$	0.57	0.79	1.16	mA		VI=5V for Pai12xEx1
	$I_{DD1(Q)}$	1.35	1.70	2.24	mA		VI=5V for Pai12xEx0
	$I_{DD2(Q)}$	1.35	1.70	2.24	mA		VI=0V for Pai12xEx1
	$I_{DD1(Q)}$	0.55	0.76	1.11	mA	$3.3V_{DC}$	VI=0V for Pai12xEx0
	$I_{DD2(Q)}$	0.55	0.76	1.11	mA		VI=3.3V for Pai12xEx1
	$I_{DD1(Q)}$	1.3	1.64	2.15	mA		VI=3.3V for Pai12xEx0
	$I_{DD2(Q)}$	1.3	1.64	2.15	mA		VI=0V for Pai12xEx1
	$I_{DD1(Q)}$	0.53	0.73	1.10	mA	$2.5V_{DC}$	VI=0V for Pai12xEx0
	$I_{DD2(Q)}$	0.53	0.73	1.10	mA		VI=2.5V for Pai12xEx1
	$I_{DD1(Q)}$	1.23	1.58	2.12	mA		VI=2.5V for Pai12xEx0
	$I_{DD2(Q)}$	1.23	1.58	2.12	mA		VI=0V for Pai12xEx1
Pai122E7x	$I_{DD1(Q)}$	0.57	0.79	1.16	mA	$5V_{DC}$	VI=0V for Pai12xEx0
	$I_{DD2(Q)}$	0.57	0.79	1.16	mA		VI=5V for Pai12xEx1
	$I_{DD1(Q)}$	1.35	1.70	2.24	mA		VI=5V for Pai12xEx0
	$I_{DD2(Q)}$	1.35	1.70	2.24	mA		VI=0V for Pai12xEx1
	$I_{DD1(Q)}$	0.55	0.76	1.11	mA	$3.3V_{DC}$	VI=0V for Pai12xEx0
	$I_{DD2(Q)}$	0.55	0.76	1.11	mA		VI=3.3V for Pai12xEx1
	$I_{DD1(Q)}$	1.3	1.64	2.15	mA		VI=3.3V for Pai12xEx0
	$I_{DD2(Q)}$	1.3	1.64	2.15	mA		VI=0V for Pai12xEx1
	$I_{DD1(Q)}$	0.53	0.73	1.10	mA	$2.5V_{DC}$	VI=0V for Pai12xEx0
	$I_{DD2(Q)}$	0.53	0.73	1.10	mA		VI=2.5V for Pai12xEx1
	$I_{DD1(Q)}$	1.23	1.58	2.12	mA		VI=2.5V for Pai12xEx0
	$I_{DD2(Q)}$	1.23	1.58	2.12	mA		VI=0V for Pai12xEx1

Table 13.Total Supply Current vs. Data Throughput

Typical values are measured at T_A = 25°C. C_L = 0pF and parasitic capacitance (C_p) is 10pF, unless otherwise noted.

Part	Symbol	2Mbps			20Mbps			200Mbps			Unit	Supply voltage
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Pai120E7x	I_{DD1}		1.19	1.9		1.31	2.1		2.52	4.02	mA	$5V_{DC}$
	I_{DD2}		1.98	3.17		3.9	6.24		21.7	34.7		
	I_{DD1}		1.13	1.8		1.24	1.99		2.33	3.73	mA	$3.3V_{DC}$
	I_{DD2}		1.82	2.91		3	4.8		14.3	22.8		
	I_{DD1}		1.04	1.67		1.09	1.75		2.16	3.45	mA	$2.5V_{DC}$
	I_{DD2}		1.74	2.78		2.62	4.2		11.4	18.2		
Pai121E7x	I_{DD1}		1.33	2.15		2.32	3.76		13.1	21.4	mA	$5V_{DC}$
	I_{DD2}		1.33	2.15		2.32	3.76		13.1	21.4		
	I_{DD1}		1.27	2.03		1.91	3.1		9.13	15.1	mA	$3.3V_{DC}$
	I_{DD2}		1.27	2.03		1.91	3.1		9.13	15.1		
	I_{DD1}		1.2	1.93		1.7	2.75		6.98	11.7	mA	$2.5V_{DC}$
	I_{DD2}		1.2	1.93		1.7	2.75		6.98	11.7		
Pai122E7x	I_{DD1}		1.33	2.15		2.32	3.76		13.1	21.4	mA	$5V_{DC}$
	I_{DD2}		1.33	2.15		2.32	3.76		13.1	21.4		
	I_{DD1}		1.27	2.03		1.91	3.1		9.13	15.1	mA	$3.3V_{DC}$
	I_{DD2}		1.27	2.03		1.91	3.1		9.13	15.1		
	I_{DD1}		1.2	1.93		1.7	2.75		6.98	11.7	mA	$2.5V_{DC}$
	I_{DD2}		1.2	1.93		1.7	2.75		6.98	11.7		

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 14.Insulation Specifications

Parameter	Symbol	Value	Unit	Test Conditions/Comments
		Pai12xE7x		
Rated Dielectric Insulation Voltage		5700	V_{RMS}	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	≥8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	≥8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		≥21	µm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	≥600	V	DIN EN 60112 (VDE 0303-11):2010-05
Material Group		I		IEC 60112:2003 + A1:2009

PACKAGE CHARACTERISTICS

Table 15.Package Characteristics

Parameter	Symbol	Typical Value	Typical Value	Unit	Test Conditions/Comments
		Pai12xE7x -W5R	Pai12xE7x-W1R		
Capacitance (Input to Output)[1]	C_{IO}	1.5	1.5	pF	@1MHz
Input Capacitance[2]	C_I	3	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}	86.5	45	°C/W	Thermocouple located at center of package underside

Notes:

1. The device is considered a 2-terminal device. Short-circuit all terminals on the VDD_1 side as one terminal and short-circuit all terminals on the VDD_2 side as the other terminal.
2. Testing from the input signal pin to ground.

REGULATORY INFORMATION

Table 16.Regulatory

Regulatory	Pai12xE7x
UL	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 5700V_{RMS} Isolation Voltage File E494497
VDE	DIN VDE V 0884-11:2017-01[2] Reinforced insulation, V_{IORM} = 2121V_{Peak}, V_{IOSM} = 6250V_{Peak} File number: 40056491
CQC	Certified under CQC11-471543-2012 and GB4943.1-2022 Basic insulation at 845V_{RMS} (1200V_{peak}) working voltage Reinforced insulation at 422V_{RMS} (600V_{peak}) Pai12XE7X-W5R File number: CQC23001377708 Pai12XE7X-W1R File number: CQC23001377704

Notes:

[1] In accordance with UL 1577, each Pai120E7x/Pai121E7x/Pai122E7x is proof tested by applying an insulation test voltage ≥ 6840V_{RMS} for 1 sec.

DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 INSULATION CHARACTERISTICS

Table 17.VDE Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic Pai12xE7x	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V_{RMS} For Rated Mains Voltage ≤ 300 V_{RMS} For Rated Mains Voltage ≤ 400 V_{RMS}			 I to IV I to IV I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive peak isolation voltage		V_{IORM}	2121	V_{peak}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5pC	$V_{pd\ (m)}$	3977	V_{peak}
Input to Output Test Voltage, Method A After Environmental Tests Subgroup 1 After Input and/or Safety Test Subgroup 2 and Subgroup 3	 V_{IORM} × 1.6 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5pC V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5pC	 $V_{pd\ (m)}$ $V_{pd\ (m)}$	 3394 2545	 V_{peak} V_{peak}
Highest Allowable Overvoltage		V_{IOTM}	8060	V_{peak}
Maximum Surge Isolation Voltage	Reinforced insulation, 1.2/50 µs combination wave, VTEST = 1.6 × VIOSM (qualification)[1]	V_{IOSM}	6250	V_{peak}
Safety Limiting Values	Maximum value allowed in the event of a failure (see *Figure 9* and *Figure 10*.)			
Maximum safety Temperature		T_S	150	°C
Maximum Power Dissipation at 25°C	Pai12xE7x-W5R, WB SOIC-8 Package	P_S	1.44	W
Maximum Power Dissipation at 25°C	Pai12xE7x-W1R, WB SOIC-16 Package	P_S	2.78	W
Insulation Resistance at T_S	V_{IO} = 500 V at T_A=25°C	R_{IO}	⩾10^{12}	Ω
	V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C		⩾10^{11}	Ω
	V_{IO} = 500 V at T_S=150°C		⩾10^{9}	Ω

Notes:

[1]In accordance with DIN V VDE V 0884-17, Pai1xxE7x is proof tested by applying a surge isolation voltage 10000V.

TYPICAL THERMAL CHARACTERISTIC

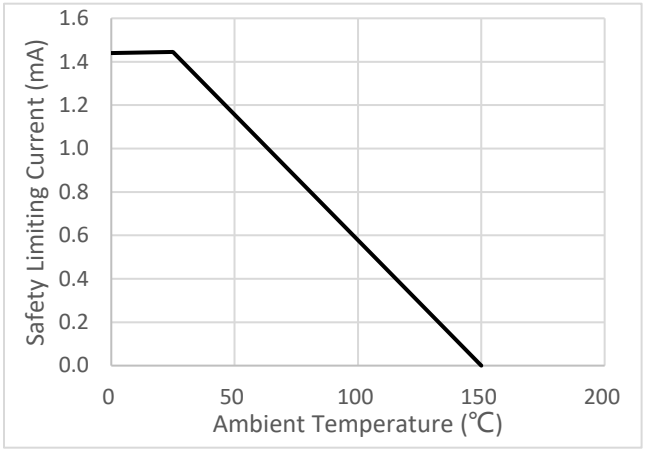


Figure 9.Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE, WB SOIC-8 Package, Pai12xE7x-W5R

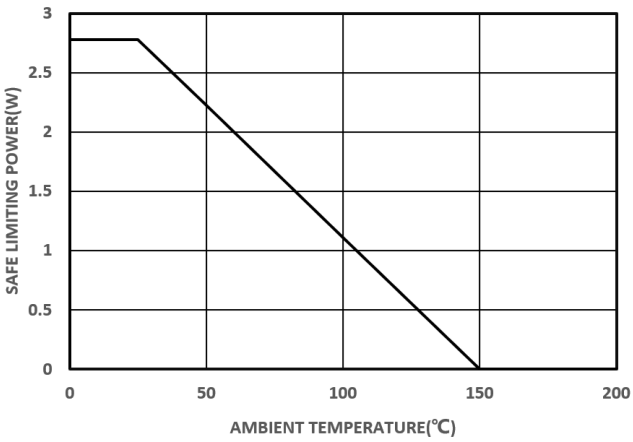


Figure 10.Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE, WB SOIC-16 Package, Pai12xE7x-W1R

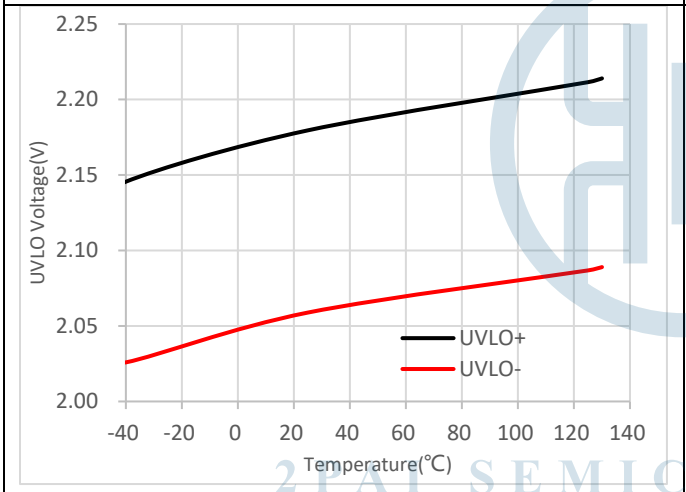


Figure 11.UVLO vs. Free-Air Temperature

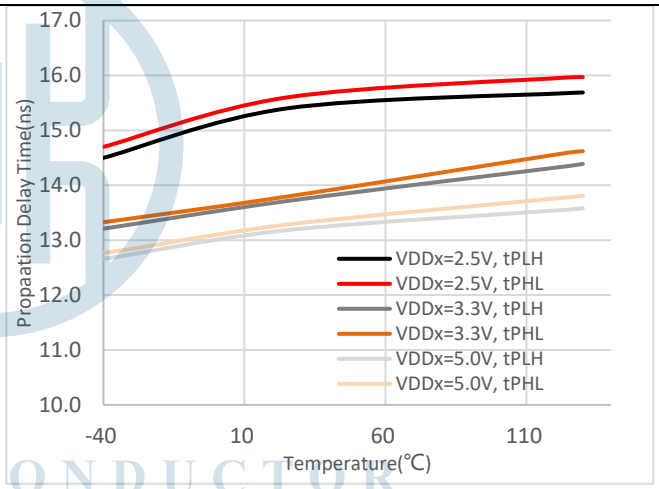


Figure 12.Pai12xE7x Propagation Delay Time vs. Free-Air Temperature

TIMING TEST INFORMATION

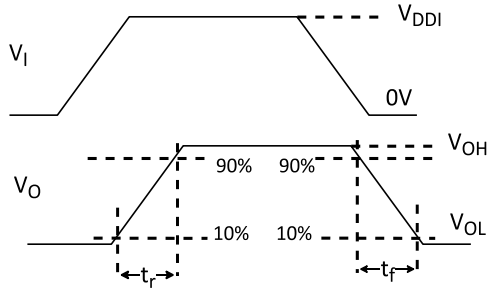


Figure 13.Transition Time Waveform Measurement

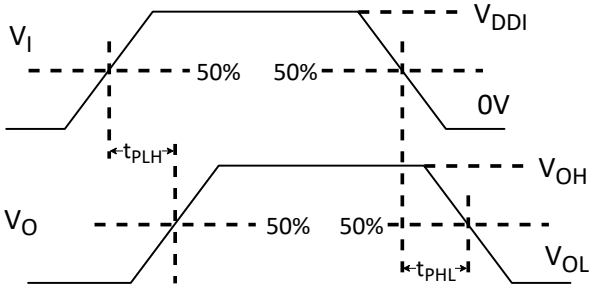


Figure 14. Propagation Delay Time Waveform Measurement

APPLICATIONS INFORMATION

OVERVIEW

The Pai1xxxxx are 2PaiSemi digital isolators product family based on 2PaiSemi unique ***iDivider®*** technology. Intelligent voltage ***Divider*** technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, ***iDivider®*** is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using maturated standard semiconductor CMOS technology and the innovative ***iDivider®*** design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The Pai12xE7x isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 5.7 kV_{RMS} and the data rate from DC up to 200Mbps (see the Ordering Guide).

The Pai120Exx/Pai121Exx/Pai122Exx are the outstanding dual-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The Pai120E7x/Pai121E7x/Pai122E7x have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 2.5V to 5.5V, offering voltage translation of 3.3V and 5V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

PCB LAYOUT

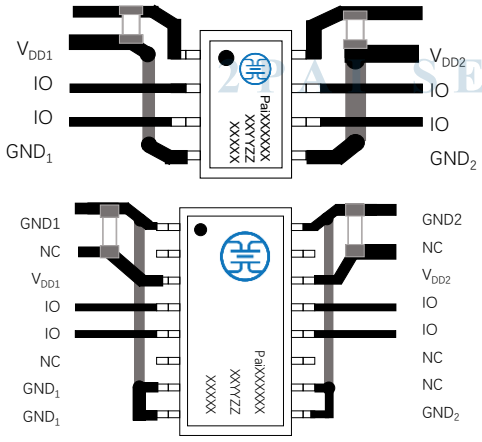


Figure 15.Recommended Printed Circuit Board Layout

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1μF and 10μF. The user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy, or in order to enhance the anti ESD ability of the system.

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

JITTER MEASUREMENT

The eye diagram shown in the figure below provides the jitter measurement result for the Pai120Exx/Pai121Exx/Pai122Exx. The Keysight 81160A pulse function arbitrary generator works as the data source for the Pai120Exx/Pai121Exx/Pai122Exx, which generates 100Mbps pseudo random bit sequence (PRBS). The Keysight DSOS104A digital storage oscilloscope captures the Pai120Exx/Pai121Exx/Pai122Exx output waveform and recoveries the eye diagram with the SDA jitter tools and eye diagram analysis tools. The result shows a typical measurement jitter data.

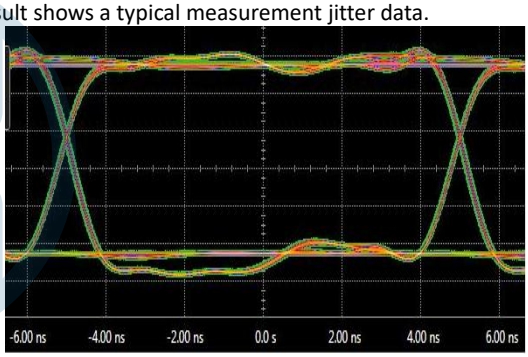


Figure 16.Pai120Exx/Pai121Exx/Pai122Exx Eye Diagram

CMTI MEASUREMENT

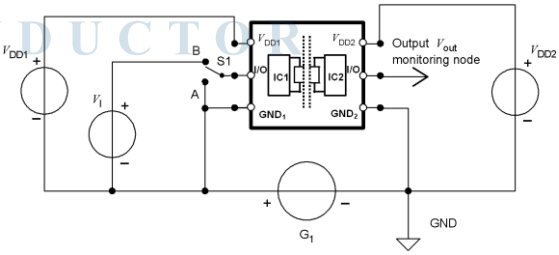
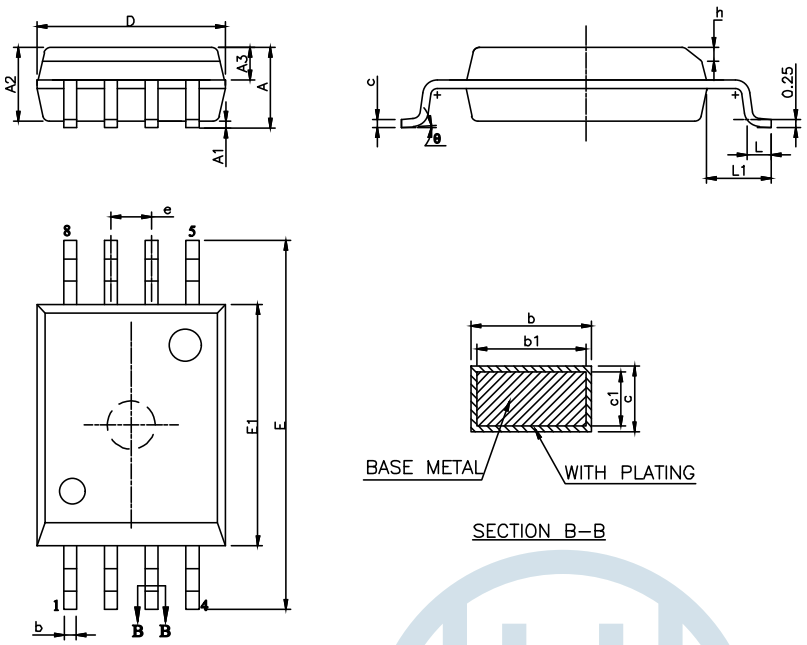


Figure 17.Common-mode Transient Immunity (CMTI) Measurement

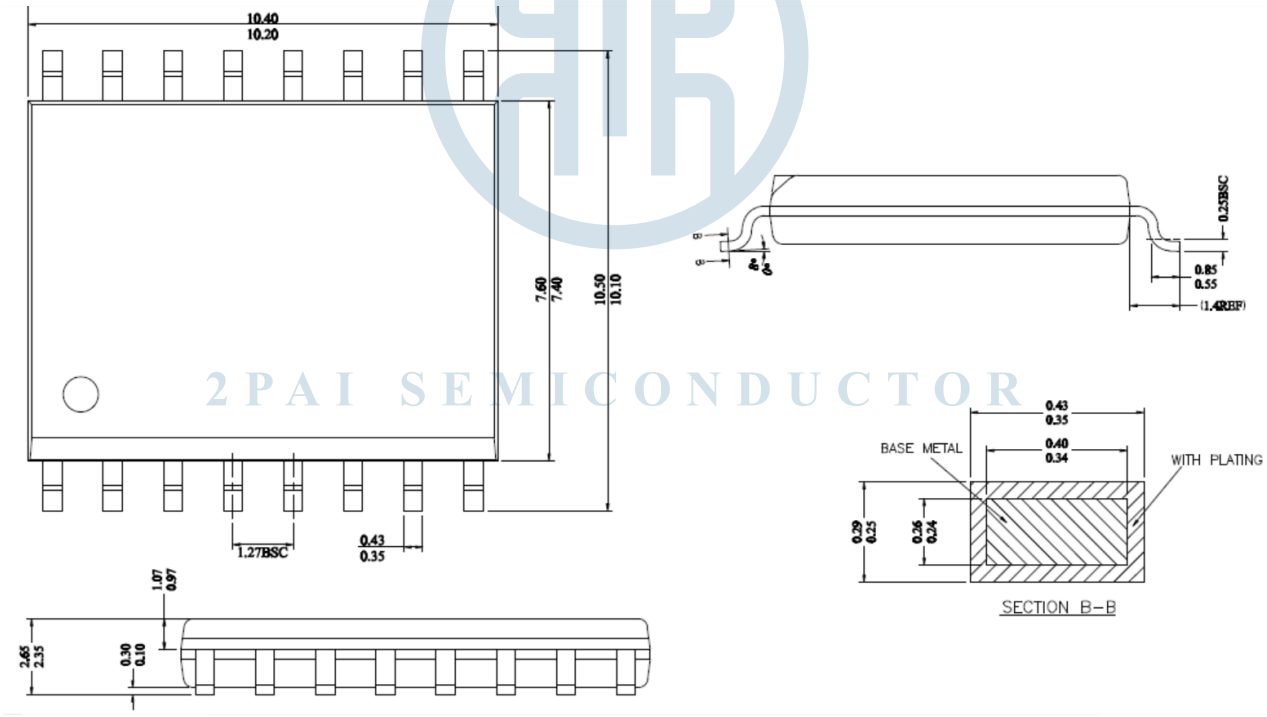
To measure the Common-Mode Transient Immunity (CMTI) of Pai1xxxxx isolator under specified common-mode pulse magnitude (V_{CM}) and specified slew rate of the common-mode pulse (dV_{CM}/dt) and other specified test or ambient conditions, The common-mode pulse generator (G_1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (V_{CM}),such that the maximum common-mode slew rates (dV_{CM}/dt) can be applied to Pai1xxxxx isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of Pai1xxxxx isolator and shall be capable of providing positive transients as well as negative transients.

OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	1.00
L1	2.00REF		
θ	0	—	8°

Figure 18. 8-Lead Wide Body SOIC [WB SOIC-8] *Outline Package–dimension unit(mm)*



Notes:

ALL DIMENSIONS MEET JEDEC STANDARD MS-013 AA

DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure 19.16-Lead Wide Body SOIC [WB SOIC-16] *Outline Package –dimension unit(mm)*

LAND PATTERNS

8-Lead Wide Body SOIC [WB SOIC-8]

The figure below illustrates the recommended land pattern details for the Pai1xxxxx in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

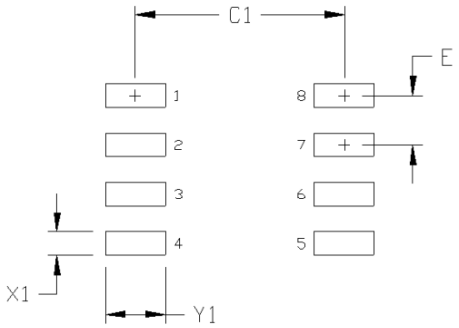


*Figure 20.*8-Lead Wide Body SOIC [WB SOIC-8] Land Pattern

Table 18.8-Lead Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	9.75	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	2.00	mm

Note：

1.This land pattern design is based on IPC -7351.

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

16-Lead Wide Body SOIC [WB SOIC-16]

The figure below illustrates the recommended land pattern details for the π1xxxxx in a 16-pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

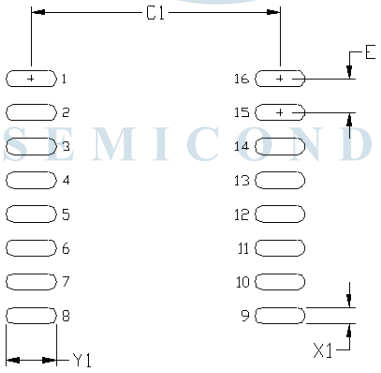


*Figure 21.*16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern

Table 19. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	9.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.90	mm

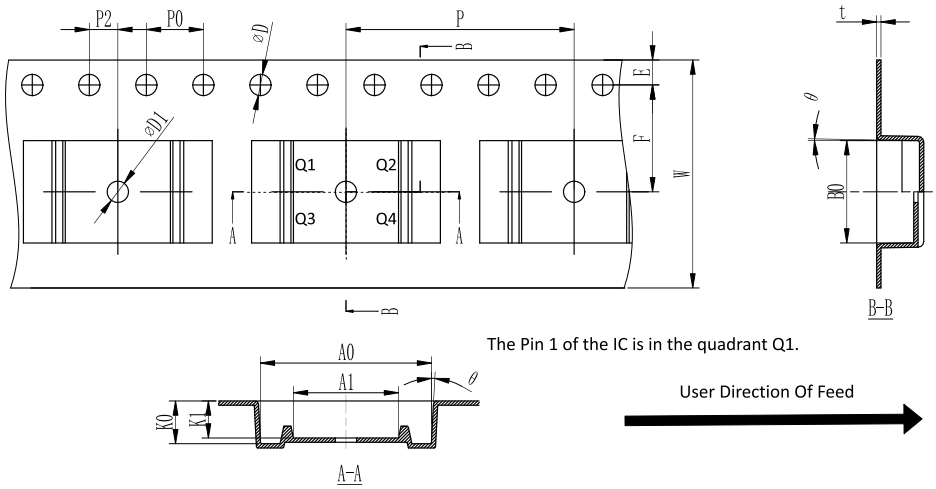
Note：

1.This land pattern design is based on IPC -7351

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

REEL INFORMATION

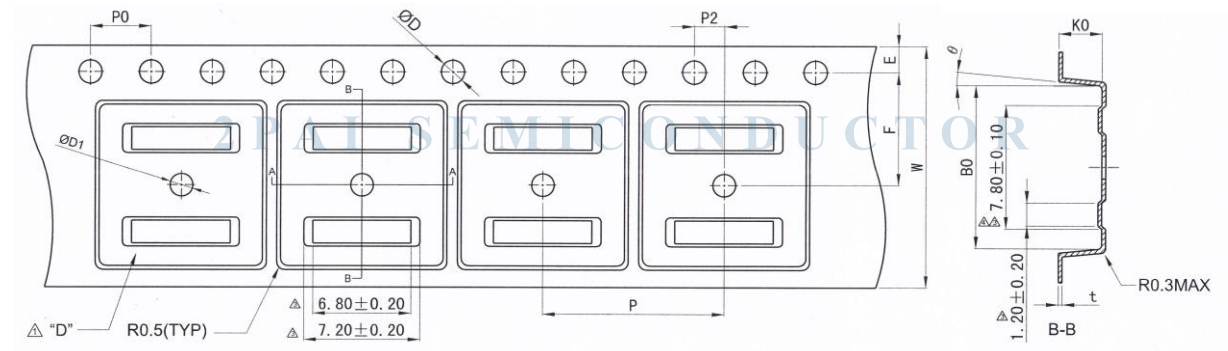
8-Lead Wide Body SOIC [WB SOIC-8]



Items	Size	Unit	Items	Size	Unit
E	1.75 ± 0.10	mm	W	16.00 ± 0.30	mm
F	7.50 ± 0.10	mm	P	16.00 ± 0.10	mm
P2	2.00 ± 0.10	mm	A0	11.98 ± 0.10	mm
D	$1.50^{+0.10}_{0}$	mm	A1	7.37 ± 0.10	mm
D1	$1.50^{+0.10}_{0}$	mm	B0	6.11 ± 0.10	mm
P0	4.00 ± 0.10	mm	K0	3.00 ± 0.10	mm
10P0	40.0 ± 0.20	mm	K1	2.60 ± 0.10	mm
			t	0.30 ± 0.05	mm
			θ	5 typical	Degree

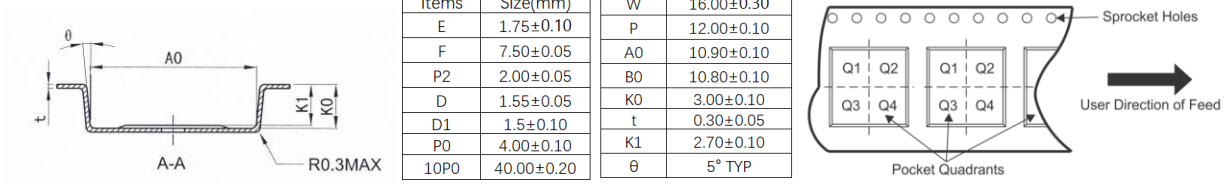
Figure 22. 8-Lead Wide Body SOIC [WB SOIC-8] Reel Information–*dimension unit(mm)*

16-Lead Wide Body SOIC [WB SOIC-16]



Items	Size(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5±0.10
P0	4.00±0.10
10P0	40.00±0.20

Items	Size(mm)
W	16.00±0.30
P	12.00±0.10
A0	10.90±0.10
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70±0.10
θ	5° TYP



Note：The Pin 1of the chip is in the quadrant Q1

Figure 23. 16-Lead Wide Body SOIC [WB SOIC-16] Reel Information

TOP MARKING

Line 1	Pai1XXXXXX = Product name
Line 2	YY = Work year WW = Work week ZZ = Manufacturing code from assembly house
Line 3	XXXXX, no special meaning

Figure 24. Top Marking

ORDERING GUIDE

Table 20. ORDERING GUIDE

Model Name [3]	Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV_{RMS})	Fail-Safe Output State	Package Description	MSL Peak Temp [1]	MOQ/ Quantity per reel[2]
Pai120E71-W5R	−40 to 125°C	2	0	5.7	High	WB SOIC-8	Level-3-260C-168 HR	1000
Pai120E71Q-W5R	−40 to 125°C	2	0	5.7	High	WB SOIC-8	Level-3-260C-168 HR	1000
Pai120E70-W5R	−40 to 125°C	2	0	5.7	Low	WB SOIC-8	Level-3-260C-168 HR	1000
Pai120E70Q-W5R	−40 to 125°C	2	0	5.7	Low	WB SOIC-8	Level-3-260C-168 HR	1000
Pai121E71-W5R	−40 to 125°C	1	1	5.7	High	WB SOIC-8	Level-3-260C-168 HR	1000
Pai121E71Q-W5R	−40 to 125°C	1	1	5.7	High	WB SOIC-8	Level-3-260C-168 HR	1000
Pai121E70-W5R	−40 to 125°C	1	1	5.7	Low	WB SOIC-8	Level-3-260C-168 HR	1000
Pai121E70Q-W5R	−40 to 125°C	1	1	5.7	Low	WB SOIC-8	Level-3-260C-168 HR	1000
Pai122E71-W5R	−40 to 125°C	1	1	5.7	High	WB SOIC-8	Level-3-260C-168 HR	1000
Pai122E71Q-W5R	−40 to 125°C	1	1	5.7	High	WB SOIC-8	Level-3-260C-168 HR	1000
Pai122E70-W5R	−40 to 125°C	1	1	5.7	Low	WB SOIC-8	Level-3-260C-168 HR	1000
Pai122E70Q-W5R	−40 to 125°C	1	1	5.7	Low	WB SOIC-8	Level-3-260C-168 HR	1000
Pai120E71-W1R	−40 to 125°C	2	0	5.7	High	WB SOIC-16	MSL2 (Pending)	1500
Pai120E71Q-W1R	−40 to 125°C	2	0	5.7	High	WB SOIC-16	MSL2 (Pending)	1500
Pai120E70-W1R	−40 to 125°C	2	0	5.7	Low	WB SOIC-16	MSL2 (Pending)	1500
Pai120E70Q-W1R	−40 to 125°C	2	0	5.7	Low	WB SOIC-16	MSL2 (Pending)	1500
Pai121E71-W1R	−40 to 125°C	1	1	5.7	High	WB SOIC-16	MSL2 (Pending)	1500
Pai121E71Q-W1R	−40 to 125°C	1	1	5.7	High	WB SOIC-16	MSL2 (Pending)	1500
Pai121E70-W1R	−40 to 125°C	1	1	5.7	Low	WB SOIC-16	MSL2 (Pending)	1500
Pai121E70Q-W1R	−40 to 125°C	1	1	5.7	Low	WB SOIC-16	MSL2 (Pending)	1500
Pai122E71-W1R	−40 to 125°C	1	1	5.7	High	WB SOIC-16	MSL2 (Pending)	1500
Pai122E71Q-W1R	−40 to 125°C	1	1	5.7	High	WB SOIC-16	MSL2 (Pending)	1500
Pai122E70-W1R	−40 to 125°C	1	1	5.7	Low	WB SOIC-16	MSL2 (Pending)	1500
Pai122E70Q-W1R	−40 to 125°C	1	1	5.7	Low	WB SOIC-16	MSL2 (Pending)	1500

Note:

1. MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
2. MOQ, minimum ordering quantity.
3. Devices with Q suffix are AEC-Q100 qualified.

PART NUMBER NAMED RULE

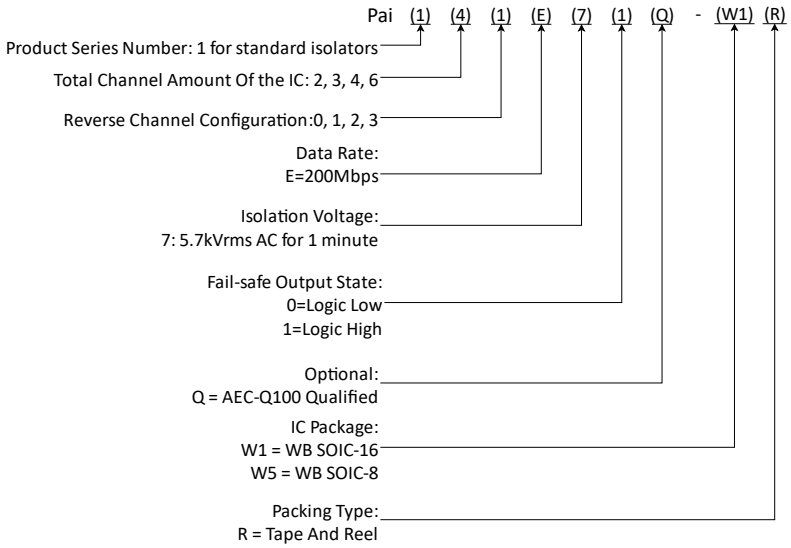


Figure 25. Part Number Named Rule

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http://www.rpsemi.com/

REVISION HISTORY

Revision	Date	Page	Change Record
0.1	2022/11/21	All	Initial version
0.2	2023/03/21	3	Recommended Operating Conditions.
0.3	2023/06/28	1~3, 7~8, 12~15	Added WB SOIC-16 products.
0.4	2023/8/16	14	Changed the moisture sensitivity level; added AEC-Q100 description.
0.5	2023/12/10	6, 7	Refined supply current data.

单击下面可查看定价，库存，交付和生命周期等信息

>>2pai semi(荣湃半导体)