Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Features

- Wide-Supply Voltage Range: 1.6 V to 6.0 V
- Very Low Quiescent Current: 600 nA typ
- Fixed Threshold Voltage from 0.6 V to 5 V with 100 mV Step
- Adjustable Version with Low Threshold Voltage 0.405 V (min)
- Power-on Reset Generator with Adjustable Delay Time from 1.25 ms to 10 s
- High Threshold Accuracy 1% Typ
- Manual Reset $\overline{MR}$ Input
- Open-drain (TPV8308xD) $\overline{RESET}$ /RESET Output
- Push-pull (TPV8308xP) $\overline{RESET}$ /RESET Output
- Push-pull (TPV8308xP) $\overline{RESET}$ /RESET Output
- Active Low $\overline{RESET}$ (TPV8308Lx) and Active High RESET (TPV8308Hx)
- Temperature Range: −40°C to 125°C
- Green Product, SOT23-6 and DFN2X2-6 Package

Applications

- Server and Data Center
- Surveillance and IP Camera
- Network Switches and Routers
- Solid State Drive
- Optical Communication Module

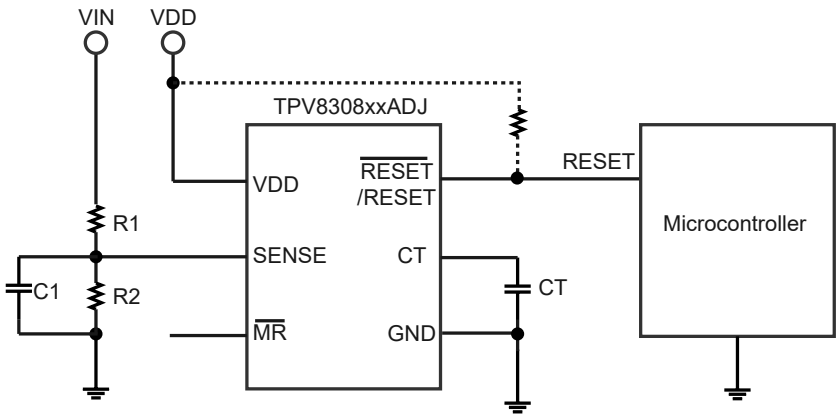
Description

The TPV8308 is a family of supervisory circuits to monitor a voltage rail from 0.4 V to 5 V, asserting an active low/ active high open-drain or push-pull $\overline{RESET}$ /RESET output when the voltage of the sense pin drops below a fixed threshold or when the manual reset pin $\overline{MR}$ is logic low. The $\overline{RESET}$ /RESET output remains low/high for the user-adjusted delay time by the external capacitor after the sense voltage returns above the fixed threshold with a hysteresis and the manual reset MR return to logic high.

The threshold voltage of the TPV8308 device can achieve 1% accuracy. The delay time can be set to 1.25 ms to 10 s by connecting the external capacitor to the CT pin. The TPV8308 family has a very low typical quiescent current of 600 nA.

The TPV8308 is available in SOT23 and DFN2x2 packages. Its operating temperature range is from −40°C to +125°C.

Typical Application Circuit



Low Quiescent Current Supervisory Circuits with Programmable Reset Delay

Table of Contents

Product Family Table

Order Number	Threshold Voltage (V_{IT})	Nominal Monitored Voltage	Marking	Package
TPV8308LDADJ-S6TR	0.405 V	Adjustable	LDJ	SOT23-6
TPV8308LD080-S6TR (1)	0.8 V	0.9 V	X08	SOT23-6
TPV8308LD160-S6TR	1.6 V	1.8 V	X16	SOT23-6
TPV8308LD170-S6TR (1)	1.7 V	1.9 V	X17	SOT23-6
TPV8308LD220-S6TR (1)	2.2 V	2.5 V	X22	SOT23-6
TPV8308LD270-S6TR (1)	2.7 V	3.0 V	X27	SOT23-6
TPV8308LD300-S6TR (1)	3.0 V	3.3 V	X30	SOT23-6
TPV8308LD400-S6TR (1)	4.0 V	5.0 V	X40	SOT23-6
TPV8308LD420-S6TR (1)	4.2 V	5.0 V	X42	SOT23-6
TPV8308HDADJ-S6TR (1)	0.405 V	Adjustable	HDJ	SOT23-6
TPV8308LPADJ-S6TR (1)	0.405 V	Adjustable	LPJ	SOT23-6
TPV8308HPADJ-S6TR (1)	0.405 V	Adjustable	HPJ	SOT23-6
TPV8308LDADJ-DFOR (1)	0.405 V	Adjustable	DDJ	DFN2X2-6

(1) For future products, contact the 3PEAK factory for more information and samples.

Revision History

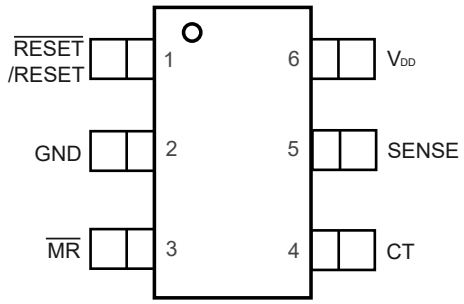
Date	Revision	Notes
2020-08-05	Rev.Pre.0	Pre-Release Version.
2020-12-30	Rev.Pre.1	Modified Definition of Part Number.
2021-07-14	Rev.Pre.2	Updated Description.
2022-04-04	Rev.Pre.3	Updated ESD/CDM to 1000 V.
2022-07-18	Rev.Pre.4	Updated as new datasheet format, thermal resistance information, and VIT accuracy in EC table.
2022-09-05	Rev.Pre.5	Updated description by adding reset timing and equation of delay time.
2022-12-20	Rev.A.0	Updated block diagram.

Pin Configuration and Functions

TPV8308

SOT23-6 Package

Top View



TPV8308

DFN2X2-6 Package

Top View

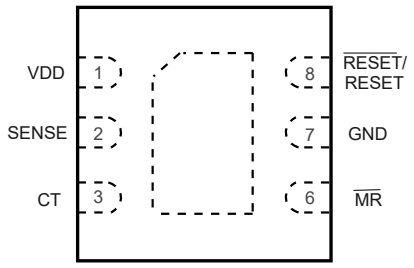


Table 1. Pin Functions: TPV8308

Pin		Name	I/O	Description
SOT23-6	DFN2X2-6			
1	6	$\overline{\text{RESET}}$/ RESET	O	$\overline{\text{RESET}}$/RESET Output. This pin is active low open drain output or push-pull output. It is driven to a low impedance state when $\overline{\text{RESET}}$/RESET is asserted by the voltage of the sense pin lower than the threshold V_{IT}, or $\overline{\text{MR}}$ pin is low. $\overline{\text{RESET}}$/RESET will keep low for the reset delay time programmed by the CT pin after both of the sense pin is above V_{IT} and $\overline{\text{MR}}$ pin is high. A pulled-up resistor from 10 kΩ to 1 MΩ should be connected to VDD if it is open drain output.
2	5	GND	G	Ground. This pin should be connected to ground reference.
3	4	$\overline{\text{MR}}$	I	Manual Reset Input $\overline{\text{MR}}$ low asserts $\overline{\text{RESET}}$/RESET pin. $\overline{\text{MR}}$ is internal tied to VDD by a 90 kΩ pull-up resistor.
4	3	CT	I/O	Reset Delay Time Programming Pin. Connecting this pin to VDD through a 40 kΩ to 200 kΩ resistor or leaving it open results in fixed reset delay times. Connecting this pin to ground referenced capacitor (≥ 100 pF) gives a user-programmable reset delay time.
5	2	SENSE	I	Sense Pin. It is used for monitoring voltage. If the voltage drops below the threshold voltage VIT, the $\overline{\text{RESET}}$/ RESET is asserted. The sense pin can be connected to any voltage by configuring an external resistor divider.
6	1	VDD	P	Supply Voltage. A 0.1-μF ceramic capacitor was placed as close as to the VDD pin.
-	EP	EP		Exposed Pad. Connect it to ground plane for good thermal dissipation.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Power Supply, V_{DD} to GND		−0.3	6.5	V
V_{CT} V_{RESET} V_{MR}	Input Voltage for CT, $\overline{MR}$, $\overline{RESET}$/RESET pin	−0.3 to V_{DD} + 0.3 V, max 6 V		
V_{SENSE}	Input Voltage for SENSE Pin	−0.3	6.5	V
I_{RESET}	Current of $\overline{RESET}$/RESET Pin		5	mA
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		300	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-6	128.8	67	°C/W
DFN2X2-6	120	20.3	°C/W

Electrical Characteristics

All test conditions: V_{IN} = 5 V, T_A = +25°C, unless otherwise noted.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range		−40°C < T_A < 125°C	1.6		6.0	V
$V_{DD(min)}$	Minimum VDD to Guaranteed $\overline{RESET}$/ RESET Output Valid (1)				0.5	0.8	V
I_{DD}	Quiescent Current (I_Q)		V_{DD} = 5.5V, $\overline{RESET}$/RESET not asserted, $\overline{MR}$, $\overline{RESET}$ /RESET, CT pin open		0.6	1.5	μA
V_{OL}	Output Low Voltage of $\overline{RESET}$/RESET Pin		1.6 V ≤ V_{DD} < 6.0 V, I_{OL} = 2.0 mA			0.3	V
$V_{IT,ERR}$	Negative-going Input Threshold Accuracy		−40°C < T_J < 125°C	−3	±1	3	%
V_{HYS}	Hysteresis on V_{IT}		1.6 ≤ V_{DD} ≤ 4.2 V		1.0	3.0	%
			4.2 ≤ V_{DD} ≤ 6.0 V		1.75	3.75	%
R_{MR}	MR Internal Pull-up Resistance				90		kΩ
I_{SENSE}	Input Current at SENSE Pin	TPV8308ADJ	V_{SENSE} = V_{IT}		5		nA
		Fixed version	V_{SENSE} = 5.5 V		110		nA
I_{OH}	$\overline{RESET}$/RESET Leakage Current		V_{RESET} = 5.5 V			300	nA
C_{IN}	Input Capacitance, any pin	CT pin	V_{IN} = 0 V to V_{DD}		5	5	pF
		Other pins	V_{IN} = 0 V to 6.0 V		5	5	pF
V_{IL}	$\overline{MR}$ Logic Low Input			0		0.3V_{DD}	
V_{IH}	$\overline{MR}$ Logic High Input			0.7V_{DD}		V_{DD}	
Switching Electrical Specifications							
t_w	Input Pulse Width to Assert $\overline{RESET}$/RESET Pin	SENSE	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		12		μs
		$\overline{MR}$	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		300		ns
t_D	Reset Delay Time	C_T = Open	Guaranteed by design and characterization		20		ms
		C_T = V_{DD}			300		ms
		C_T = 100 pF			1.25		ms
		C_T = 180 nF			1200		ms
t_{P1}	Propagation Delay from $\overline{MR}$	$\overline{MR}$ to $\overline{RESET}$/ RESET	V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}		300		ns
t_{P2}	Propagation Delay from SENSE	SENSE to $\overline{RESET}$/ RESET	V_{IH} = 1.05 V_{DD}, V_{IL} = 0.95 V_{DD}		12		μs

(1) Guaranteed by bench test

Typical Performance Characteristics

All test conditions: V_{IN} = 5 V, T_A = + 25°C, unless otherwise noted.

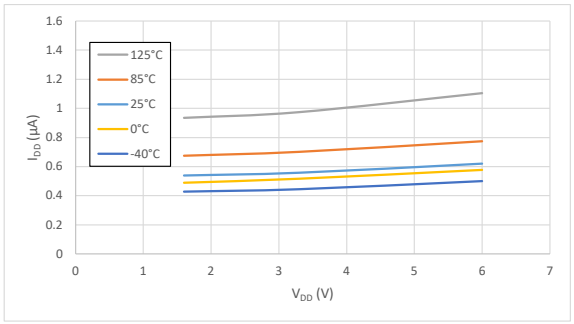


Figure 1. Supply Current vs Supply Voltage

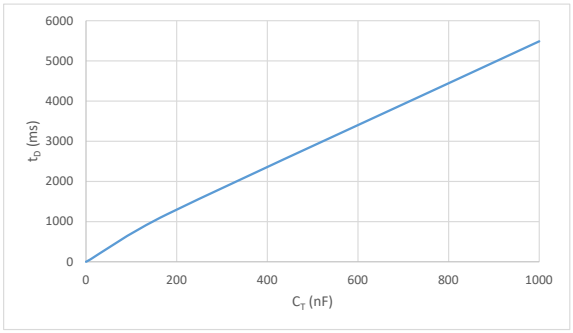


Figure 2. Reset Delay Time vs C_T

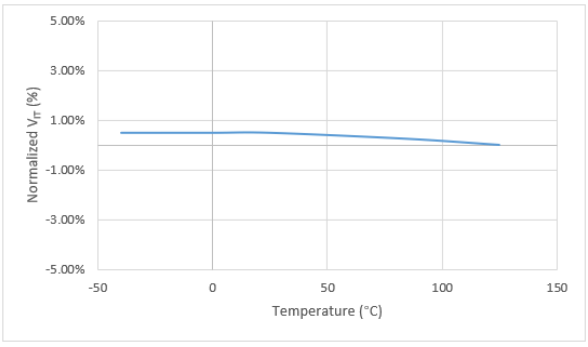


Figure 3. Normalized Sense Threshold Voltage vs Temperature

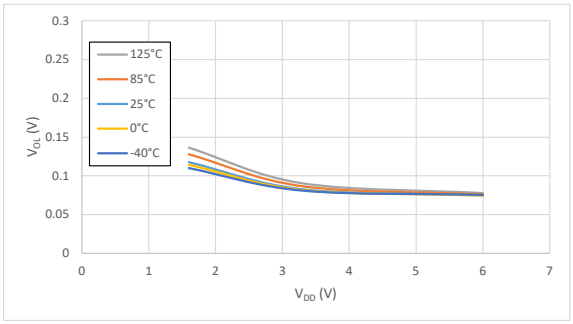


Figure 4. Low-level Reset Voltage vs Supply Voltage

Detailed Description

Overview

The TPV8308 is a family of supervisory circuits to monitor a voltage rail from 0.4 V to 5 V, asserting an active low/active high open-drain or push-pull $\overline{\text{RESET}}$ /RESET output when the voltage of the sense pin drops below a fixed threshold or when the manual reset pin $\overline{\text{MR}}$ is logic low. The $\overline{\text{RESET}}$ /RESET output remains low/high for the user-adjusted delay time by an external capacitor after the sense voltage returns above the fixed threshold with a hysteresis and the manual reset $\overline{\text{MR}}$ return to logic high.

Functional Block Diagram

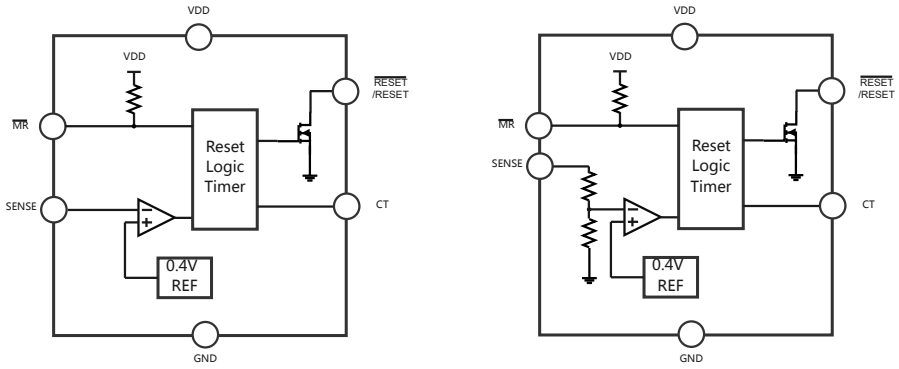


Figure 5. Functional Block Diagram

Feature Description

RESET Output

The reset threshold voltage can be set by the factory from 0.8 V to 4.2 V or be set to any voltage above 0.405 V using an external resistor divider. The sense pin monitors the system voltage. If the voltage on this pin drops below V_{IT}, the $\overline{\text{RESET}}$ /RESET is asserted.

The TPV8308 features an active-low or active-high output. For active-low output, the reset signal is guaranteed to be logic low for VSENSE down to V_{IT}. For active-high output, the reset signal is guaranteed to be logic high for VSENSE down to V_{IT}. Reset remains asserted for the duration of the reset delay time (t_D) after VSENSE rises above the reset threshold. Figure 6 shows the reset outputs.

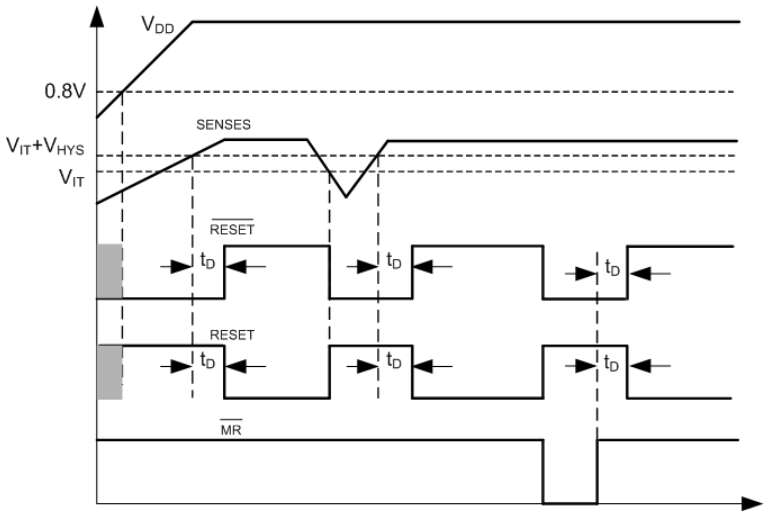


Figure 6. SENSE Reset and MR Reset Timing

RESET Delay Time

The TPV8308 provides programmable reset delay time (t_D), which is realized by selecting a capacitor between CT and GND to allow the designer to set any reset delay time from 1.25 ms to 10 s. The reset delay time (t_D) under a given capacitor value is calculated using Equation 1.

$$t_D\,(\mu s) = 6 \times C_{CT}\,(pF) + 500\ \ (\mu s) \quad (1)$$

Manual RESET ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a microcontroller to initiate a reset. A logic low on $\overline{MR}$ causes $\overline{RESET}$ to assert. After $\overline{MR}$ returns to logic high and SENSE is above the reset threshold, $\overline{RESET}$ is de-asserted after the reset delay time. $\overline{MR}$ can be left unconnected if not used.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Figure 7 shows the typical application circuit of TPV8308 with a reset threshold voltage set by the external resistor divider. Figure 8 shows the application circuit of TPV8308 with the reset threshold voltage set by the factory.

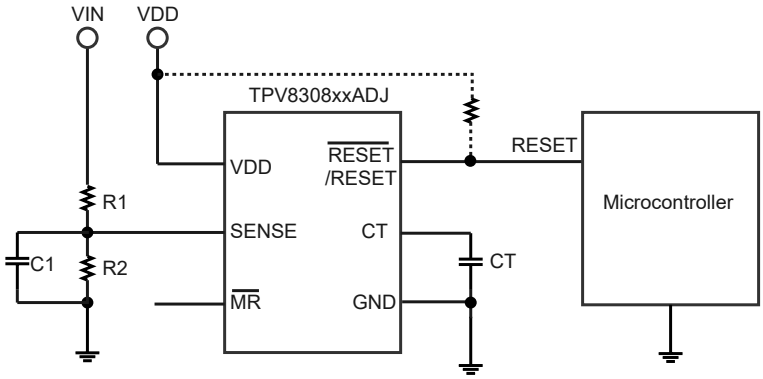


Figure 7. TPV8308 Adjustable Version Typical Application Circuit

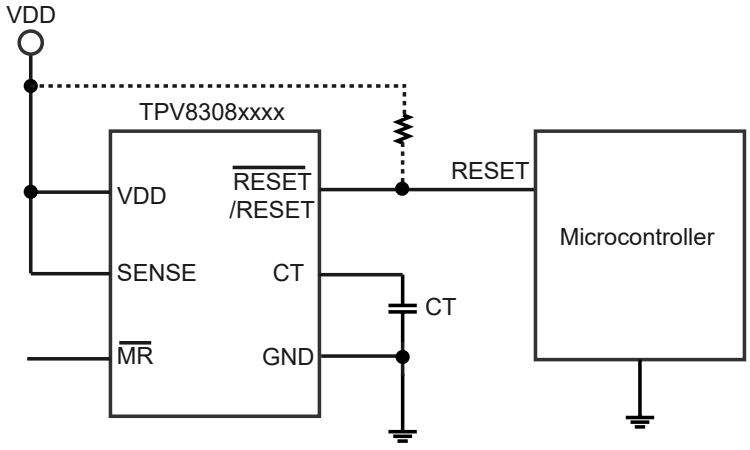
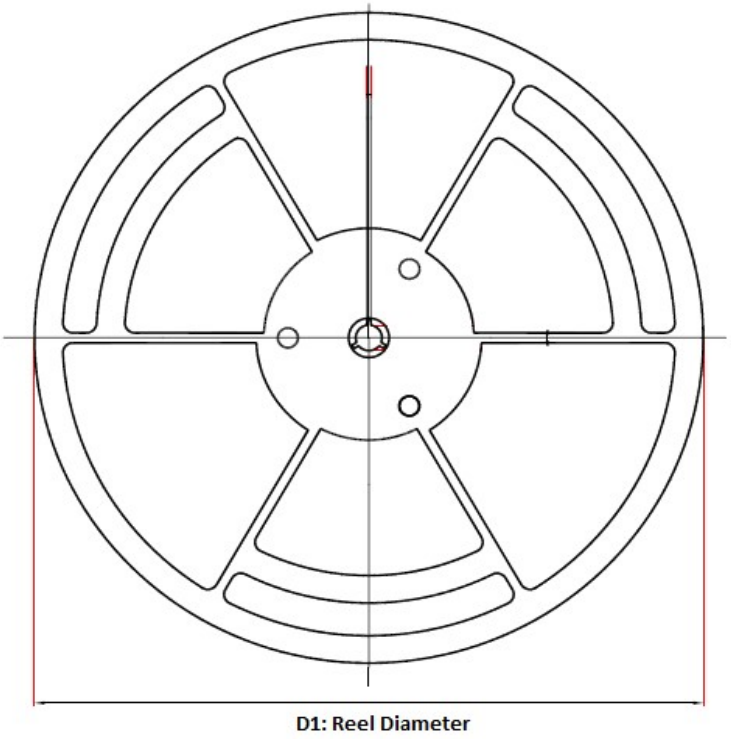
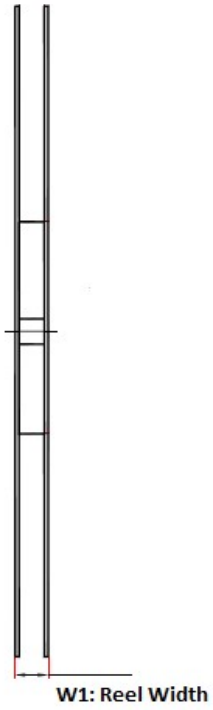
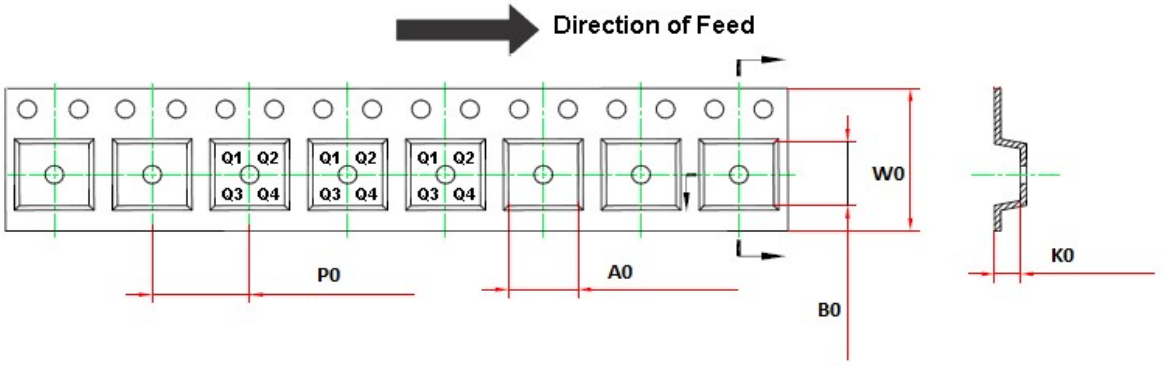


Figure 8. TPV8308 Fixed Version Typical Application Circuit

Tape and Reel Information





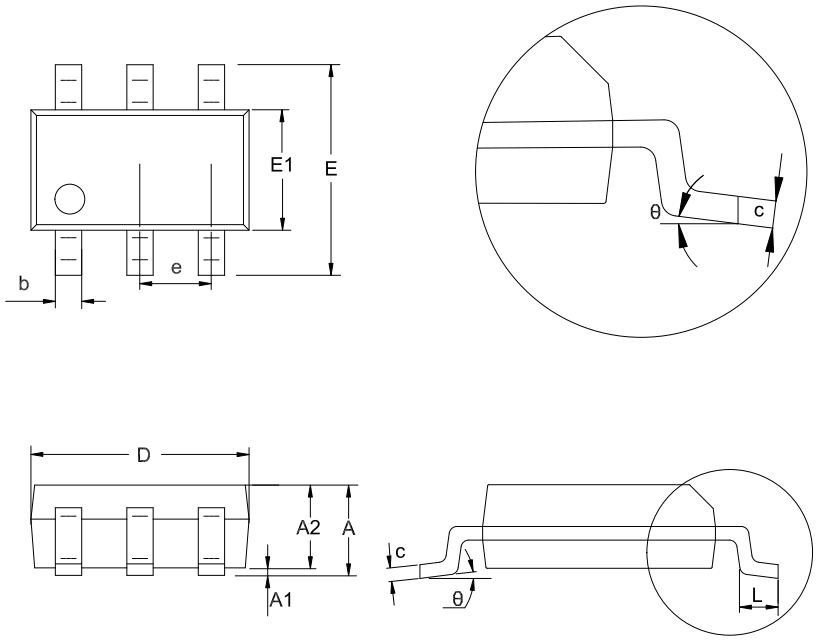


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPV8308xxxxx-S6TR	SOT23-6	178	12.3	3.2	3.2	1.4	4	8	Q3
TPV8308xxxx-DFOR	DFN2X2-6	180	13.1	2.3	2.3	1.1	4	8	Q1

Package Outline Dimensions

SOT23-6

Package Outline Dimensions S6T(SOT23-6-A)



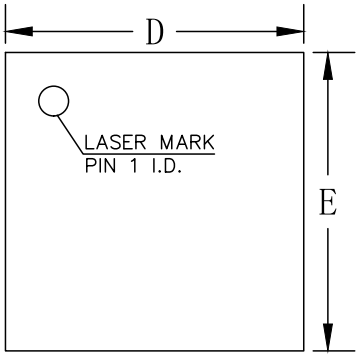
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

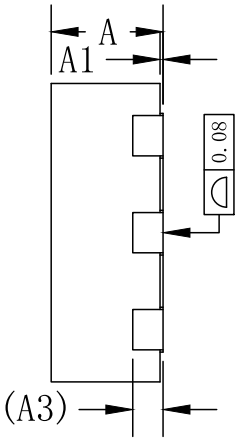
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN2X2-6

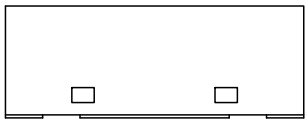
Package Outline Dimensions DFO(DFN2X2-6-B)



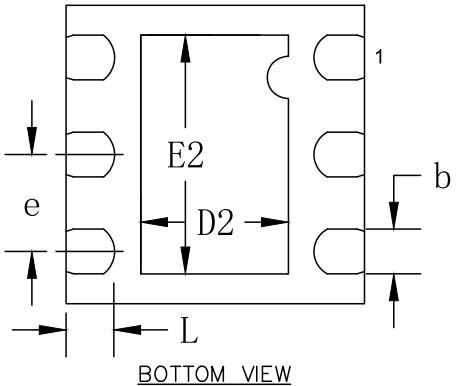
TOP VIEW



SIDE VIEW



SIDE VIEW



BOTTOM VIEW

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
A3	0.150	0.250	0.006	0.010
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D2	0.600	0.800	0.024	0.031
E2	1.100	1.300	0.043	0.051
e	0.650 BSC		0.026 BSC	
L	0.274	0.426	0.011	0.017

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPV8308LDADJ-S6TR	−40 to 125°C	SOT23-6	LDJ	3	Tape and Reel, 3000	Green
TPV8308LD080-S6TR (1)	−40 to 125°C	SOT23-6	X09	3	Tape and Reel, 3000	Green
TPV8308LD160-S6TR	−40 to 125°C	SOT23-6	X16	3	Tape and Reel, 3000	Green
TPV8308LD170-S6TR (1)	−40 to 125°C	SOT23-6	X17	3	Tape and Reel, 3000	Green
TPV8308LD220-S6TR (1)	−40 to 125°C	SOT23-6	X24	3	Tape and Reel, 3000	Green
TPV8308LD270-S6TR (1)	−40 to 125°C	SOT23-6	X27	3	Tape and Reel, 3000	Green
TPV8308LD300-S6TR (1)	−40 to 125°C	SOT23-6	X30	3	Tape and Reel, 3000	Green
TPV8308LD400-S6TR (1)	−40 to 125°C	SOT23-6	X40	3	Tape and Reel, 3000	Green
TPV8308LD420-S6TR (1)	−40 to 125°C	SOT23-6	X42	3	Tape and Reel, 3000	Green
TPV8308HDADJ-S6TR (1)	−40 to 125°C	SOT23-6	HDJ	3	Tape and Reel, 3000	Green
TPV8308LPADJ-S6TR (1)	−40 to 125°C	SOT23-6	LPJ	3	Tape and Reel, 3000	Green
TPV8308HPADJ-S6TR (1)	−40 to 125°C	SOT23-6	HPJ	3	Tape and Reel, 3000	Green
TPV8308LDADJ-DFOR (1)	−40 to 125°C	DFN2X2-6	DDJ	3	Tape and Reel, 3000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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单击下面可查看定价，库存，交付和生命周期等信息

>>3PEAK(思瑞浦)