

Features

- Supply Voltage: 2.3 V to 3.6 V
- 5-V Tolerant I/Os with Device Power-up or Power-down
- Device Isolation during Power-off
- Low On-State Resistance: Typical 4 Ω at $V_{CC} = 3\text{ V}$
- Bandwidth: 400 MHz
- Break-Before-Make Switching
- Operation Temperature Range: -40°C to 125°C

Applications

- SPI Routing
- Server
- Video Signal Routing
- Computer

Description

The TPW3257 device is a high-bandwidth bus switch utilizing a charge pump to provide low and flat on-state resistance.

The TPW3257 can be used to multiplex and de-multiplex up to 4 channels simultaneously in a 2:1 configuration. The $\overline{\text{OE}}$ and S pins are used to control the chip by the bus controller.

The device has isolation during power-off even when the signal exits the switch pins.

The V_{CC} operating range is from 2.3 V to 3.6 V and the switch pins support 0-V to 5-V signal levels.

Typical Application Circuit

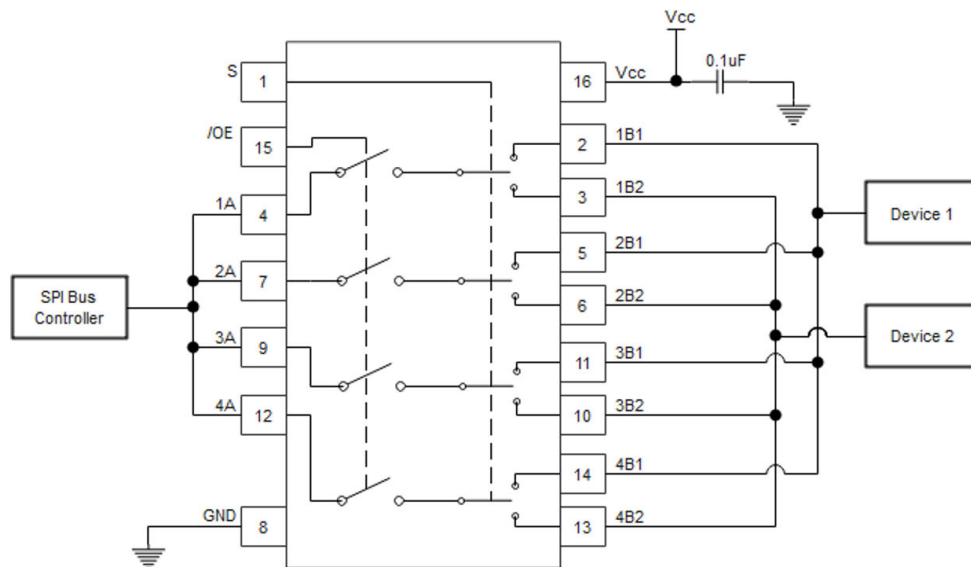


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Revision History

Date	Revision	Notes
2021-09-20	Rev.A.0	Initial version
2024-12-04	Rev.A.1	Added the layout information Updated the Order Information. The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. Updated to a new datasheet format. Updated the Tape and Reel Information. Updated the Package Outline Dimensions.

Pin Configuration and Functions

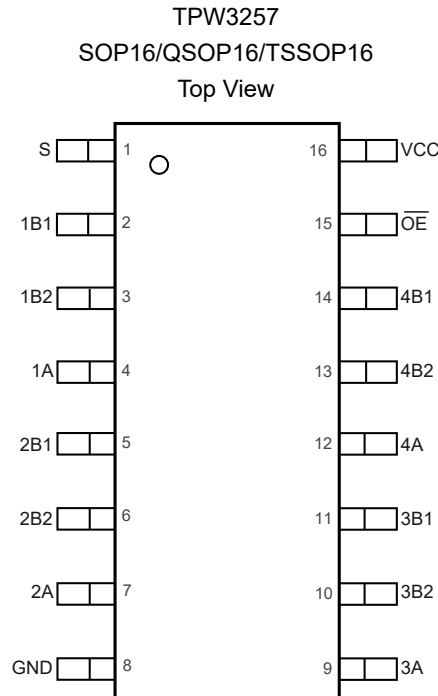


Table 1. Pin Functions: TPW3257

Pin No.	Name	I/O	Description
1	S	I	Select pin
2	1B1	I/O	Channel 1 I/O 1
3	1B2	I/O	Channel 1 I/O 2
4	1A	I/O	Channel 1 I/O common
5	2B1	I/O	Channel 2 I/O 1
6	2B2	I/O	Channel 2 I/O 2
7	2A	I/O	Channel 2 I/O common
8	GND		Ground
9	3A	I/O	Channel 3 I/O common
10	3B2	I/O	Channel 3 I/O 2
11	3B1	I/O	Channel 3 I/O 1
12	4A	I/O	Channel 4 I/O common
13	4B2	I/O	Channel 4 I/O 2
14	4B1	I/O	Channel 4 I/O 1
15	$\overline{\text{OE}}$	I	Output enable (active low)
16	V _{CC}		Power

Table 2. Functional Table

$\overline{\text{OE}}$	S	Input/Output A	Function
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

(1) X = Don't care.

Specifications

Absolute Maximum Ratings ⁽¹⁾

Parameter		Min	Max	Unit
	Supply Voltage, V_{CC}	-0.5	4.6	V
	Bus Switch Voltage	-0.5	7	V
	Bus Switch Current	-100	100	mA
	Bus Switch Diode Current		50	mA
	Digital Input Voltage, \overline{OE} , S	-0.5	7	V
	Digital Input Diode Current		50	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	-65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions ⁽¹⁾

All test conditions: over operating temperature range, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	2.3		3.6	V
	Transition Rise and Fall Rate for Control Input			100	ns/V
	Switch I/O Port Voltage	0		5.5	V
T_A	Operating Temperature Range	-40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
QSOP16	100	50	°C/W

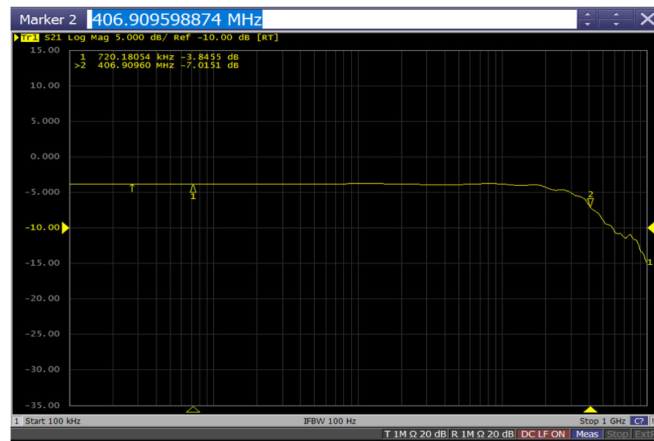
Electrical Characteristics

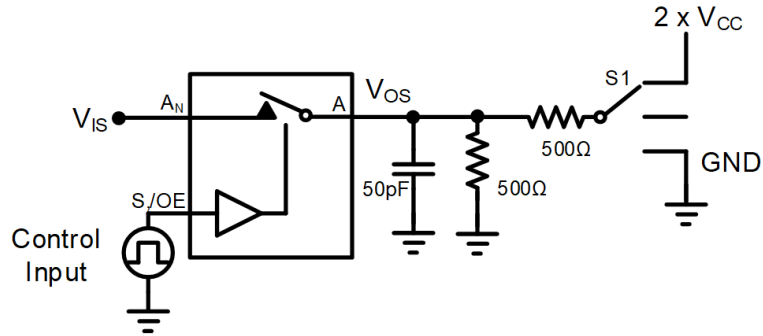
 All test conditions: $T_A = -40$ to 125°C , all typical values are at $T_A = 25^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
I_{CC}	Quiescent Supply Current	$V_{CC} = 3.6\text{ V}$, $V_{IN} = 0\text{ V}$ or V_{CC}			1.5	mA
ΔI_{CC}	Increase in Supply Current	$V_{CC} = 3.6\text{ V}$, $V_{IN} = 3.0\text{ V}$			30	μA
Digital Input (V_{IN})						
V_{IH}	Input Voltage High	$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.7		5.5	V
V_{IL}	Input Voltage Low	$V_{CC} = 2.3\text{ V}$ to 2.7 V			0.7	V
V_{IH}	Input Voltage High	$V_{CC} = 2.7\text{ V}$ to 3.6 V	2		5.5	V
V_{IL}	Input Voltage Low	$V_{CC} = 2.7\text{ V}$ to 3.6 V			0.8	V
I_{IN}	Control Input Leakage	$V_{IN} = 0\text{ V}$ or V_{CC}			± 1	μA
Analog Switch						
R_{ON}		$V_{CC} = 2.3\text{ V}$, $I_{OUT} = 30\text{ mA}$, $V_{IS} = 0\text{ V}$	4		8	Ω
		$V_{CC} = 2.3\text{ V}$, $I_{OUT} = -15\text{ mA}$, $V_{IS} = 1.7\text{ V}$	4		9	Ω
		$V_{CC} = 3\text{ V}$, $I_{OUT} = 30\text{ mA}$, $V_{IS} = 0\text{ V}$	4		6	Ω
		$V_{CC} = 3\text{ V}$, $I_{OUT} = -15\text{ mA}$, $V_{IS} = 2.4\text{ V}$	4		8	Ω
I_{OZ}	Switch OFF Leakage Current on Channel	$V_{CC} = 3.6\text{ V}$, $V_{OS} = 0$ to 5.5 V , $V_{IS} = 0$			± 1	μA
I_{OFF}	Switch OFF Leakage Current on Common	V_{CC} floating, $V_{OS} = 0$ to 5.5 V , $V_{IS} = 0$			± 1	μA
Dynamic Characteristics, $V_{CC} = 2.5\text{ V}$						
t_{PD}		From A to B or B to A		0.2		ns
$t_{PD(S)}$		From S to A or B		5		ns
		From S to A or B, $T_A = -40^\circ\text{C}$ to 125°C		10		ns
t_{EN}		From \overline{OE} to A or B		5		ns
		From \overline{OE} to A or B, $T_A = -40^\circ\text{C}$ to 125°C		10		ns
t_{OFF}		From \overline{OE} to A or B		5		ns
		From \overline{OE} to A or B, $T_A = -40^\circ\text{C}$ to 125°C		10		ns
Dynamic Characteristics, $V_{CC} = 3.3\text{ V}$						
t_{PD}		From A to B or B to A		0.2		ns
$t_{PD(S)}$		From S to A or B		5		ns

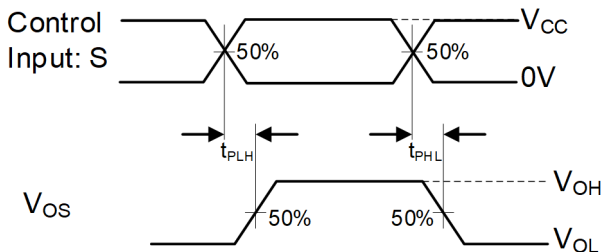
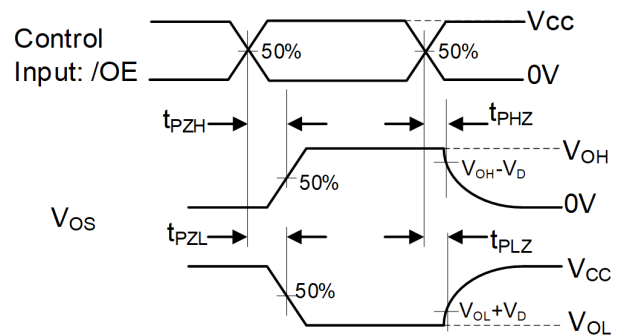
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		From S to A or B, $T_A = -40^\circ\text{C}$ to 125°C		8		
t_{EN}		From \overline{OE} to A or B		5		ns
		From \overline{OE} to A or B, $T_A = -40^\circ\text{C}$ to 125°C		8		
t_{OFF}		From \overline{OE} to A or B		5		ns
		From \overline{OE} to A or B, $T_A = -40^\circ\text{C}$ to 125°C		8		
BW	Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$		400		MHz
Capacitance						
C_{IN}	Control Input Capacitance	$V_{CC} = 3.3\ \text{V}$		5		pF
$C_{IO(ON)}$	Switch On Capacitance	$V_{CC} = 3.3\ \text{V}$		15		pF
$C_{IO(OFF)}$	Switch Off Capacitance	$V_{CC} = 3.3\ \text{V}$		5		pF

Typical Performance Characteristics

Figure 1. Bandwidth, $V_{CC} = 3.3$ V

Test Circuit and Waveforms


Test	V _{CC}	S1	V _{IS}	C _L	V _D
t _{PD(S)}	2.5	Open	V _{CC} or GND	30pF	
	3.3	Open	V _{CC} or GND	50pF	
t _{PLZ} /t _{PZL}	2.5	2 × V _{CC}	GND	30pF	0.15V
	3.3	2 × V _{CC}	GND	50pF	0.3V
t _{PHZ} /t _{PZH}	2.5	GND	V _{CC}	30pF	0.15V
	3.3	GND	V _{CC}	50pF	0.3V


 Test waveforms for t_{PD(S)}: t_{PLH} or t_{PHL}

 Test waveforms for t_{EN} and t_{OFF}
 t_{EN}: t_{PZH} or t_{PZL}, t_{OFF}: t_{PHZ} or t_{PLZ}

Detailed Description

Overview

The TPW3257 device is a high-bandwidth bus switch using a charge pump to provide higher voltage for the internal circuit than the input power voltage (V_{CC}). The design provides low and flat on-state resistance and low switch I/O capacitance, which allows for minimal propagation delay and supports high-bandwidth applications.

The TPW3257 device is organized as two 1-of-4 multiplexers/demultiplexers with single output-enable input (\overline{OE}) and single select input (S) control the data path of each multiplexer/demultiplexer. When \overline{OE} is low, the switch is enabled, and bidirectional data flow between A and B ports is allowed. When \overline{OE} is high, the switch is disabled, and a high-impedance state exists between the A and B ports.

Functional Block Diagram

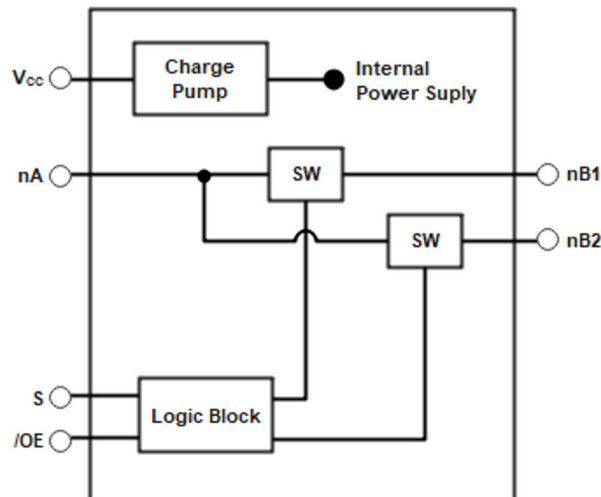


Figure 2. Functional Block Diagram

Feature Description

Over-Power Rail Input for Switch

This device with an internal charge pump has switching pass ability on data I/O ports for 0-V to 5-V switching with 3.3 V V_{CC} and for 0-V to 3.3-V switching with 2.5 V V_{CC} .

Isolation during Power-off

The device has isolation during power-off. The internal circuit prevents current flow when the device is powered down and the voltage is still applied at A, B ports, or control inputs (S, \overline{OE}).

\overline{OE} should be tied to V_{CC} through a pull-up resistor to ensure the high-impedance state during power-up or power-down.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPW3257 device can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration. Figure 3 is a 4-bit bus being multiplexed between two devices. The control inputs (\overline{OE} and S) are used to control the device by the bus controller. If an application requires less than 4 channels, the unused channels of A port should tie to either high or low.

Typical Application

Figure 3 shows the typical application schematic.

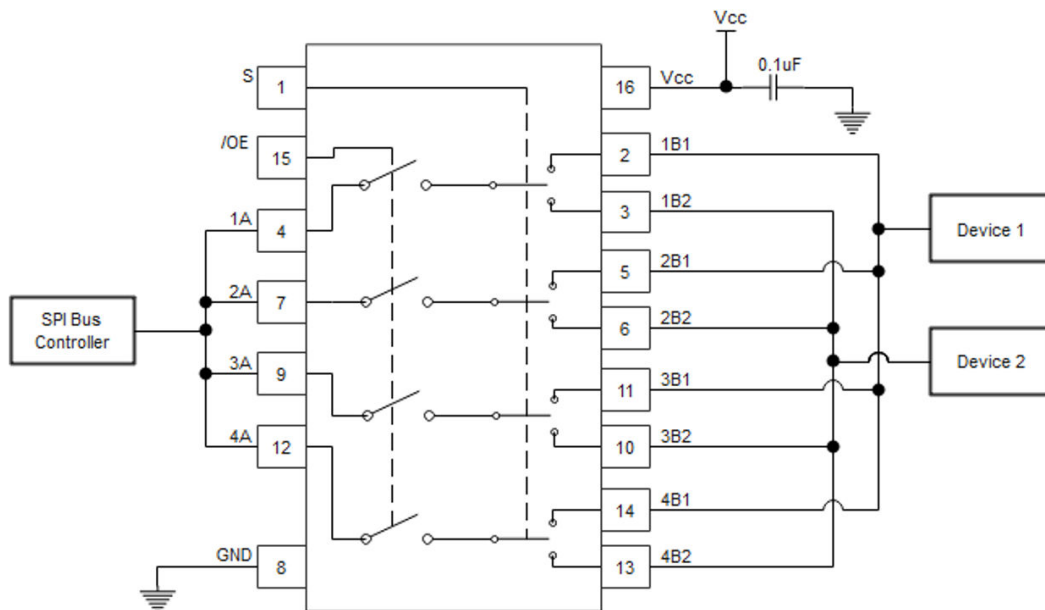


Figure 3. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to the loop antenna theory. But the differences warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in width of the trace. At the apex of the turn, the trace width increases to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in reflection. Not all PCB traces can be straight, so they have to turn corners. Figure 4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

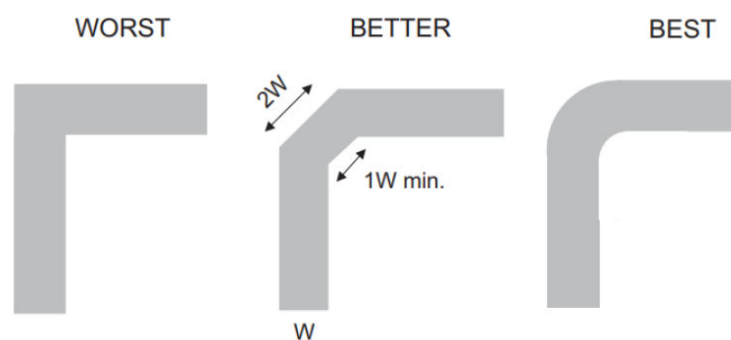
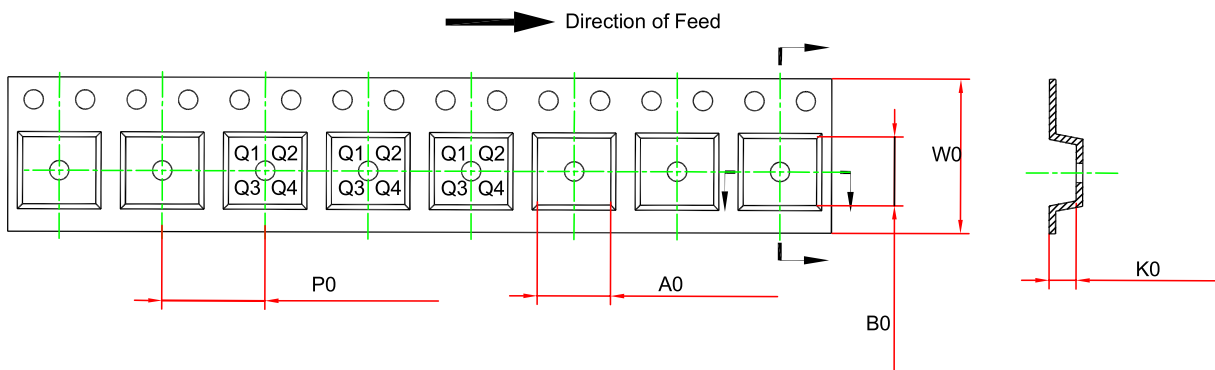
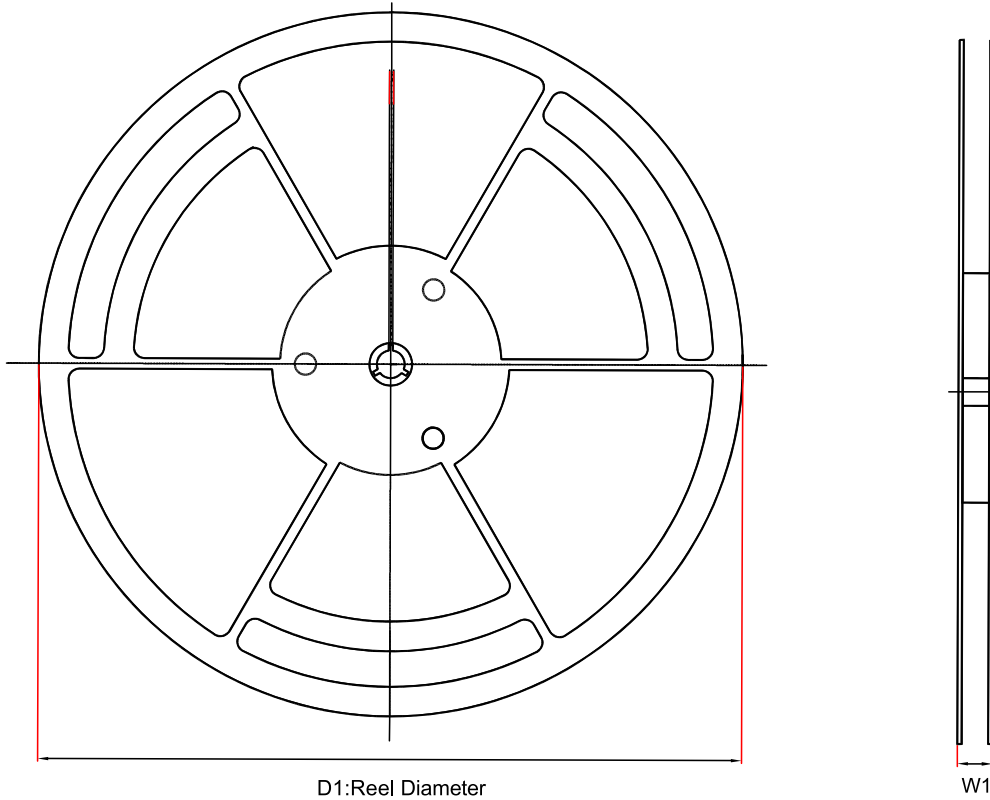


Figure 4. Trace Example

Route high-speed signals use a minimum of vias and corners which reduces signal reflections and impedance changes. When a via is necessary, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points. Through-hole pins are not recommended at high frequencies.

Tape and Reel Information

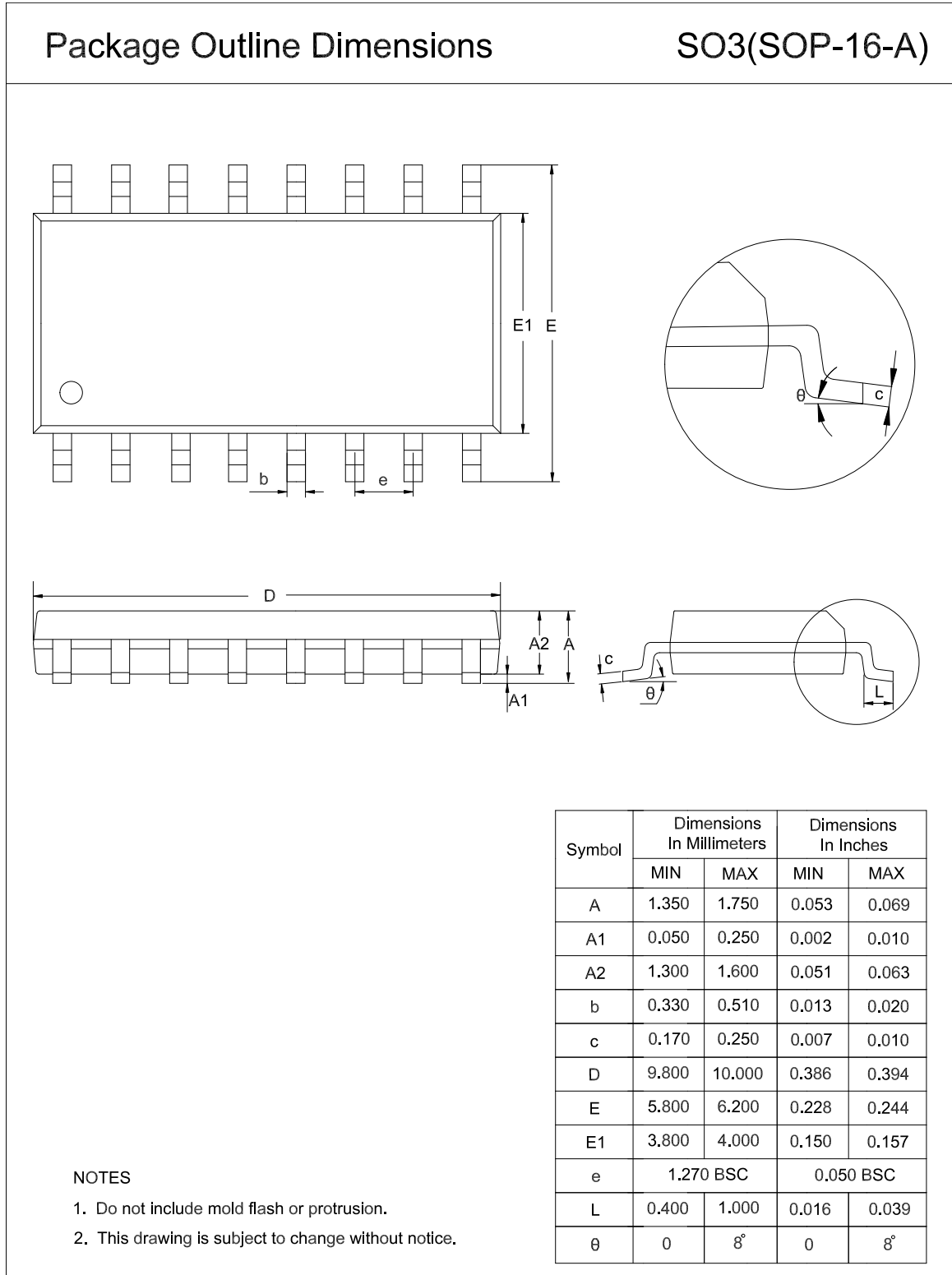


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) ⁽¹⁾	B0 (mm) ⁽¹⁾	K0 (mm) ⁽¹⁾	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPW3257-SO3R	SOP16	330	21.6	6.6	10.4	2.1	8	16	Q1
TPW3257-TS3R	TSSOP16	330	17.6	6.8	5.5	1.5	8	12	Q1
TPW3257-SS3R	QSOP16	330	17.6	6.5	5.4	2.0	8	12	Q1

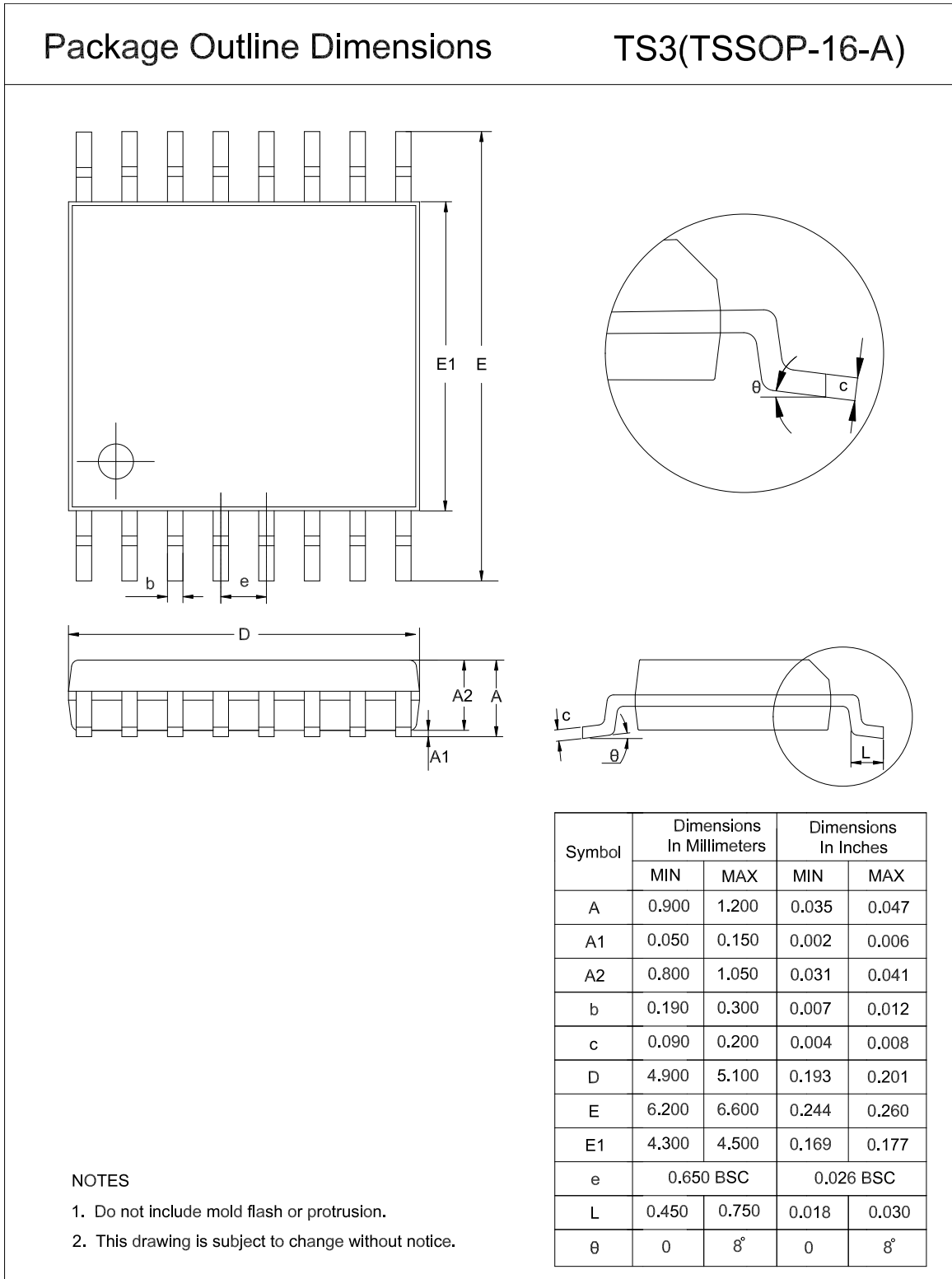
(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

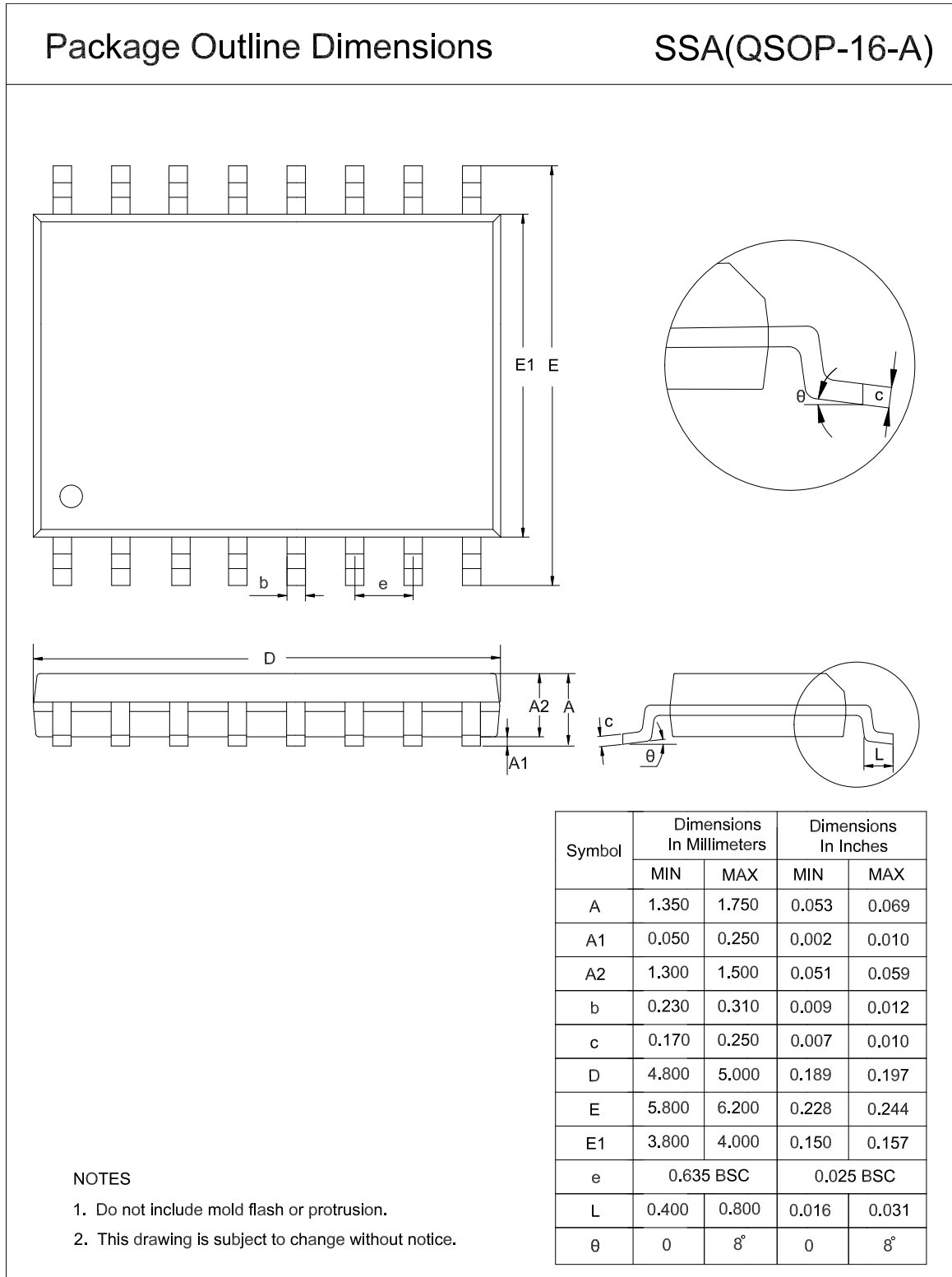
SOP16



TSSOP16



QSOP16



Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPW3257-SO3R	-40 to 125°C	SOP16	W3257	3	Tape and Reel, 4000	Green
TPW3257-TS3R	-40 to 125°C	TSSOP16	W3257	3	Tape and Reel, 4000	Green
TPW3257-SS3R ⁽¹⁾	-40 to 125°C	QSOP16	W3257	3	Tape and Reel, 4000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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