Features

- **Precision low voltage monitoring and Power Fail detector**
- **200 ms (typical) reset timeout**
- **Manual reset input**
- **Independent watchdog timer**
- **Reset output stage**
- **Push-pull Active-low output (TPV706)**
- **Low power consumption: 4 µA**
- **Guaranteed reset output valid to VCC = 1 V**
- **Power supply glitch immunity**
- **Specified from −40°C to +125°C**
- **8-lead SOP package**

Applications

- **Microprocessor systems**
- **Computers**
- **Controllers**
- **Intelligent instruments**
- **Portable equipment**

Description

The TPV706 is a supervisory circuit that monitors power supply voltage levels and provides a power-on reset signal.

A watchdog monitor is provided, which is activated if the watchdog input doesn't toggle within 1.6 sec.

A reset signal can also be asserted by an external manual reset input.

In addition, there is a power fail detector with 1.25V threshold, which can be used to monitor an additional power supply.

The reset periods are fixed at 200 ms (typical).

The TPV706 is available in a 8-lead SOP package and typically consumes only 4 µA, suitable for use in low power, portable applications.

Function block diagram

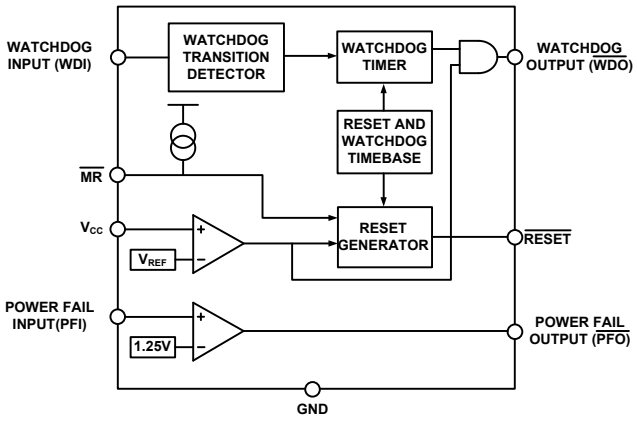

Figure 1.

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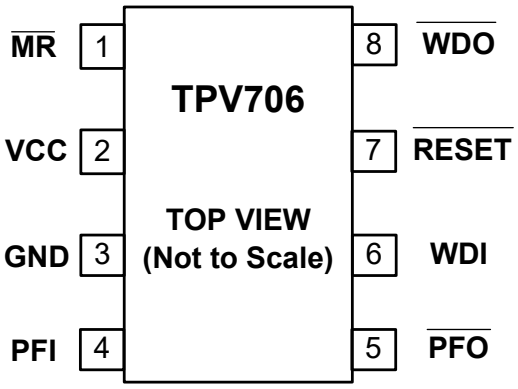
Revision History

Table 1.

Date	Revision	Notes
2019/1/1	Rev.A.01	Initial version
2019/5/28	Rev.A.02	Add WDI pulse interval spec

Pin Configuration and Functions



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Name	PIN NO	Description
$\overline{MR}$	1	Manual Reset Input. This is an active-low input, which generates a reset when forced low for at least 1 μs. It features an internal pull-up current.
Vcc	2	Power Supply Voltage being Monitored.
GND	3	Ground.
PFI	4	Power Fail Input. When PFI is less than 1.25 V, PFO goes low. If unused, connect PFI connects to GND.
$\overline{PFO}$	5	Power-Fail Output. It goes low when PFI is less than 1.25V; otherwise stays high.
WDI	6	Watchdog Input. Generates a reset if the voltage on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated. Floating WDI disables the watchdog function.
$\overline{RESET}$	7	Active-Low Reset Push-Pull Output Stage. Asserted whenever VCC is below the reset threshold or by a low signal on the $\overline{MR}$ input. It remains low for 200mS after VCC goes above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout does not trigger $\overline{RESET}$.
$\overline{WDO}$	8	Watchdog Output. Pulls low if WDI remains low or high for the duration of the watchdog timeout, and does not go high again until the watchdog is cleared. Whenever VCC is below the reset threshold, $\overline{WDO}$ stays low. As soon as VCC rises above the reset threshold, $\overline{WDO}$ goes high with no delay.

Order Information

Table 2.

Model Name	Order Number	Package	Transport Media, Quantity	Package Marking
TPV706	TPV706VL1-SR	SOP-8	Tape and Reel, 4,000	V6V

TPV706	TPV706WL1-SR	SOP-8	Tape and Reel, 4,000	V6W
TPV706	TPV706YL1-SR	SOP-8	Tape and Reel, 4,000	V6Y
TPV706	TPV706ZL1-SR	SOP-8	Tape and Reel, 4,000	V6Z
TPV706	TPV706RL1-SR	SOP-8	Tape and Reel, 4,000	V6R
TPV706	TPV706SL1-SR	SOP-8	Tape and Reel, 4,000	V6S
TPV706	TPV706TL1-SR	SOP-8	Tape and Reel, 4,000	V6T
TPV706	TPV706ML1-SR	SOP-8	Tape and Reel, 4,000	V6M
TPV706	TPV706LL1-SR	SOP-8	Tape and Reel, 4,000	V6L

Absolute Maximum Ratings

Table 3

Parameter	Rating
VCC	−0.3 V to 6 V
Output Current	20 mA
Operating Temperature Range	−40°C to 125°C
Storage Temperature Range	−65°C to 150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Table 4

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	4000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	2000	V

Electrical Characteristics

VCC = 1.53 V to 5.5V; TA = –40°C to +125°C, unless otherwise noted.

Table 5

TPV706			SPEC		
Parameter	Test conditions	Unit	Min	Typ	Max
VCC Operating Voltage Range		V	1		5.5
Supply Current	WDI and MR unconnected (VCC=1.8V)	μA		4	15
	WDI and MR unconnected (VCC=5V)	μA		6	20
RESET THRESHOLD VOLTAGE					
TPV706V	Vth	V	1.51	1.58	1.63
TPV706W	Vth	V	1.62	1.67	1.71
TPV706Y	Vth	V	2.12	2.19	2.25
TPV706Z	Vth	V	2.25	2.32	2.38
TPV706R	Vth	V	2.55	2.63	2.70
TPV706S	Vth	V	2.82	2.93	3.00
TPV706T	Vth	V	3.00	3.08	3.15
TPV706M	Vth	V	4.25	4.38	4.5
TPV706L	Vth	V	4.5	4.63	4.75
RESET THRESHOLD TEMPERATURE COEFFICIENT		ppm/°C		80	
RESET THRESHOLD HYSTERESIS		mV		2 × VTH	
VCC TO RESET DELAY	VTH − VCC = 100 mV	μs		20	
RESET TIMEOUT PERIOD		ms	140	200	280
RESET OUTPUT VOLTAGE VOL (Push-Pull)	VCC ≥ 1 V, ISINK = 50 μA	V			0.3
	ISINK = 1.2mA @ Vcc≥2V	V			0.4
RESET OUTPUT VOLTAGE VOH (Push-Pull Only)	ISOURCE = 800 μA, @ Vcc≥5V	V	0.7 × VCC		
MR Input Threshold VIL		V			0.3 × VCC
MR Input Threshold VIH		V	0.7 × VCC		
MR Input Pulse Width		μS	6		
MR Glitch Rejection		nS		100	
MR to Reset Delay		μS		1	6
MR Pull-Up Current	VCC = 3V	μA		80	

VCC = 1.53 V to 5.5V; TA = –40°C to +125°C, unless otherwise noted.

TPV706			SPEC		
Parameter	Test conditions	Unit	Min	Typ	Max
Watchdog Timeout Period		sec	1	1.6	2.4
WDI Pulse Width 50 ns		nS	50		
WDI Pulse Interval		mS	12		
WDI Input Threshold VIL		V			0.3 × VCC
WDI Input Threshold VIH		V	0.7 × VCC		
WDI Input Current	VWDI = VCC	μA		20	
	VWDI = 0	μA		-15	
$\overline{WDO}$ V_{OL}	ISINK = 1.2mA @ Vcc≥5V	V			0.4V
$\overline{WDO}$ V_{OH}	ISOURCE = 800 μA @ Vcc≥5V	V	0.7*Vcc		
Power Fail input threshold	PFI falling	V	1.18	1.25	1.32
$\overline{PFO}$ V_{OL}	ISINK = 1.6mA @ Vcc≥5V	V			0.4V
$\overline{PFO}$ V_{OH}	ISOURCE = 800 μA @ Vcc≥5V	V	0.7*Vcc		

Typical Performance Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.

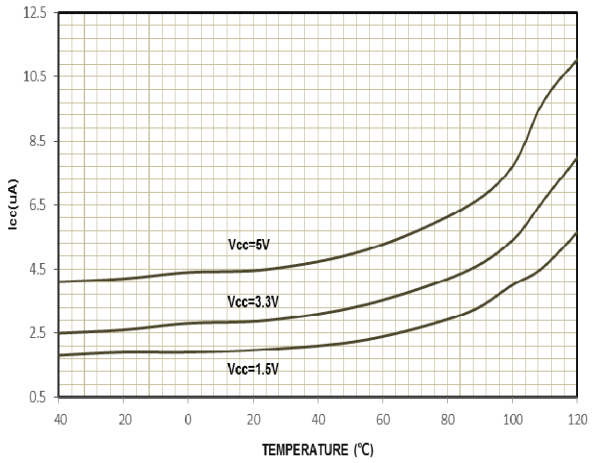


Figure 2. Supply Current vs. Temperature

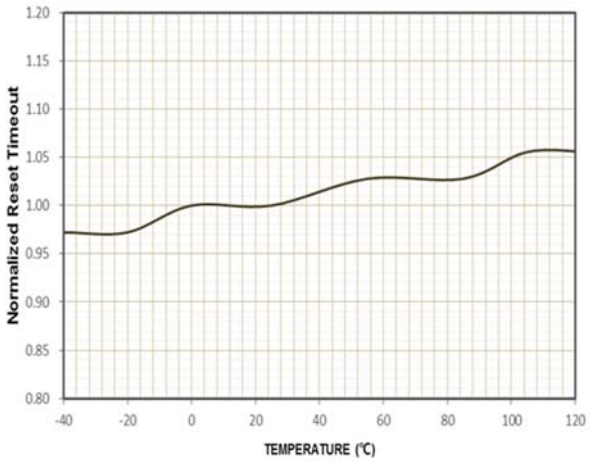


Figure 3. Normalized RESET Timeout Period vs. Temperature

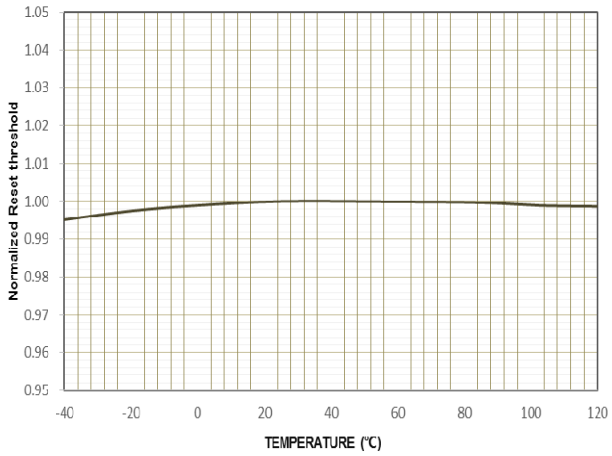


Figure 4. Normalized RESET Threshold vs. Temperature

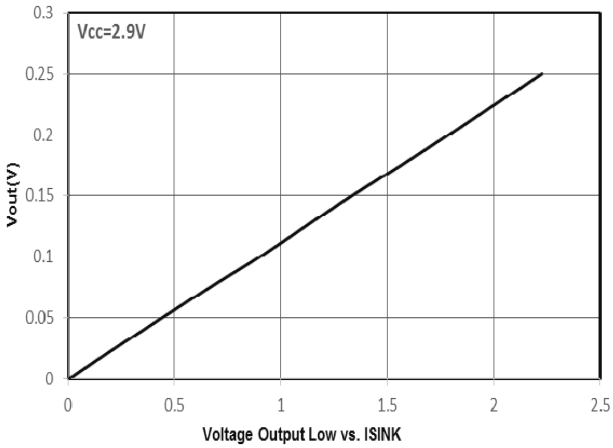


Figure 5. Voltage Output Low vs. ISINK

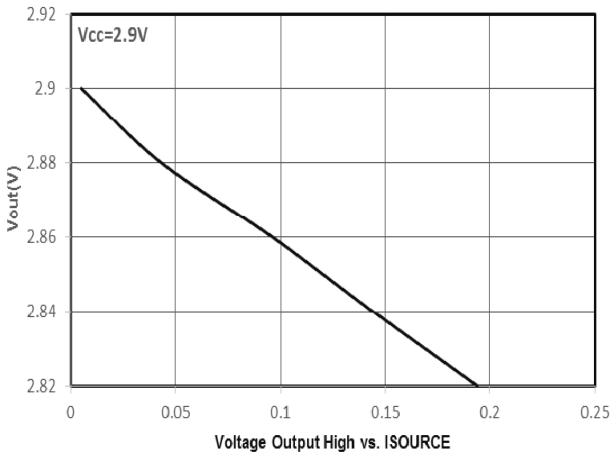


Figure 6. Voltage Output Low vs. ISOURCE

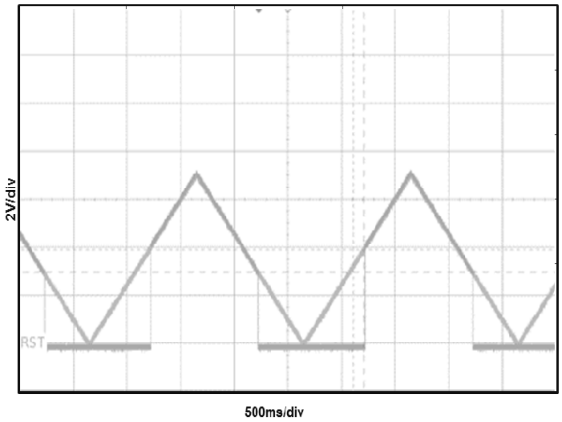


Figure 7. RESET Output Voltage vs. Supply Voltage

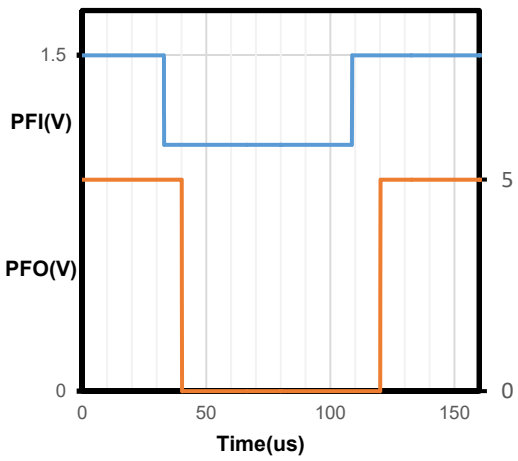


Figure 8. PFI vs. PFO

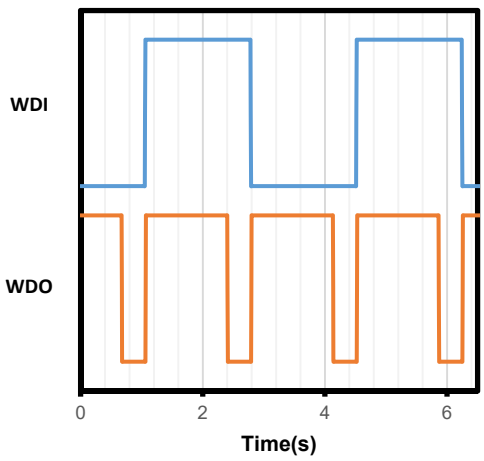


Figure 9. WDI vs. WDO

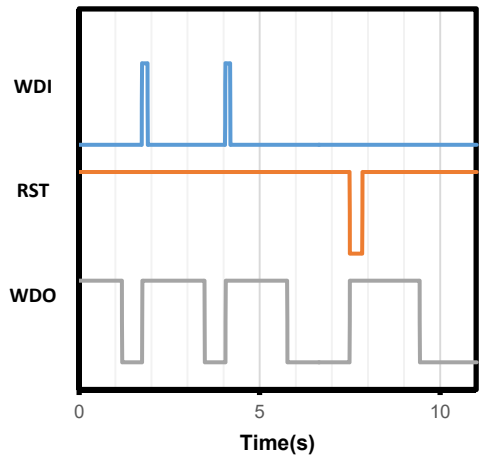


Figure 10. WDI vs. RST and WDO

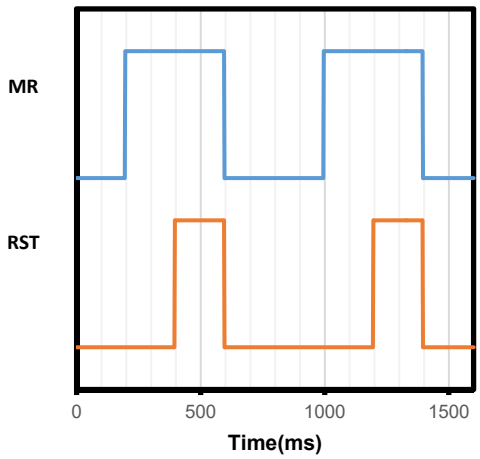


Figure 11. MR vs. RST

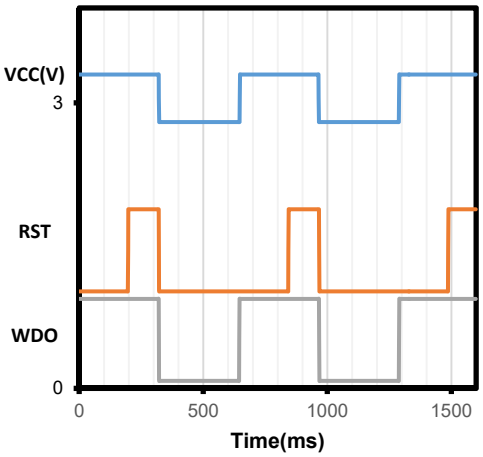


Figure 12. Vcc vs. RST and WDO

Theory of Operation

The TPV706 provides supply voltage supervision, watchdog function, manual reset function as well as a 1.25V power fail comparator.

RESET OUTPUT

The TPV706 features an active-low push-pull output. The reset signal is guaranteed to be logic low for VCC down to 1 V. The reset output is asserted when VCC is below the reset threshold (VTH), or when MR is driven low. Reset remains asserted for the duration of the reset active timeout period (tRP) after VCC rises above the reset threshold, or after MR transitions from low to high. Figure 10 shows the reset (active low) outputs.

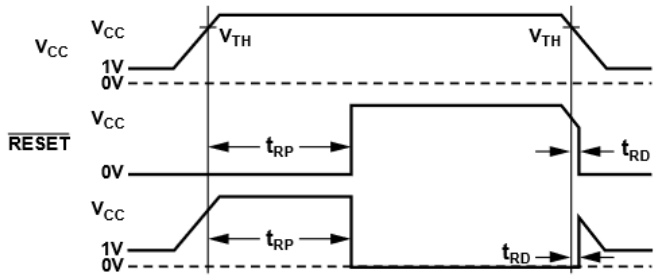


Figure 10. Reset Timing Diagram

MANUAL RESET INPUT

The TPV706 features a manual reset input (MR), which, when driven low, asserts the reset output. When MR transitions from low to high, reset remains asserted for the duration of the reset active timeout period before de-asserting.

The MR input has an internal pull-up current so that the input is always high when unconnected. Noise immunity is provided on the MR input, and fast, negative-going transients are ignored. A 0.1 μF capacitor between MR and ground provides additional noise immunity.

WATCHDOG INPUT

The TPV706 features a watchdog timer, which monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI). If the timer counts through the preset watchdog timeout period (tWD), reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset.

Whenever VCC is below the reset threshold, $\overline{\text{WDO}}$ stays low. As soon as VCC rises above the reset threshold, $\overline{\text{WDO}}$ goes high with no delay.

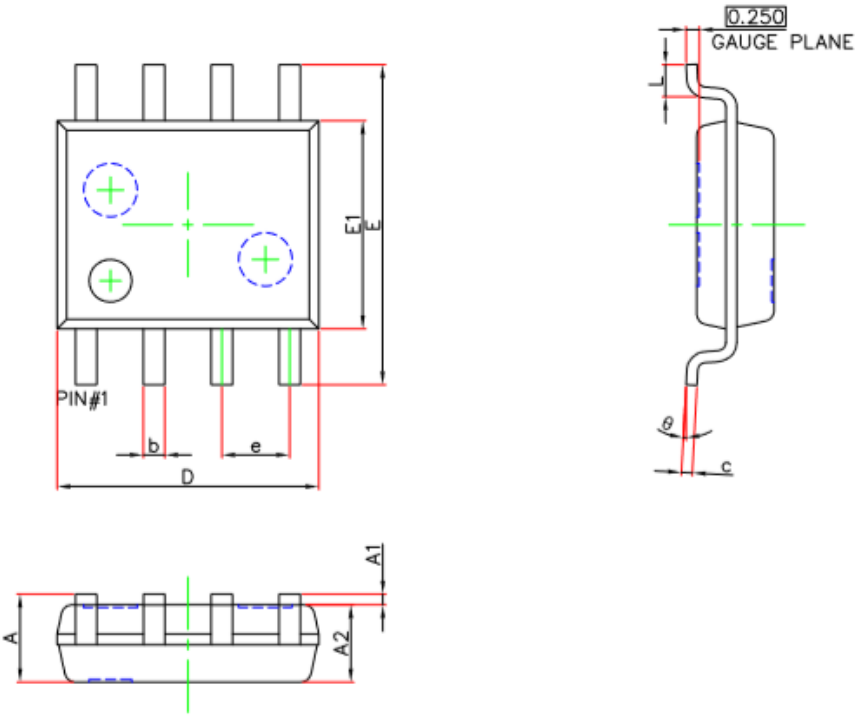
POWER FAIL COMPARATOR

The power fail comparator is a 1.25V comparator, which can monitor an external power supply through a resistive divider. When the voltage on the PFI is lower than1.25 V, the comparator output goes low, indicating a power failure, which can be used as early warning of power failure.

Package Outline Dimensions

SOP-8

SOP8(150mil)(12R) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

单击下面可查看定价，库存，交付和生命周期等信息

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