

Features

- General Purpose, Low Cost
- Gain Bandwidth Product: 1MHz
- Low Quiescent Current: 45µA/Amplifier
- Offset Voltage: 5.0mV Maximum
- Offset Voltage Temperature Drift: 2uV/°C
- Input Bias Current: 10pA
- CMRR/PSRR: 90dB
- Unity Gain Stable
- Rail-to-Rail Input and Output
- No Phase Reversal for Overdriven Inputs
- Supply Voltage Range: 2.1V to 6.0V
- Operation Range: -40°C to 125°C
- ESD Rating:
8kV – HBM, 2kV – CDM and 500V – MM
- Popular Type Package

Applications

- Audio Output
- Battery and Power Supply Control
- Smoke/Gas/Environment Sensors
- Medical Equipment
- Portable Instruments and Mobile Device
- Active Filters
- Piezo Electrical Transducer Amplifier
- Sensor Interface
- ASIC Input or Output Amplifier

Description

TP321/358/324 are general purpose single, dual and quad CMOS op-amps with low offset, high frequency response, low power, low supply voltage, and rail-to-rail inputs and outputs. They incorporate 3PEAK's proprietary and patented design techniques to achieve best in-class performance with low cost among all micro-power CMOS amplifiers.

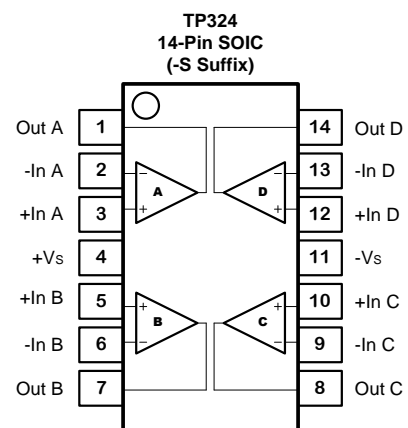
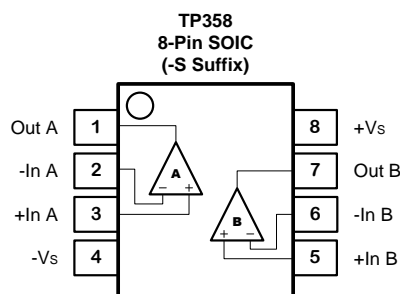
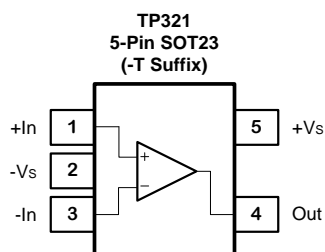
The TP321/358/324 are unity gain stable with a constant 1MHz gain-bandwidth product, 1V/µs slew rate while consuming only 45µA of supply current per amplifier. The rail-to-rail input and output characteristics allow the full power-supply voltage to be used for signal range.

This combination of features makes the TP321/358/324 superior and cost-effective among RRIO CMOS op-amps. The TP321/358/324 are ideal choices for battery-powered applications because they minimize errors due to power supply voltage variations over the lifetime of the battery and maintain high CMRR even for a rail-to-rail input op-amp.

The TP321/358/324 can be used as cost-effective plug-in replacements for many commercially available op amps to reduce power and improve input/output range and performance.

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Pin Configuration (Top View)



TP321/TP358/TP324

General Purpose, 1MHz, Micro-Power CMOS Op-Amps

Absolute Maximum Ratings Note 1

| | | | |
|---|----------------------------|--|----------------|
| Supply Voltage: $V^+ - V^-$ | 6.6V | Operating Temperature Range..... | -40°C to 125°C |
| Input Voltage..... | $V^- - 0.1$ to $V^+ + 0.1$ | Maximum Junction Temperature..... | 150°C |
| Input Current: +IN, -IN, SHDN <small>Note 2</small> | ± 10 mA | Storage Temperature Range..... | -65°C to 150°C |
| Output Current: OUT..... | ± 40 mA | Lead Temperature (Soldering, 10 sec) | 260°C |
| Output Short-Circuit Duration <small>Note 3</small> | Indefinite | | |

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

| Symbol | Parameter | Condition | Minimum Level | Unit |
|--------|--------------------------|----------------------------|---------------|------|
| HBM | Human Body Model ESD | MIL-STD-883H Method 3015.8 | 8 | kV |
| CDM | Charged Device Model ESD | JEDEC-EIA/JESD22-C101E | 2 | kV |
| MM | Machine Model ESD | JEDEC-EIA/JESD22-A115 | 500 | V |

Order and MSL Information

| Model Name | Order Number | Package | Transport Media, Quantity | Marking Information | MSL Level |
|------------|--------------|-------------|---------------------------|----------------------|-----------|
| TP321 | TP321-TR | 5-Pin SOT23 | Tape and Reel, 3000 | AT4YW ⁽¹⁾ | MSL 3 |
| TP358 | TP358-SR | 8-Pin SOIC | Tape and Reel, 4000 | A42S | MSL 3 |
| TP324 | TP324-SR | 14-Pin SOIC | Tape and Reel, 2500 | A44S | MSL 3 |

Note (1): 'YW' is date coding scheme. 'Y' stands for calendar year, and 'W' stands for single workweek coding scheme.

5V Electrical Characteristics

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 27^\circ\text{C}$.
 $V_{\text{SUPPLY}} = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = V_{\text{SUPPLY}}/2$, $R_L = 100\text{k}\Omega$, $C_L = 100\text{pF}$

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------|--|---|--------|------------|-------|------------------------------|
| V_{OS} | Input Offset Voltage | $V_{\text{CM}} = V_{\text{SUPPLY}}/2$ | ● -5.0 | ±0.8 | +5.0 | mV |
| $V_{\text{OS TC}}$ | Input Offset Voltage Drift | | | 2 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{B} | Input Bias Current | | | 10 | | μA |
| I_{OS} | Input Offset Current | | | 1.0 | | μA |
| e_n | Input Voltage Noise Density | $f = 1\text{kHz}$ $f = 10\text{kHz}$ | | 45 29 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| R_{IN} | Input Resistance | | >100 | | | $\text{G}\Omega$ |
| C_{IN} | Input Capacitance | Differential Common Mode | | 1.5 3.0 | | pF |
| CMRR | Common Mode Rejection Ratio | $V_{\text{CM}} = 0.1\text{V to } 4.9\text{V}$ | ● 80 | 90 | | dB |
| V_{CM} | Common-mode Input Voltage Range | | ● -0.1 | | ● 5.1 | V |
| PSRR | Power Supply Rejection Ratio | | ● 80 | 90 | | dB |
| A_{VOL} | Open-Loop Large Signal Gain | $V_{\text{OUT}} = 2.5\text{V}$, $R_{\text{LOAD}} = 100\text{k}\Omega$ | ● 80 | 97 | | dB |
| | | $V_{\text{OUT}} = 0.1\text{V to } 4.9\text{V}$, $R_{\text{LOAD}} = 100\text{k}\Omega$ | ● 72 | 95 | | |
| V_{OL} | Output Swing from Supply Rail | $R_{\text{LOAD}} = 100\text{k}\Omega$ | | 5 | | mV |
| I_{SC} | Output Short-Circuit Current | Sink or source current | | 40 | | mA |
| I_{Q} | Quiescent Current per Amplifier | | ● | 45 | 87 | μA |
| PM | Phase Margin | $R_{\text{LOAD}} = 100\text{k}\Omega$, $C_{\text{LOAD}} = 100\text{pF}$ | | 63 | | $^\circ$ |
| GM | Gain Margin | $R_{\text{LOAD}} = 100\text{k}\Omega$, $C_{\text{LOAD}} = 100\text{pF}$ | | -15 | | dB |
| GBWP | Gain-Bandwidth Product | $f = 1\text{kHz}$ | | 1.0 | | MHz |
| t_s | Settling Time, 1.5V to 3.5V, Unity Gain | 0.1% | | 2.3 | | μs |
| | | 0.01% | | 2.8 | | |
| | Settling Time, 2.45V to 2.55V, Unity Gain | 0.1% | | 0.33 | | |
| | | 0.01% | | 0.38 | | |
| SR | Slew Rate | $A_v = 1$, $V_{\text{OUT}} = 1.5\text{V to } 3.5\text{V}$, $C_{\text{LOAD}} = 100\text{pF}$, $R_{\text{LOAD}} = 100\text{k}\Omega$ | | 1.0 | | $\text{V}/\mu\text{s}$ |
| THD+N | Total Harmonic Distortion and Noise | $f=1\text{kHz}$, $A_v=1$, $R_L=100\text{k}\Omega$, $V_{\text{OUT}} = 2V_{\text{PP}}$ $f=10\text{kHz}$, $A_v=1$, $R_L=100\text{k}\Omega$, $V_{\text{OUT}} = 2V_{\text{PP}}$ | | -105 | -90 | dB |

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300mV beyond the power supply, the input current should be limited to less than 10mA.

A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

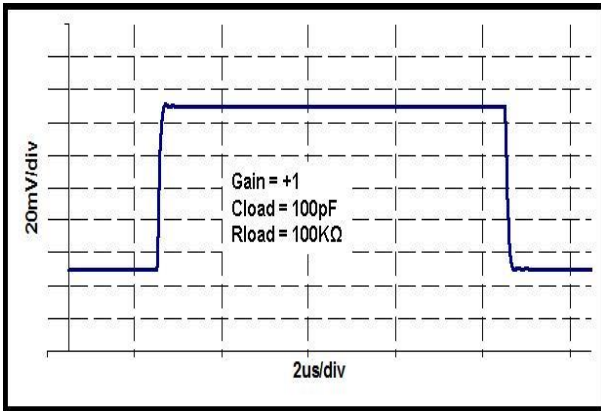
Full power bandwidth is calculated from the slew rate $\text{FPBW} = \text{SR}/\pi \cdot V_{\text{P-P}}$.

TP321/TP358/TP324

General Purpose, 1MHz, Micro-Power CMOS Op-Amps

Typical Performance Characteristics

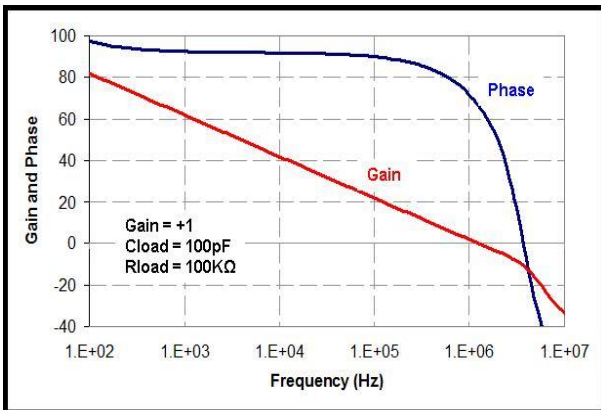
Small-Signal Step Response, 100mV Step



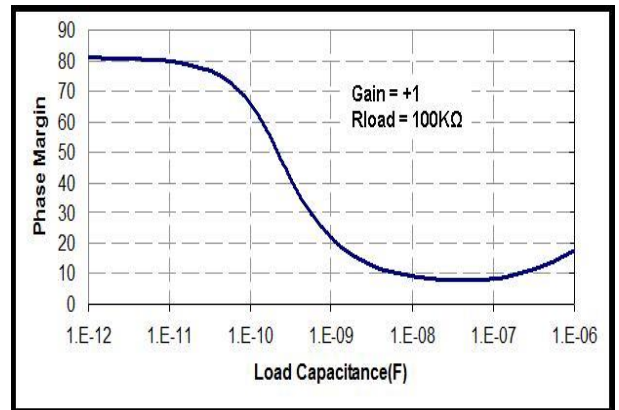
Large-Signal Step Response, 2V Step



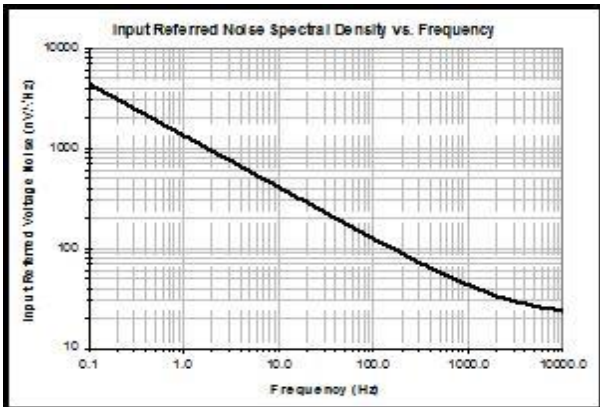
Open-Loop Gain and Phase



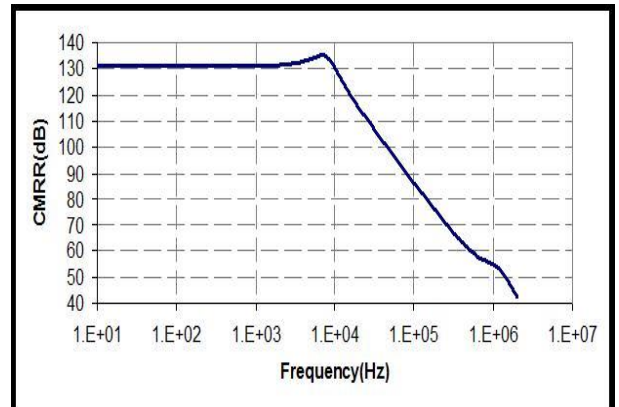
Phase Margin vs. C_{LOAD} (Stable for Any C_{LOAD})



Input Voltage Noise Spectral Density

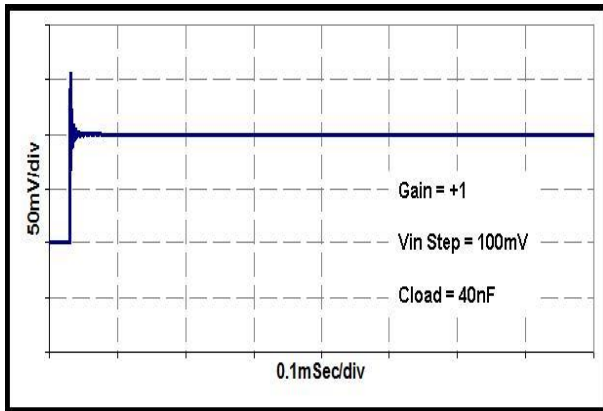


Common-Mode Rejection Ratio

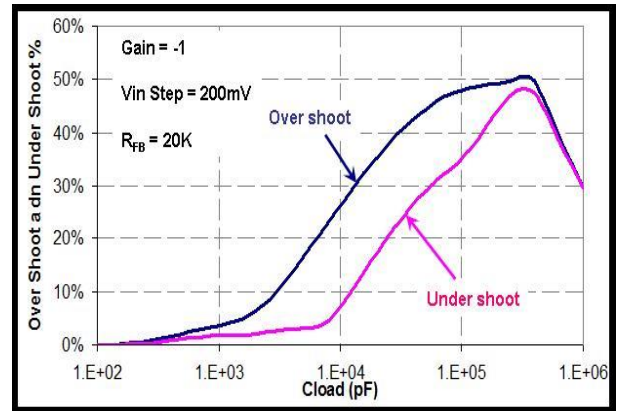


Typical Performance Characteristics

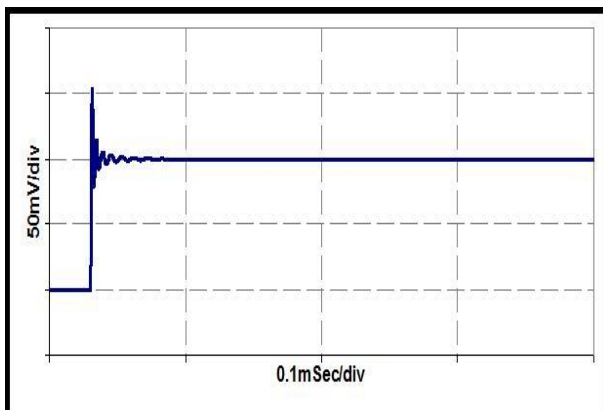
Over-Shoot Voltage, $C_{LOAD} = 40nF$, Gain = +1



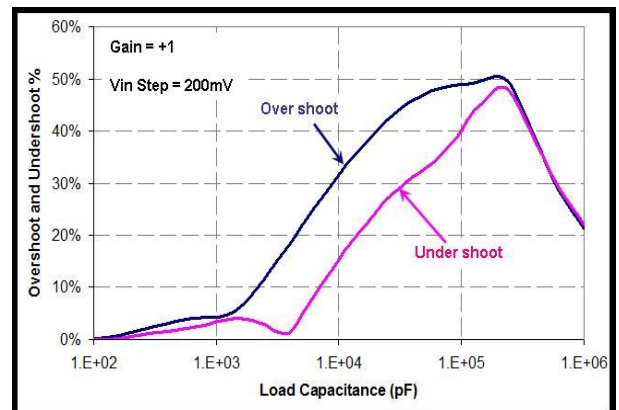
Over-Shoot % vs. C_{LOAD} , Gain = -1, $R_{FB} = 20k\Omega$



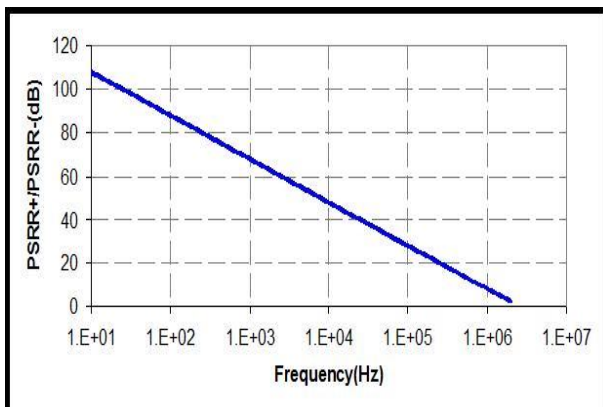
Over-Shoot Voltage, $C_{LOAD} = 40nF$, Gain = -1, $R_{FB} = 100k\Omega$



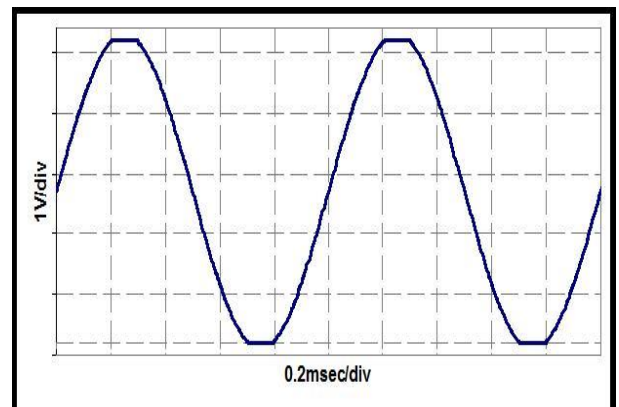
Small-Signal Over-Shoot % vs. C_{LOAD} , Gain = +1



Power-Supply Rejection Ratio



$V_{IN} = -0.2V$ to $5.7V$, No Phase Reversal

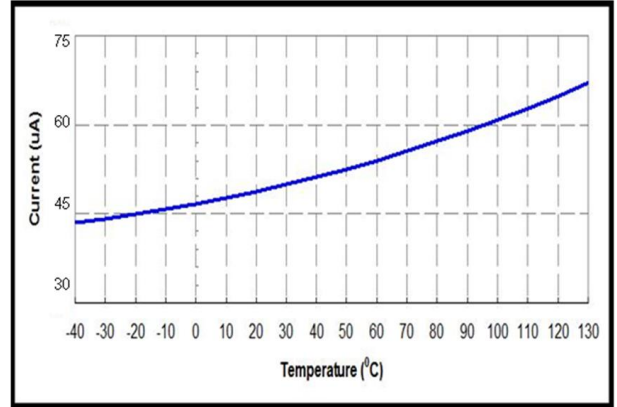


Typical Performance Characteristics

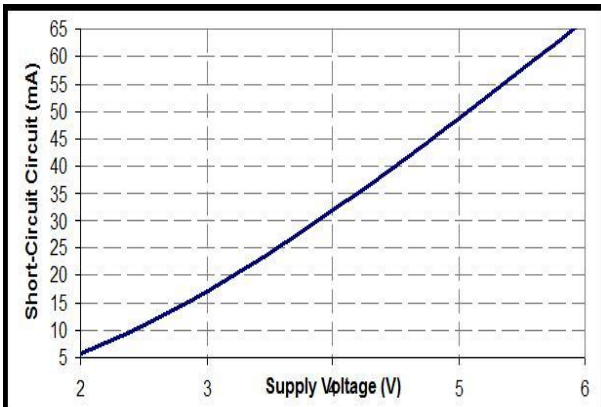
Quiescent Supply Current vs. Supply Voltage



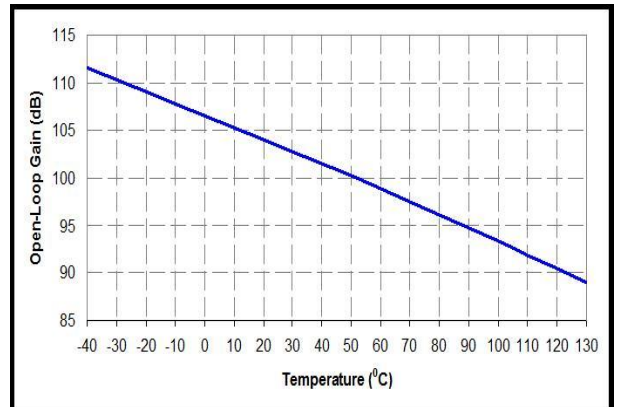
Quiescent Supply Current vs. Temperature



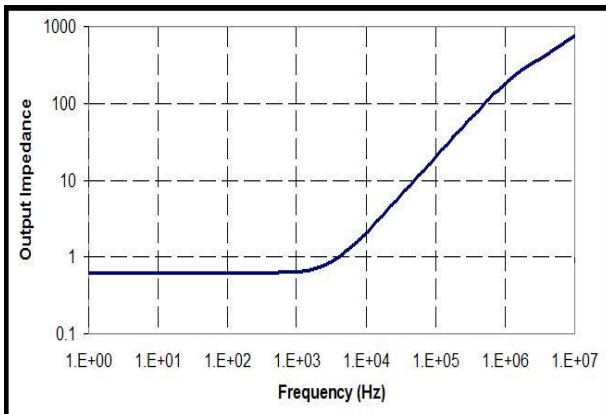
Short-Circuit Current vs. Supply Voltage



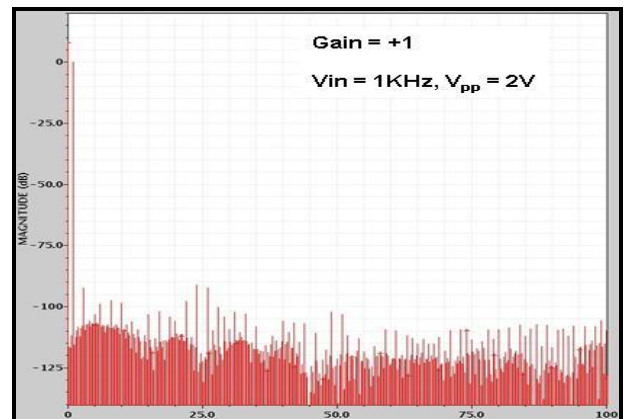
Open-Loop Gain vs. Temperature



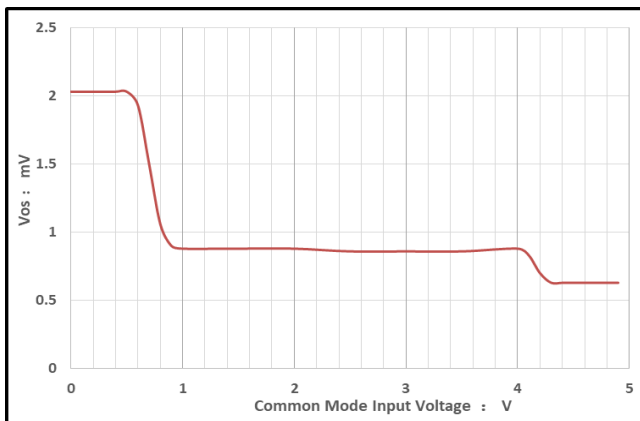
Closed-Loop Output Impedance vs. Frequency



THD+Noise, Gain = +1, V_{IN} = 1kHz, V_{pp} = 2V



Vos vs. Common Mode Input Voltage



TP321/TP358/TP324

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Pin Functions

-IN: Inverting Input of the Amplifier. Voltage range of this pin can go from $V^- - 0.1V$ to $V^+ + 0.1V$.

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as -IN.

+Vs: Positive Power Supply. Typically the voltage is from 2.1V to 5.25V. Split supplies are possible as long as the voltage between V^+ and V^- is between 2.1V and 5.25V. A bypass capacitor of 0.1 μ F as close to the part as possible should be used

between power supply pins or between supply pins and ground.

-Vs: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 2.1V to 5.25V. If it is not connected to ground, bypass it with a capacitor of 0.1 μ F as close to the part as possible.

OUT: Amplifier Output. The voltage range extends to within millivolts of each supply rail.

Operation

The TP321/358/324 input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is comprised of two CMOS differential amplifiers, a PMOS stage and NMOS stage that are active over different ranges of common mode input voltage. The

Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

Low Supply Voltage and Low Power Consumption

The TP321/358/324 of operational amplifiers can operate with power supply voltages from 2.1V to 6.0V. Each amplifier draws only 45 μ A typical quiescent current. The low supply voltage capability and low supply current are ideal for portable applications demanding high capacitive load driving capability and wide bandwidth. The TP321/358/324 is optimized for wide bandwidth low power applications. They have an industry leading high GBWP to power ratio and are unity gain stable. When the load capacitance increases, the increased capacitance at the output pushed the non-dominant pole to lower frequency in the open loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence better phase margin.

Low Input Referred Noise

The TP321/358/324 provides a low input referred noise density of 45nV/ $\sqrt{\text{Hz}}$ at 1kHz. The voltage noise will grow slowly with the frequency in wideband range.

Positive Input Offset Voltage

The TP321/358/324 has a low offset voltage of 5.0mV maximum which is essential for precision applications.

Low Input Bias Current

The TP321/358/324 is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on "PCB Surface Leakage" for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of

current to flow, which is similar to the TP321/358/324 OPA's input bias current at +27°C ($\pm 10\text{pA}$, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

- Connect the non-inverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.
- Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

- Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the op-amp (e.g., $V_{DD}/2$ or ground).
- Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.

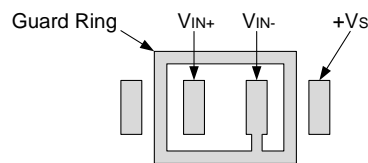


Figure 1

Ground Sensing and Rail to Rail Output

The TP321/358/324 has excellent output drive capability, delivering over 10mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 10mV of either rail. Since the inputs can go 100mV beyond either rail, the op-amp can easily perform 'True Ground Sensing'.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.3V beyond either supply, otherwise current will flow through these diodes.

ESD

The TP321/358/324 has reverse-biased ESD protection diodes on all inputs and output. Input and output pins cannot be biased more than 100mV beyond either supply rail.

Feedback Components and Suppression of Ringing

Care should be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example, in a gain of +2 configuration with gain and feedback resistors of 10k, a poorly designed circuit board layout with parasitic capacitance of 5pF (part +PC board) at the amplifier's inverting input will cause the amplifier to ring due to a pole formed at 3.2MHz. An additional capacitor of 5pF across the feedback resistor as shown in Figure 2 will eliminate any ringing.

Careful layout is extremely important because low power signal conditioning applications demand high-impedance circuits. The layout should also minimize stray capacitance at the OPA's inputs. However some stray capacitance may be unavoidable and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor. Select the smallest capacitor value that ensures stability.

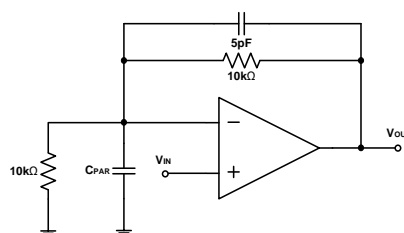


Figure 2

Driving Large Capacitive Load

The TP321/358/324 of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for “Phase Margin vs. Load Capacitance”. As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop’s phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer ($G = +1V/V$) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP321/358/324 (e.g., $> 200\text{ pF}$ when $G = +1V/V$), a small series resistor at the output (R_{ISO} in Figure 3) improves the feedback loop’s phase margin and stability by making the output load resistive at higher frequencies.

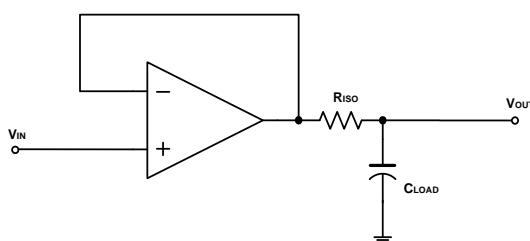


Figure 3

Power Supply Layout and Bypass

The TP321/358/324 OPA’s power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., $0.01\mu\text{F}$ to $0.1\mu\text{F}$) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., $1\mu\text{F}$ or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA’s inputs and outputs. To decrease stray capacitance, minimize PCB board lengths and resistor leads, and place external components as close to the op amps’ pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

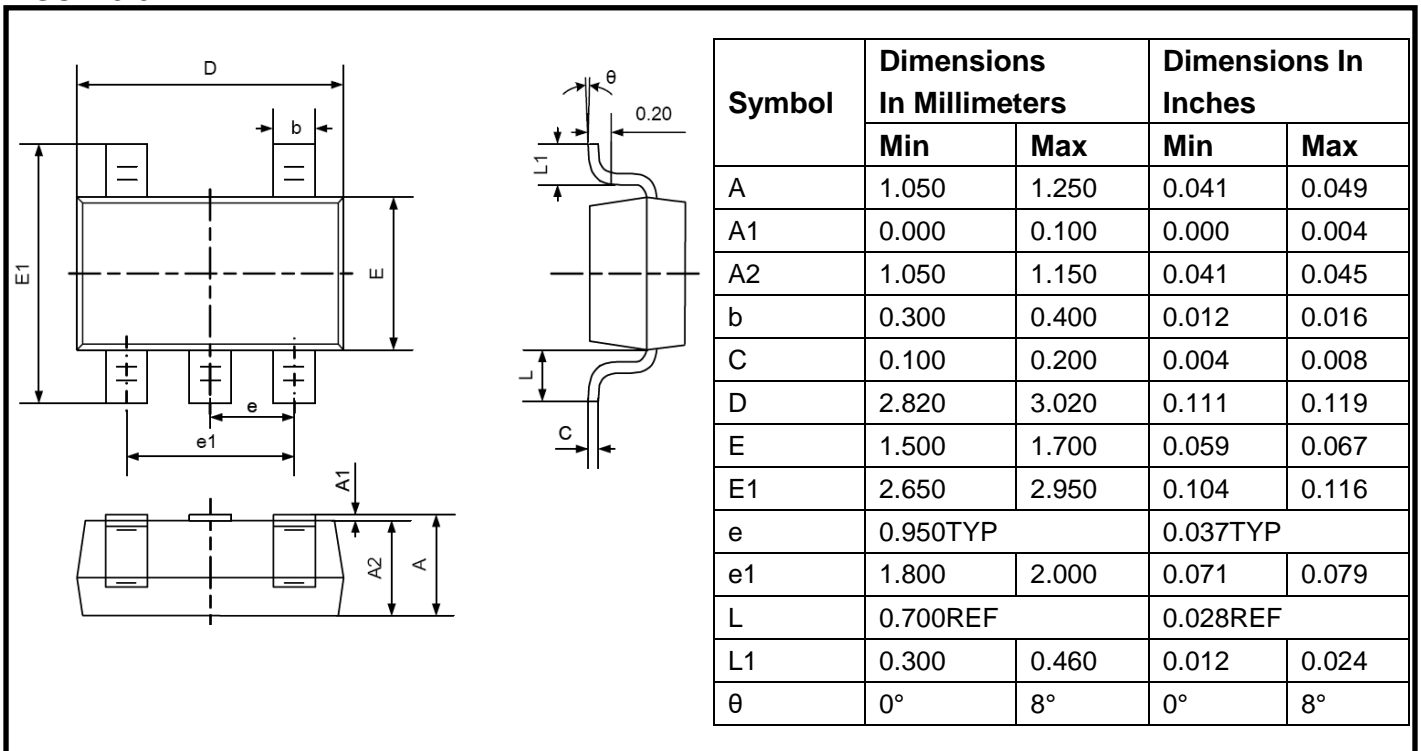
Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

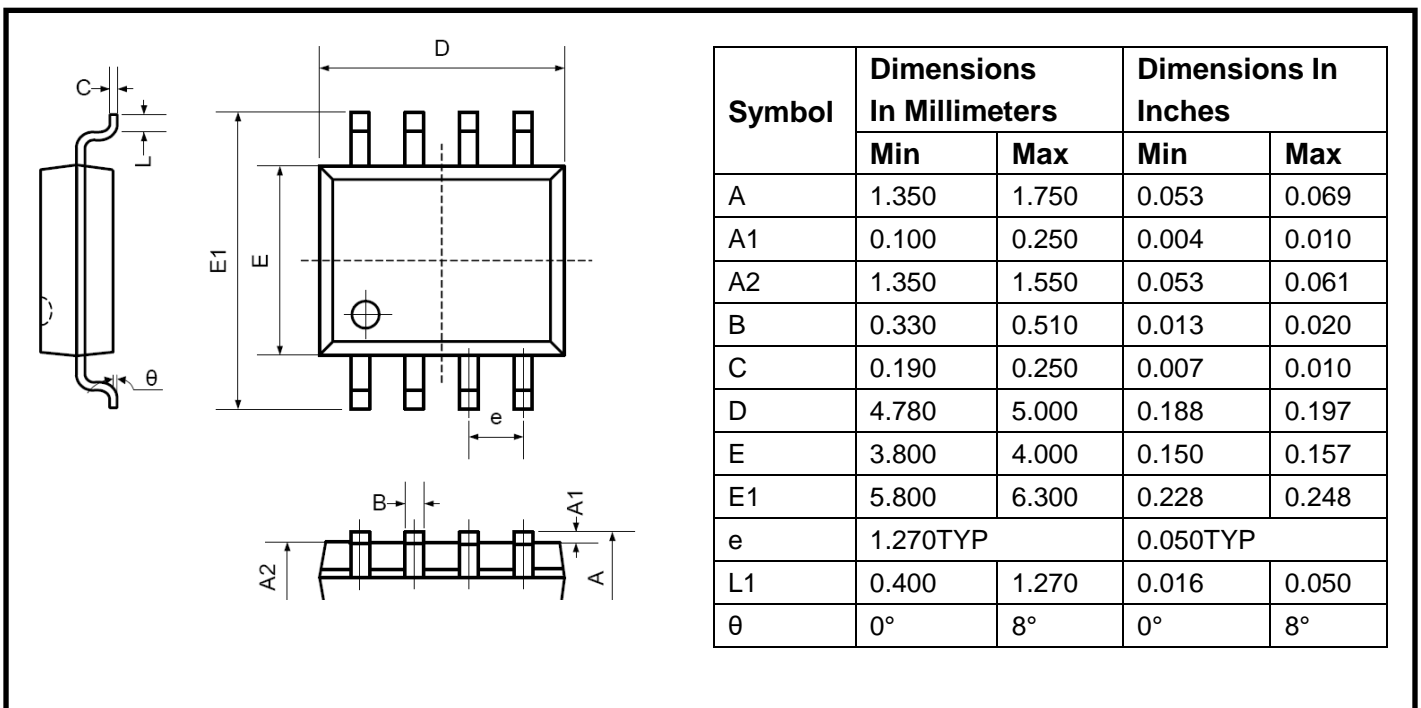
The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Package Outline Dimensions

SOT23-5



SOIC-8

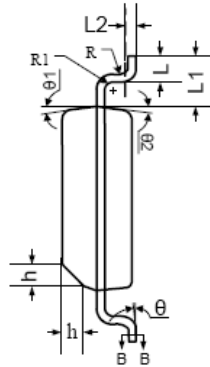
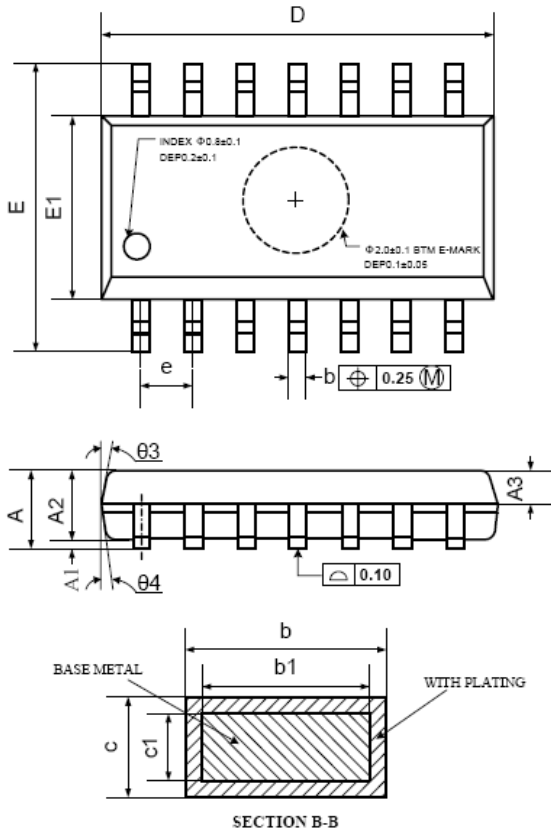


TP321/TP358/TP324

General Purpose, 1MHz, Micro-Power CMOS Op-Amps

Package Outline Dimensions

SOIC-14



| Symbol | Dimensions In Millimeters | | |
|------------|------------------------------|------|------|
| | MIN | NOM | MAX |
| A | 1.35 | 1.60 | 1.75 |
| A1 | 0.10 | 0.15 | 0.25 |
| A2 | 1.25 | 1.45 | 1.65 |
| A3 | 0.55 | 0.65 | 0.75 |
| b | 0.36 | | 0.49 |
| b1 | 0.35 | 0.40 | 0.45 |
| c | 0.16 | | 0.25 |
| c1 | 0.15 | 0.20 | 0.25 |
| D | 8.53 | 8.63 | 8.73 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27 BSC | | |
| L | 0.45 | 0.60 | 0.80 |
| L1 | 1.04 REF | | |
| L2 | 0.25 BSC | | |
| R | 0.07 | | |
| R1 | 0.07 | | |
| h | 0.30 | 0.40 | 0.50 |
| θ | 0° | | 8° |
| $\theta 1$ | 6° | 8° | 10° |
| $\theta 2$ | 6° | 8° | 10° |
| $\theta 3$ | 5° | 7° | 9° |
| $\theta 4$ | 5° | 7° | 9° |

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