

### Features

- Input Voltage Range: 2.2 V to 6.5 V
- Output Voltage Options:
  - Fixed Output: 1.2 V, 1.8 V, 3.3 V and 5 V
  - Adjustable Output: 0.8 V to 6 V
- $\pm 3\%$  Accuracy over Line Regulation, Load Regulation, and Operating Temperature Range
- 1 A Maximum Output Current
- Low Dropout Voltage: 500 mV Maximum at 1 A
- High PSRR:
  - 80 dB at 1 kHz
  - 50 dB at 1 MHz
- 4.5  $\mu\text{V}_{\text{RMS}}$  Output Voltage Noise (100 Hz to 100 kHz)
- Excellent Transient Response
- Stable with a 4.7  $\mu\text{F}$  or Larger Ceramic Output Capacitor
- Over-Current Protection and Over-Temperature Protection
- Package: 3x3 DFN-8

### Description

The TPL910A series are 1-A high-current, 4.5- $\mu\text{V}_{\text{RMS}}$  low-noise, high-PSRR, high-accuracy linear regulators with only 500-mV maximum ultra-low dropout voltage at 1-A load current. The TPL910A series support both fixed output voltage ranges from 1.2 V to 5 V and adjustable output voltage ranges from 0.8 V to 6 V with external resistor divider.

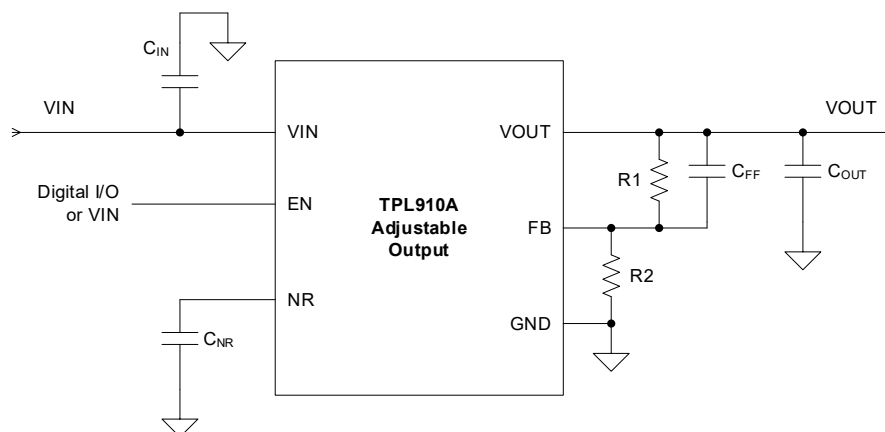
Ultra-low noise, high PSRR, and high output current capability makes the TPL910A series as the ideal power supply for noise-sensitive applications, such as high-speed communication facilities, and high-definition imaging equipment. Accurate output voltage tolerance, excellent transient response, and adjustable soft-start control ensures the TPL910A series products optimal power supply for the large-scale processors or digital loads, such as such as ASIC, FPGA, CPLD and DSP.

The TPL910A series provide small 3x3 DFN-8 package with guaranteed operating temperature ranges from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Applications

- Communication: CPU, ASIC, FPGA, CPLD, DSP
- High-Performance Analog: ADC, DAC, LVDS, VCO
- Noise-Sensitive Imaging: CMOS Sensors, Video ASICs

### Typical Application Circuit



**1-A Output, High-PSRR, Low-Noise Low-Dropout  
Linear Regulator****Product Family Table**

Part Number	Order Number	Output Voltage (V)	Package
TPL910A	TPL910ADJA-DF6R	Adjustable	3×3 DFN-8

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**Revision History**

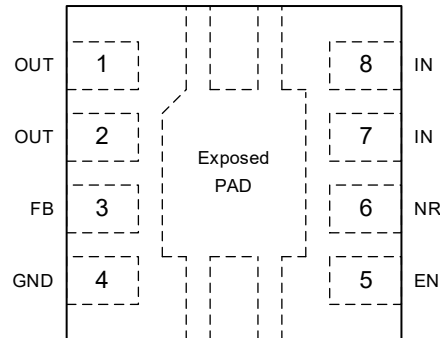
Date	Revision	Notes
2020-12-31	Rev.Pre.0	Preliminary Version
2021-08-31	Rev.A.0	Initial Release

## Pin Configuration and Functions

### TPL910A Series

DFN-8 Package

Top View



## Pin Functions

Pin		I/O	Description
No.	Name		
5	EN	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly. The EN pin must not be left floating.
3	FB	I	Output voltage feedback pin. Connect to an external resistor divider to adjust the output voltage. A 10-nF feed-forward capacitor from FB to OUT (as close as possible to FB pin) is recommended to maximize regulator ac performance.
4	GND	–	Ground reference pin. Connect GND pin to PCB ground plane directly.
7, 8	IN	I	Input voltage pin. Suggest connecting a 10- $\mu$ F or larger ceramic capacitor from IN to ground (as close as possible to IN pin) to reduce the jitter from previous-stage power supply.
6	NR/SS	I	Noise-reduction and soft-start pin. A 10-nF or larger capacitor from NR/SS to GND (as close as possible to NR/SS pin) is recommended to maximize ac performance.
1, 2	OUT	O	Regulated output voltage pin. A 4.7- $\mu$ F or larger ceramic capacitor from OUT to ground (as close as possible to OUT pin) is required to ensure regulator stability.
–	Exposed Pad	–	Exposed PAD must be connected to a large-area ground plane to maximum the thermal performance.

## Specifications

### Absolute Maximum Ratings

Parameter		Min	Max	Unit
IN, EN		-0.3	7	V
OUT		-0.3	$V_{IN} + 0.3$	V
FB, NR		-0.3	3.6	V
T <sub>J</sub>	Junction Temperature Range	-40	150	°C
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C
T <sub>L</sub>	Lead Temperature (Soldering 10 sec)		260	°C

- (1) Stresses beyond the Absolute Maximum Ratings may permanently damage the device.  
 (2) All voltage values are with respect to GND.

### ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
IN	Input voltage	2.2		6.5	V
EN	Enable voltage	0		6.5	V
OUT	Output voltage	0.8		6	V
OUT	Output current	0		1	A
C <sub>OUT</sub>	Output capacitor	4.7			μF
C <sub>FF</sub>	Feed-forward capacitor		10		nF
C <sub>NR</sub>	NR capacitor		10		nF
T <sub>J</sub>	Junction Temperature Range	-40		125	°C

### Thermal Information

Package Type	θ <sub>JA</sub>	θ <sub>JC</sub>	Unit
3×3 DFN-8	69.3	8.16	°C/W

## 1-A Output, High-PSRR, Low-Noise Low-Dropout Linear Regulator

### Electrical Characteristics

All test conditions:  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (typical value at  $T_J = +25^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $2.2\text{ V}$ , whichever is greater;  $V_{EN} = 2.2\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 4.7\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $C_{NR} = 10\text{ nF}$ ,  $C_{FF} = \text{open}$ , unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit	
<b>Supply Input Voltage and Current</b>						
$V_{IN}$	Supply voltage range <sup>(1)</sup>	2.2		6.5	V	
UVLO	Input supply UVLO	$V_{IN}$ rising, $R_L = 1\text{ k}\Omega$		2.1	V	
	Hysteresis		70		mV	
$I_{GND}$	GND pin current	$V_{IN} = 6.5\text{ V}$ , $I_{OUT} = 1\text{ mA}$		130	$\mu\text{A}$	
		$V_{IN} = 6.5\text{ V}$ , $I_{OUT} = 1\text{ A}$		5.4	8	mA
$I_{SD}$	Shutdown current	$V_{IN} = 6.5\text{ V}$ , $V_{EN} = 0\text{ V}$		2.2	$\mu\text{A}$	
<b>Device Enable</b>						
$V_{IH(EN)}$	EN high-level input voltage	Device enable	1.2		6.5	V
$V_{IL(EN)}$	EN low-level input voltage	Device disable	0		0.4	V
$I_{EN}$	EN leakage current	$V_{IN} = 6.5\text{ V}$ , $V_{EN} = 0\text{ V}$ to $6.5\text{ V}$		0.1	1	$\mu\text{A}$
<b>Regulated Output Voltage and Current</b>						
$V_{FB}$	Feedback voltage <sup>(2)</sup>		0.8		V	
$I_{FB}$	FB pin leakage current <sup>(2)</sup>	$V_{IN} = 6.5\text{ V}$ , stress $V_{FB} = 0.8\text{ V}$		0.1	1	$\mu\text{A}$
$V_{NR/SS}$	NR/SS pin voltage		0.8		V	
$I_{NR/SS}$	NR/SS pin charging current	$V_{IN} = 6.5\text{ V}$ , $V_{NR} = \text{GND}$		6.2	9	$\mu\text{A}$
$V_{OUT}$	Output accuracy <sup>(3)</sup>	$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $2.2\text{ V}$ to $6.5\text{ V}$ , $V_{OUT} = 0.8\text{ V}$ to $6\text{ V}$ , $I_{OUT} = 100\text{ mA}$ to $500\text{ mA}$	-2%		2%	
		$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $2.2\text{ V}$ to $6.5\text{ V}$ , $V_{OUT} = 0.8\text{ V}$ to $6\text{ V}$ , $I_{OUT} = 100\text{ mA}$ to $1\text{ A}$	-3%		3%	
$\Delta V_{OUT}$	Line regulation	$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $2.2\text{ V}$ to $6.5\text{ V}$ , $I_{OUT} = 100\text{ mA}$		0.03		mV/V
	Load regulation	$I_{OUT} = 100\text{ mA}$ to $1\text{ A}$		2		mV/A

(1) Minimum  $V_{IN} = V_{OUT(NOM)} + V_{DO}$  or  $2.2\text{ V}$ , whichever is greater.

(2) For adjustable output voltage version only.

(3) Resistor tolerance is not included. Output accuracy is not tested at this condition:  $V_{OUT} = 0.8\text{ V}$ ,  $4.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ , and  $750\text{ mA} \leq I_{OUT} \leq 1\text{ A}$ , because the power dissipation is out of package limitation.

**1-A Output, High-PSRR, Low-Noise Low-Dropout Linear Regulator**
**Electrical Characteristics (continued)**

All test conditions:  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (typical value at  $T_J = +25^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $2.2\text{ V}$ , whichever is greater;  $V_{EN} = 2.2\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 4.7\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $C_{NR} = 10\text{ nF}$ ,  $C_{FF} = \text{open}$ , unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit		
<b>Regulated Output Voltage and Current</b>							
$V_{DO}$	Dropout voltage <sup>(4)</sup>	$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $2.2\text{ V}$ to $6.5\text{ V}$ , $I_{OUT} = 500\text{ mA}$ , $V_{FB} = \text{GND}$ or $V_{SNS} = \text{GND}$			250	mV	
		$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $2.2\text{ V}$ to $6.5\text{ V}$ , $I_{OUT} = 750\text{ mA}$ , $V_{FB} = \text{GND}$ or $V_{SNS} = \text{GND}$			350	mV	
		$V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or $2.2\text{ V}$ to $6.5\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $V_{FB} = \text{GND}$ or $V_{SNS} = \text{GND}$			500	mV	
$I_{LIM}$	Output current limit	$V_{OUT}$ is forced at $0.9 \times V_{OUT(NOM)}$ , $V_{IN} \geq 3.3\text{ V}$	1.1	1.6		A	
$I_{SC}$	Short circuit to ground current limit	$V_{OUT}$ is forced to ground, $T_A = 25^{\circ}\text{C}$		0.6		A	
$t_{STR}$	Start-up time	$V_{OUT(NOM)} = 3.3\text{ V}$ , $V_{OUT} = 0\%$ to $90\% V_{OUT(NOM)}$ , $R_L = 3.3\text{ k}\Omega$ , $C_{OUT} = 10\text{ }\mu\text{F}$ , $C_{NR} = 470\text{ nF}$		80		ms	
<b>PSRR and Noise</b>							
$PSRR$	Power supply ripple rejection	$V_{IN} = 4.3\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $C_{OUT} = 4.7\text{ }\mu\text{F}$ , $C_{NR} = 470\text{ nF}$ , $C_{FF} = 470\text{ nF}$	$f = 1\text{ kHz}$		80		dB
			$f = 10\text{ kHz}$		65		dB
			$f = 100\text{ kHz}$		54		dB
			$f = 1\text{ MHz}$		45		dB
$V_N$	Output noise voltage	$BW = 100\text{ Hz}$ to $100\text{ kHz}$ , $V_{IN} = 3.8\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $C_{OUT} = 4.7\text{ }\mu\text{F}$ , $C_{NR} = 470\text{ nF}$ , $C_{FF} = 470\text{ nF}$		4.5		$\mu\text{V}_{RMS}$	
<b>Temperature Range</b>							
$T_{SD}$	Thermal shutdown threshold	Temperature increasing		165		$^{\circ}\text{C}$	
	Hysteresis			20		$^{\circ}\text{C}$	

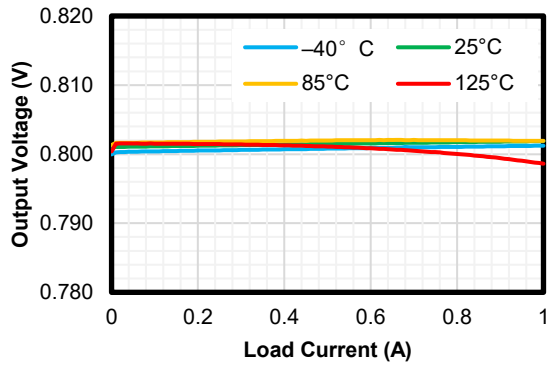
(4) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current and measure for  $V_{OUT(NOM)} \geq 2.2\text{ V}$ . In dropout mode, the output voltage will be equal to:  $V_{IN} - V_{DO}$ .



## 1-A Output, High-PSRR, Low-Noise Low-Dropout Linear Regulator

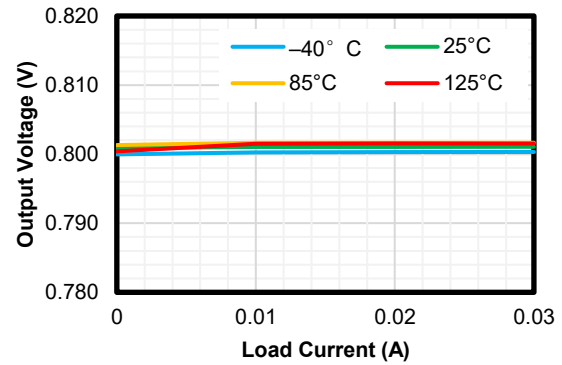
### Typical Performance Characteristics

All test conditions:  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (typical value at  $T_J = +25^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $2.2\text{ V}$ , whichever is greater;  $V_{EN} = 2.2\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 4.7\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $C_{NR} = 10\text{ nF}$ ,  $C_{FF} = \text{open}$ , unless otherwise noted.



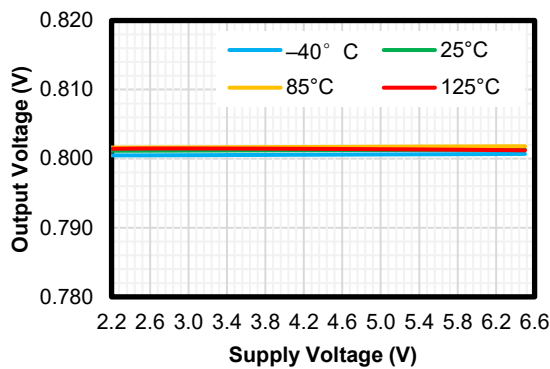
$V_{OUT} = 0.8\text{ V}$

Figure 1 Load Regulation



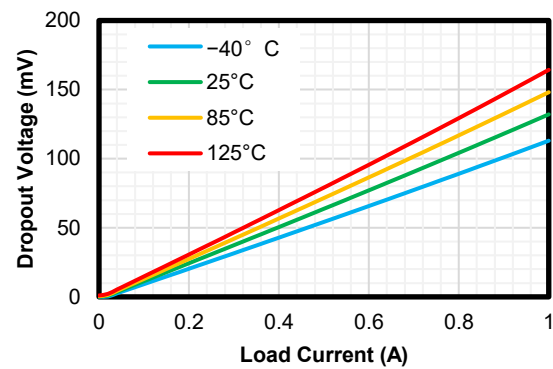
$V_{OUT} = 0.8\text{ V}$

Figure 2 Load Regulation at Light Load



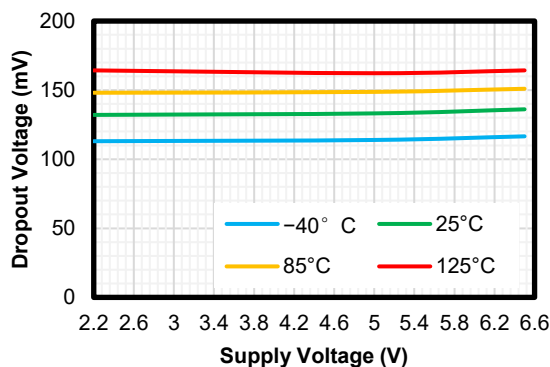
$V_{OUT} = 0.8\text{ V}$ ,  $I_{OUT} = 5\text{ mA}$

Figure 3 Line Regulation



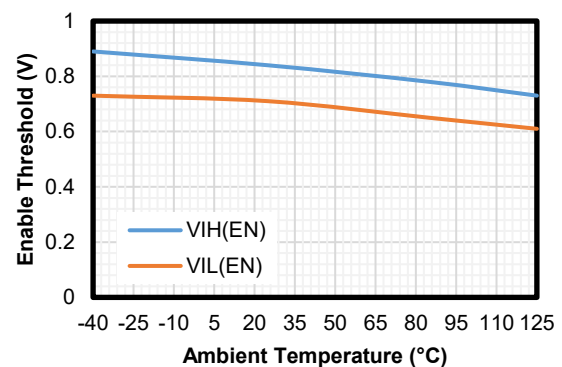
$V_{IN} = 2.2\text{ V}$

Figure 4 Dropout Voltage vs. Load Current



$I_{OUT} = 1\text{ A}$

Figure 5 Dropout Voltage vs. Supply Voltage



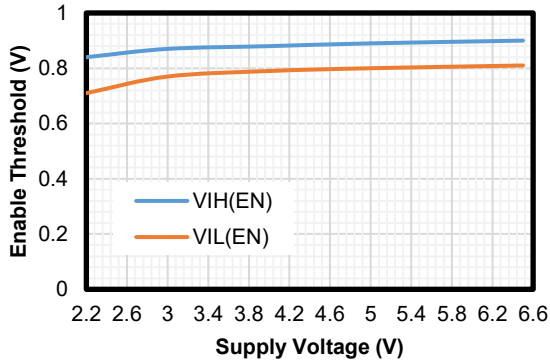
$V_{IN} = 2.2\text{ V}$

Figure 6 Enable Threshold vs. Temperature

## 1-A Output, High-PSRR, Low-Noise Low-Dropout Linear Regulator

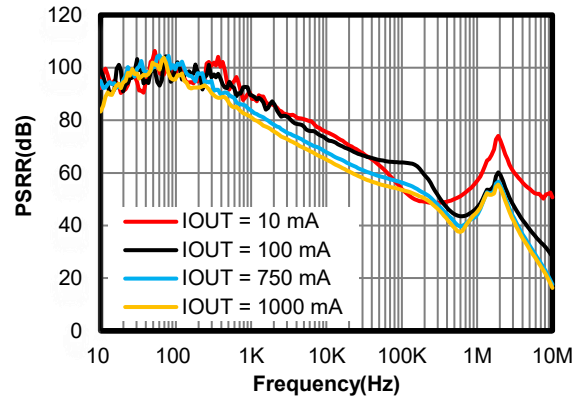
### Typical Performance Characteristics (Continued)

All test conditions:  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (typical value at  $T_J = +25^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$  or  $2.2\text{ V}$ , whichever is greater;  $V_{EN} = 2.2\text{ V}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{IN} = 4.7\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $C_{NR} = 10\text{ nF}$ ,  $C_{FF} = \text{open}$ , unless otherwise noted.



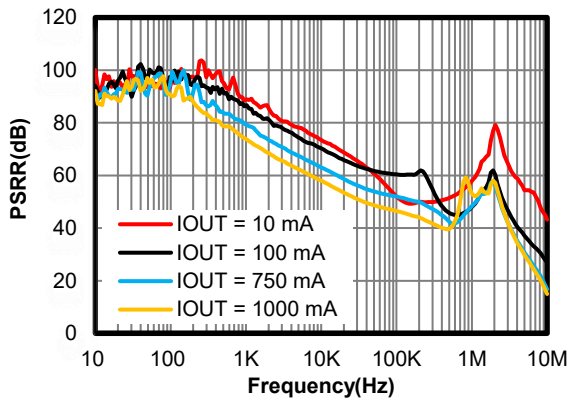
$T_A = 25^{\circ}\text{C}$

Figure 7 Enable Threshold vs. Supply Voltage



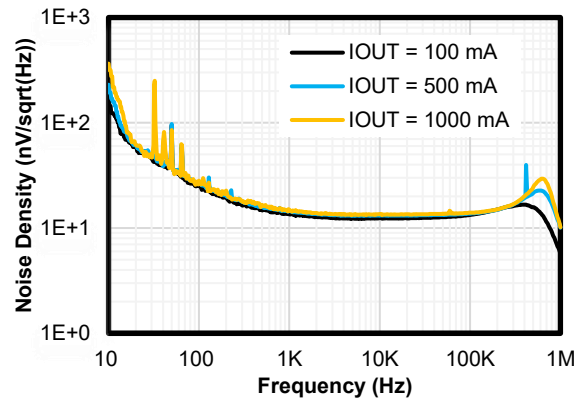
$V_{IN} = 4.3\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{NR/SS} = 470\text{ nF}$ ,  $C_{FF} = 470\text{ nF}$

Figure 8 PSRR



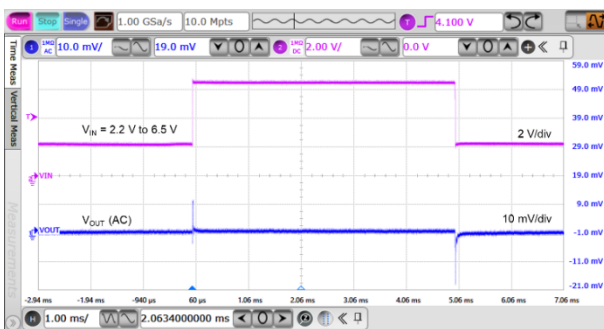
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $C_{NR/SS} = 470\text{ nF}$ ,  $C_{FF} = 470\text{ nF}$

Figure 9 PSRR



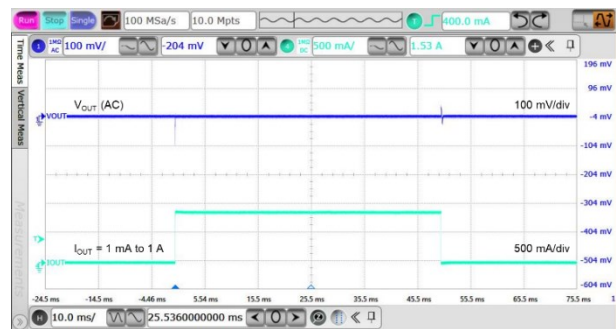
$V_{IN} = 3.8\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ ,  $C_{NR/SS} = 470\text{ nF}$ ,  $C_{FF} = 470\text{ nF}$

Figure 10 Noise



$V_{IN} = 2.2\text{ V}$  to  $6.5\text{ V}$ ,  $V_{OUT} = 0.8\text{ V}$

Figure 11 Line Transient



$I_{OUT} = 1\text{ mA}$  to  $1\text{ A}$ ,  $V_{OUT} = 0.8\text{ V}$

Figure 12 Load Transient

### Detailed Description

#### Overview

The TPL910A series are 1-A high-current, 4.5- $\mu\text{V}_{\text{RMS}}$  low-noise, high-PSRR, high-accuracy linear regulators with only 500-mV maximum ultra-low dropout voltage at 1-A load current. The TPL910A series support both fixed output voltage ranges from 1.2 V to 5 V and adjustable output voltage ranges from 0.8 V to 6 V with external resistor divider.

Ultra-low noise, high PSRR, and high output current capability makes the TPL910A series as the ideal power supply for noise-sensitive applications, such as high-speed communication facilities, and high-definition imaging equipment. Accurate output voltage tolerance, excellent transient response, and adjustable soft-start control ensures the TPL910A series products optimal power supply for the large-scale processors or digital loads, such as such as ASIC, FPGA, CPLD and DSP.

#### Functional Block Diagram

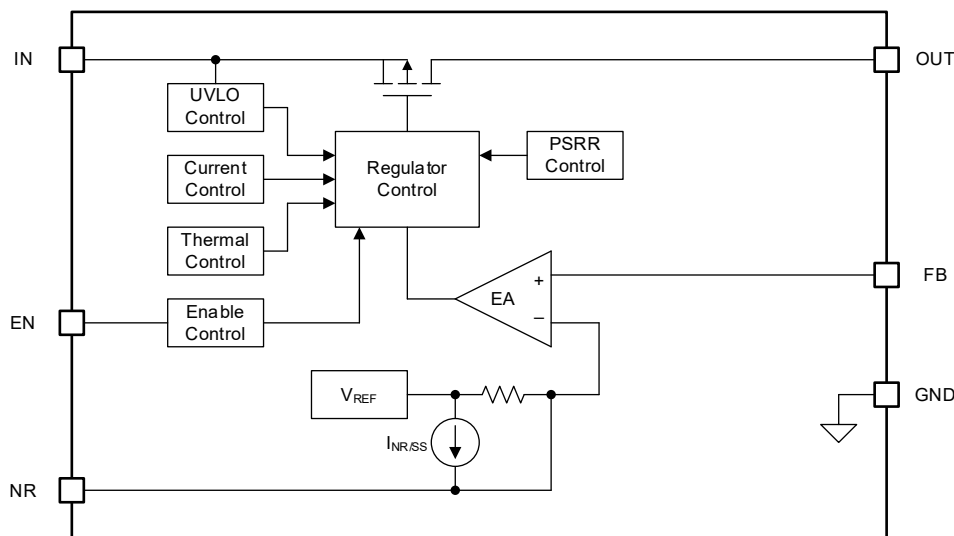


Figure 13 Functional Block Diagram

### Feature Description

#### Enable (EN)

The TPL910A series provide a device enable pin (EN) to enable or disable the device. Connect this pin to the GPIO of an external digital logic control circuit to control the device. When the  $V_{\text{EN}}$  voltage falls below  $V_{\text{IL(EN)}}$ , the LDO device turns off, and when the  $V_{\text{EN}}$  ramps above  $V_{\text{IH(EN)}}$ , the LDO device turns on.

#### Under-Voltage Lockout (IN and UVLO)

The TPL910A series use an under-voltage lockout circuit to keep the output shut off until the internal circuitry operates properly. Refer to the [Electrical Characteristics](#) table for UVLO threshold and hysteresis.

#### Fixed Output Voltage (OUT)

The TPL910A series are available in fixed voltage versions of 1.2 V, 1.8 V, 3.3 V and 5 V. When the input voltage is higher than  $V_{\text{OUT(NOM)}} + V_{\text{DO}}$  or 2.2V, whichever is greater, OUT pin is regulated with fixed voltage. When the input voltage falls below  $V_{\text{OUT(NOM)}} + V_{\text{DO}}$  and greater than UVLO threshold, OUT pin tracks the input voltage, and the output voltage value equals to  $V_{\text{IN}} - V_{\text{DO}}$ .

## 1-A Output, High-PSRR, Low-Noise Low-Dropout Linear Regulator

### Adjustable Output Voltage (OUT and FB)

The TPL910A series are also available in adjustable voltage versions of 0.8 V to 5 V. Using external resistors divider, the output voltage of TPL910A series is determined by the value of the resistor R1 and R2 in [Figure 15](#). Use [Equation 1](#) to calculate the output voltage.

$$V_{OUT} = V_{FB} \times \left( 1 + \frac{R1}{R2} \right) \quad (1)$$

Where the feedback voltage  $V_{FB}$  is 0.8 V.

[Table 1](#) provides a list of recommended resistor combinations to achieve the common output voltage values.

**Table 1 External Resistor Combinations**

Target Output Voltage (V)	External Resistors Divider		Calculated Output Voltage (V)
	R1 (kΩ)	R2 (kΩ)	
0.80	0	10	0.800
0.85	0.62	10	0.850
0.90	1.24	10	0.899
0.95	1.87	10	0.950
1.00	2.49	10	0.999
1.20	4.99	10	1.199
1.50	8.75	10	1.500
1.80	12.5	10	1.800
2.50	21.3	10	2.504
2.80	25	10	2.800
3.00	27.5	10	3.000
3.30	31.3	10	3.304
3.60	35	10	3.600
4.50	46.3	10	4.504
5.00	52.5	10	5.000

### Programmable Soft Start

The TPL910A series integrate a programmable soft-start function to control the output voltage ramp-up slew rate and start-up time. By selecting the external capacitor at the NR/SS pin, the output start-up time can be calculated with [Equation 2](#).

$$t_{Start-up} = 1.25 \times \frac{V_{NR/SS} \times C_{NR/SS}}{I_{NR/SS}} \quad (2)$$

Where, the typical value of  $V_{NR/SS}$  is 0.8 V, the typical value of  $I_{NR/SS}$  is 6.2  $\mu$ A,  $C_{NR/SS}$  is the external capacitor at the NR/SS pin.

## 1-A Output, High-PSRR, Low-Noise Low-Dropout Linear Regulator

### Over-Current Protection

The TPL910A series integrate an internal current limit that helps to protect the regulator during fault conditions.

- When the output voltage is pulled down below the regulated voltage, over-current protection starts to work and limit the output current to  $I_{LIM}$
- When the output voltage is pulled down below the short-to-ground threshold (about 140 mV), or shorted to ground directly, short-to-ground protection starts to work and limit the output current to  $I_{SC}$ .
- During startup, the output current is limited to  $I_{SC}$  before the output voltage ramps higher than the short-to-ground threshold.

Under the over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause the over temperature protection.

### Over-Temperature Protection

The over-temperature protection starts to work when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. Until when the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

The junction temperature range should be limited according to the [Recommended Operating Conditions](#) table, continuously operating above the junction temperature range will reduce the device lifetime.

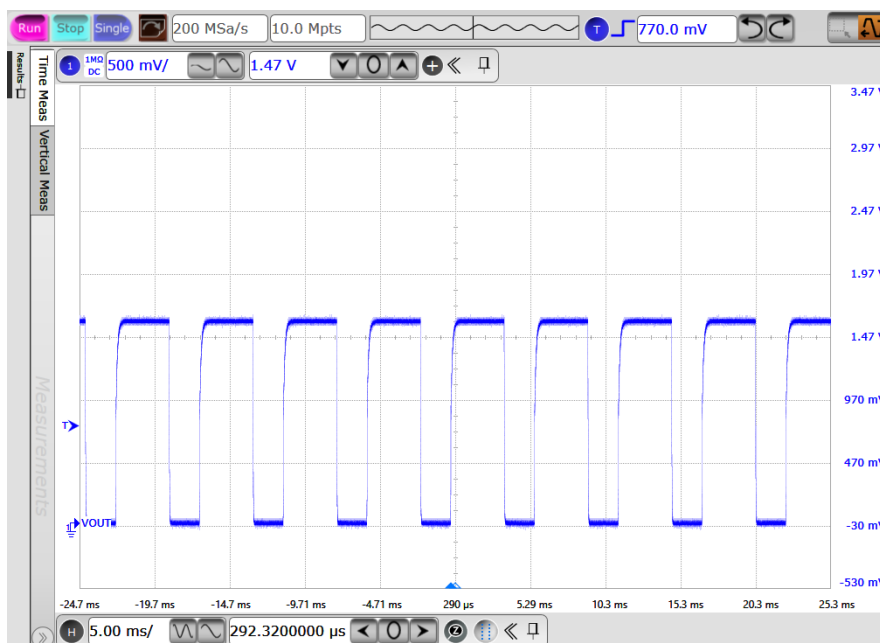


Figure 14 Over-Temperature Protection

### Application and Implementation

#### NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### Application Information

The TPL910A series products are 1-A high-current,  $4.5\text{-}\mu\text{V}_{\text{RMS}}$  low-noise, high-PSRR, high-accuracy linear regulators with only 500-mV maximum ultra-low dropout voltage. The following application schematic shows a typical usage of the TPL910A series.

### Typical Application

Figure 15 shows the typical application schematic of the TPL910A series.

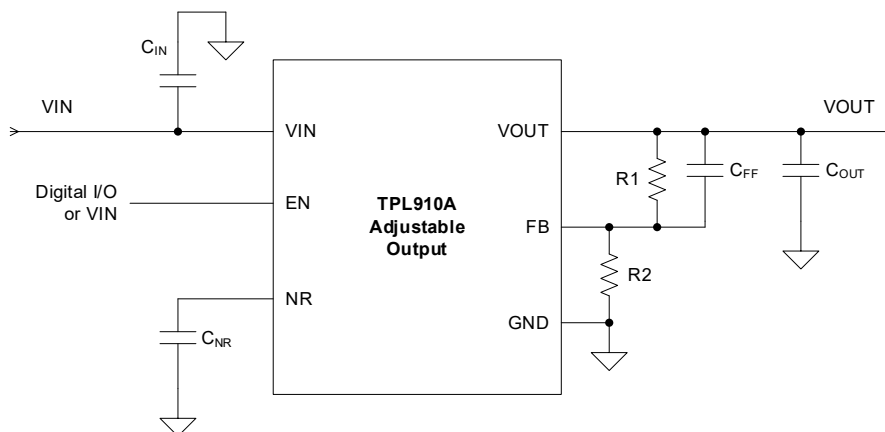


Figure 15 Adjustable Output Operation

### Input Capacitor and Output Capacitor

The TPL910A series is designed to be stable with low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR/SS). It is recommended to use ceramic capacitors with X7R-, X5R-, and COG-rated dielectric materials to get good capacitive stability across temperature.

3PEAK recommends adding a  $10\ \mu\text{F}$  or greater capacitor with a  $0.1\ \mu\text{F}$  bypass capacitor in parallel at IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL910A series requires a minimum  $4.7\ \mu\text{F}$  low ESR output capacitor. 3PEAK recommends selecting a X7R-type  $10\text{-}\mu\text{F}$  ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

### Power Dissipation

During normal operation, LDO junction temperature should meet the requirement in the [Recommended Operating Conditions](#) table. Using below equations to calculate the power dissipation and estimate the junction temperature.

**1-A Output, High-PSRR, Low-Noise Low-Dropout  
Linear Regulator**

The power dissipation can be calculated using [Equation 3](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (3)$$

The junction temperature can be estimated using [Equation 4](#).  $\theta_{JA}$  is the junction-to-ambient thermal resistance.

$$T_J = T_A + P_D \times \theta_{JA} \quad (4)$$

## Layout

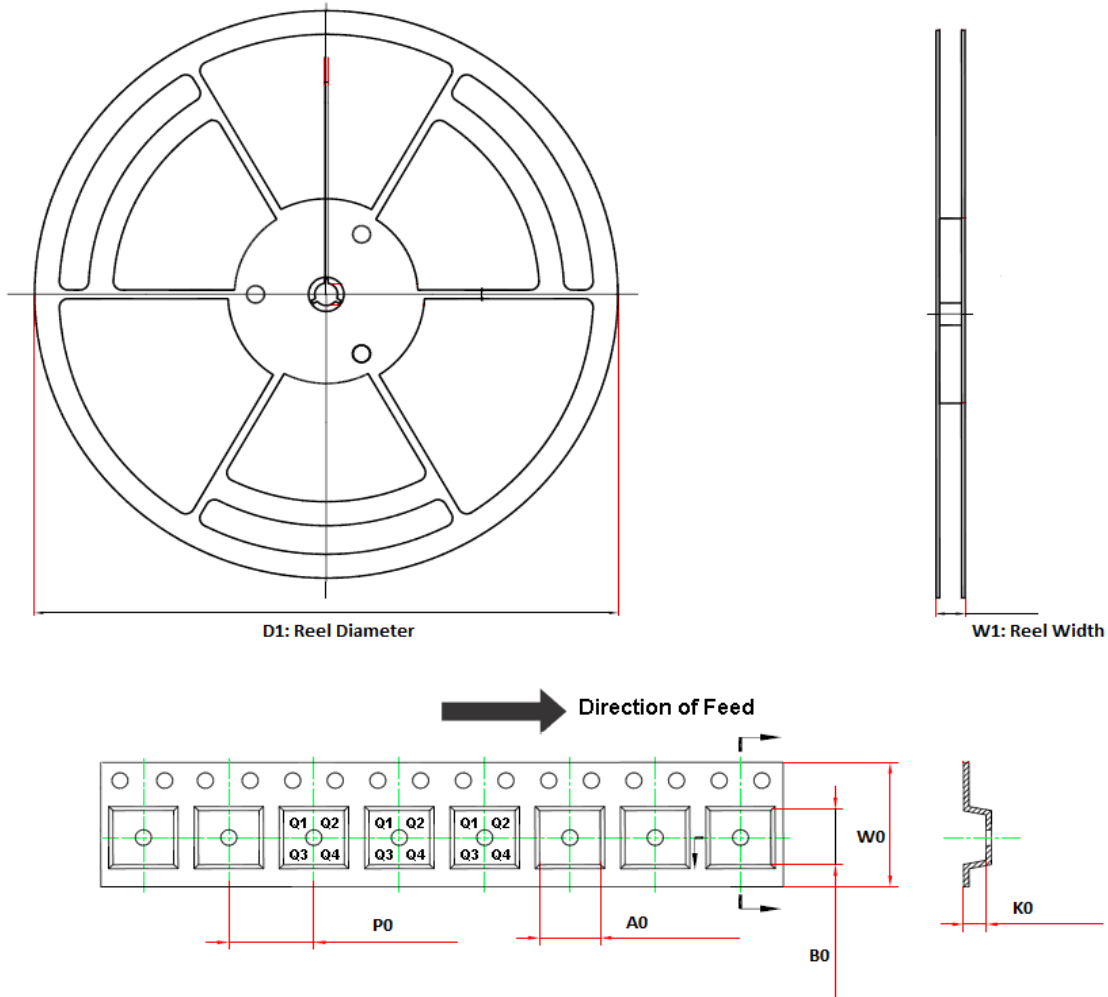
### Layout Guideline

Both input capacitors and output capacitors must be placed as close to the device pins as possible, and vias between capacitors and device power pins must be avoided.

It is recommended to bypass the input pin to ground with a 0.1  $\mu$ F bypass capacitor. The loop area formed by the bypass capacitor connection, IN pin and the GND pin of the system must be as small as possible.

It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.

Tape and Reel Information

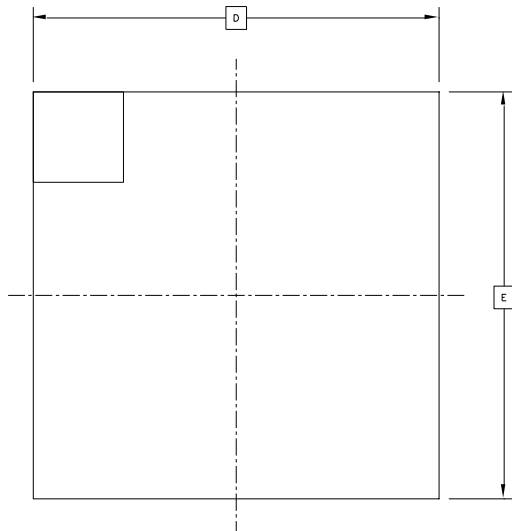


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL910ADJA-DF6R	3x3 DFN-8	330.0	17.6	3.4	3.4	1.1	8.0	12.0	Q2

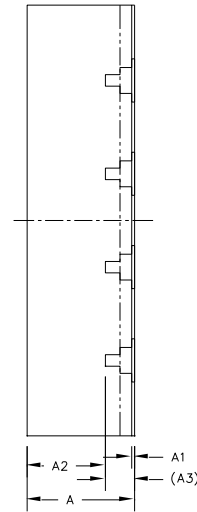


### Package Outline Dimensions

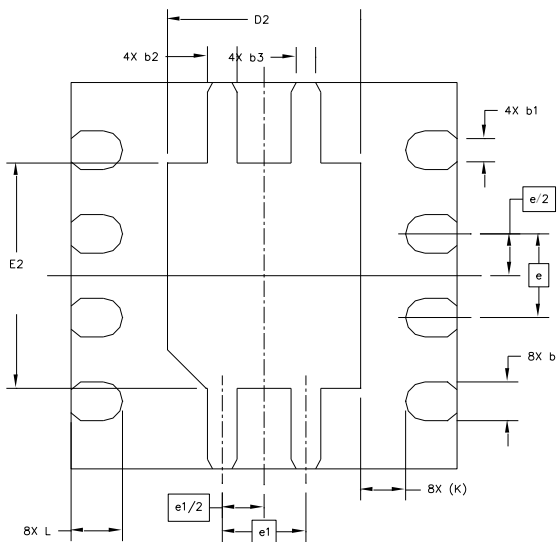
#### 3x3 DFN-8



Top View



Side View



Bottom View

	SYMBOL	MIN	NOM	MAX	
TOTAL THICKNESS	A	0.7	0.75	0.8	
STAND OFF	A1	0	0.02	0.05	
MOLD THICKNESS	A2	---	0.55	---	
L/F THICKNESS	A3	0.203 REF			
LEAD WIDTH	b	0.25	0.3	0.35	
	b1	0.18 REF			
	b2	0.18	0.23	0.28	
	b3	0.15 REF			
BODY SIZE	X	3 BSC			
	Y	3 BSC			
LEAD PITCH	e	0.65 BSC			
	e1	0.65 BSC			
EP SIZE	X	D2	1.4	1.5	1.6
	Y	E2	1.65	1.75	1.85
LEAD LENGTH	L	0.3	0.4	0.5	
LEAD TIP TO EXPOSED PAD EDGE	K	0.35 REF			
PACKAGE EDGE TOLERANCE	ooo	0.1			
LEAD OFFSET	bbb	0.1			
	ddd	0.05			
MOLD FLATNESS	ccc	0.1			
COPLANARITY	eee	0.05			
EXPOSED PAD OFFSET	fff	0.1			

## 1-A Output, High-PSRR, Low-Noise Low-Dropout Linear Regulator

## Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL910ADJA-DF6R	-40°C to +125°C	3×3 DFN-8	L910A	MSL3	Tape and Reel, 4,000	Green

**Green:** 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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