Automotive Fault Protected High-Speed CAN FD Transceiver for Partial Networking

Features

- Meet the ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 Physical Layer Standards
- Supports CAN FD and Data Rating up to 5 Mbps
- Short Propagation Delay Times and Fast Loop Times
- 5-V Power Supply, I/O Voltage Range Supports 2.8-V to 5.5-V MCU Interface
- Support Partial Networking by Means of Selective Wake Up/Wake-Up Frame with INH Output
- SPI for Device Configuration and Status Retrieving
- Ideal Passive Behavior to CAN Bus when Unpowered
- Common-Mode Input Voltage: ±30 V
- Protection Feature:
  - IEC 61000-4-2 ESD Protection up to ±10 kV
  - Bus Fault Protection: ±70 V
  - VCC Undervoltage Protection
  - TXD Dominant Time-Out Function and Bus-Dominant Time-Out Function
  - Thermal Shutdown Protection
- Available in SOP14 Package and Leadless DFN4.5X3-14L Package
- AEC-Q100 Qualified for Automotive Application, Grade 1

Applications

- All Devices Supporting Highly Loaded CAN Networks
- Automotive and Transportation
  - Body Electronics / Lighting
  - Power Train / Chassis
  - Infotainment / Cluster
  - ADAS / Safety

Description

The TPT1145 is a CAN transceiver that meets the ISO11898 high-speed CAN (Controller Area Network) physical layer standard. The device is designed to be used in CAN FD networks up to 5 Mbps, with enhanced timing margin and higher data rates in long and highly loaded networks. As designed, the device features crosswire, overvoltage, and loss of ground protection from −70 V to +70 V, over-temperature shutdown, and a −30-V to +30-V common-mode input voltage range. The TPT1145 has a secondary power supply input for I/O level shifting the input pin thresholds and RXD output level. A serial peripheral interface (SPI) is provided for configuration and status retrieve. TPT1145 supports selective wake up and enables the Electronic Control Unit (ECU) to implement the partial networking function which is operating in an active state while it is in a low-power sleep mode. The device comes with the standby mode, which can be waked up from the CAN bus, and ultra-low power management controls the ECU in standby and sleep modes, then enable the power supply by inhibit output through the local or remote wake-up via wake-up pattern or wake-up frame identification. TPT1145 includes many protection features to enhance device and network robustness. There are two versions of the device, TPT1145Q and TPT1145NQ, the difference between the two versions is that the Device ID is different.

TPT1145 is available in SOP14 and DFN4.5X3.0-14L packages, and is characterized from –40°C to +125°C.

Typical Application Circuit

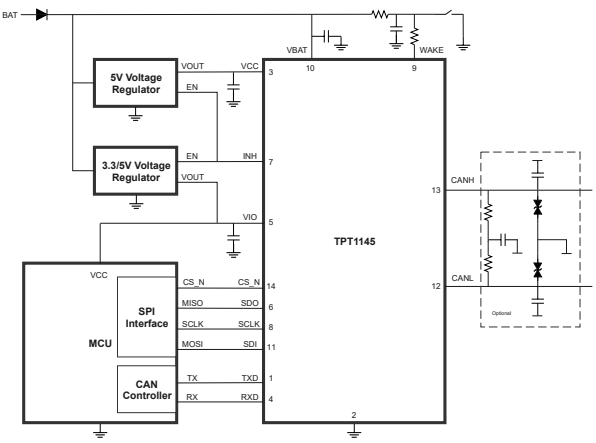

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Table of Contents

Product Family Table

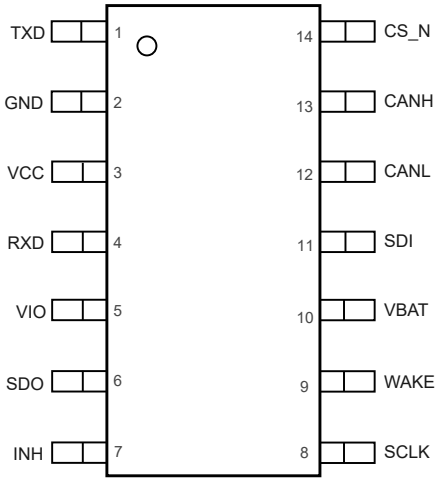
Order Number	VCC (V)	VIO (V)	BUS Protection (V)	Package
TPT1145Q-SO2R-S	4.5 to 5.5	2.8 to 5.5	±70	SOP14
TPT1145Q-DFKR-S	4.5 to 5.5	2.8 to 5.5	±70	DFN4.5X3-14L
TPT1145NQ-SO2R-S	4.5 to 5.5	2.8 to 5.5	±70	SOP14
TPT1145NQ-DFKR-S	4.5 to 5.5	2.8 to 5.5	±70	DFN4.5X3-14L

Revision History

Date	Revision	Notes
2021-08-12	Rev.Pre.0	Initial Version.
2022-12-20	Rev.A.0	Released Version.

Pin Configuration and Functions

TPT1145x
SOP14 Package
Top View



TPT1145x
DFN4.5x3-14 Package
Top View

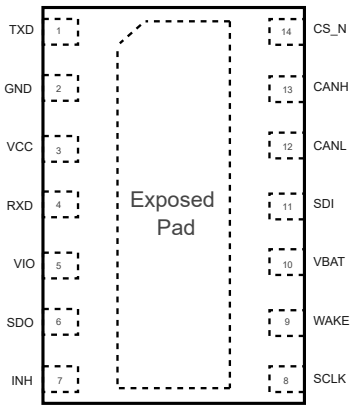


Table 1. Pin Functions: TPT1145x

Pin		I/O	Description
No.	Name		
1	TXD	Digital input	CAN transmit data input (low to drive dominant state and high to drive recessive state on CAN bus).
2	GND	GND	Ground, must be soldered to board ground.
3	VCC	Power	5-V CAN transceiver supply voltage.
4	RXD	Digital output	CAN receive data output (low for dominant and high for recessive bus states), output voltage adapted to the VIO input voltage.
5	VIO	Power	Supply voltage for Digital I/O level adaptor.
6	SDO	Digital output	SPI Serial data output, tri-state when CS_N is high.
7	INH	High voltage output	Inhibit pin to control external system voltage supplies.
8	SCLK	Digital input	SPI clock input.
9	WAKE	High voltage input	Local wake-up input.

Pin		I/O	Description
No.	Name		
10	VBAT	High voltage Power	High-voltage battery supply.
11	SDI	Digital input	SPI Serial data input.
12	CANL	Bus I/O	Low-level CAN bus line.
13	CANH	Bus I/O	High-level CAN bus line.
14	CS_N	Digital input	SPI Chip select input, active low.
	Exposed pad	GND	Thermal pad of DFN package, for enhanced thermal and electrical performance, it is required to solder the exposed pad to Ground.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{BAT}	Battery Supply Voltage Range	−0.3	60	V
V_{CC}	Power Supply Voltage Range	−0.3	7	V
V_{IO}	I/O Level-Shifting Voltage Range	−0.3	7	V
V_{BUS}	CAN Bus I/O Voltage Range (CANH, CANL)	−70	70	V
V_{BUS_DIFF}	Differential Voltage of CAN Bus (CANH - CANL)	−70	70	V
V_{LOGIC}	Logic Input and Output Terminal Voltage Range (TXD, RXD, SDI, SDO, SCK, CS_N)	−0.3	7	V
V_{WAKE}	WAKE Input Pin Voltage Range	−40	40	V
V_{INH}	INH Output Pin Voltage Range	−40	40	V
I_{O_LOGIC}	RXD Output Current	−8	8	mA
$I_{O\_INH\_}$	INH Output Current	−4	4	mA
I_{O_WAKE}	WAKE Output Current	−4	4	mA
T_J	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_{OTW}	Over-Temperature Warning Junction Temperature	-	135	°C
T_{OTP}	Over-Temperature Protection Junction Temperature	-	170	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD (Electrostatic Discharge Protection)

Parameter		Condition	Minimum Level	Unit
IEC	IEC Contact Discharge	IEC-61000-4-2, Bus Pin	±10	kV
	IEC Air-Gap Discharge	IEC-61000-4-2, Bus Pin	±15	kV
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001, All Pin	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002, All Pin	±1.5	kV
LU	Latch Up	Latch up, per JESD78, All Pin, 25℃	±500	mA
		Latch up, per JESD78, All Pin, 125℃	±100	mA
V_{tran}	ISO7637-2 transients per IEC 62228-3, CANH, CANL, WAKE, VBAT	Pulse 1	−100	V
		Pulse 2a	75	V
		Pulse 3a	−150	V
		Pulse 3b	100	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Description		Min	Max	Unit
V_{BAT}	Battery Supply Voltage Range	4.65	28	V
V_{IO}	Input/output voltage (TXD, RXD, SPI)	2.8	5.5	V
V_{CC}	CAN transceiver power supply	4.5	5.5	V
I_{OH_RXD}	RXD terminal HIGH level output current	−4	-	mA
I_{OL_RXD}	RXD terminal LOW level output current	-	4	mA
I_{O_INH}	INH output current	-	1	mA
T_A	Operating ambient temperature	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP14	65.2	34.1	°C/W
DFN4.5x3-14	38.4	33.2	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 4.5 V to 5.5 V, V_{IO} = 2.8 V to 5.5 V, V_{BAT} = 4.5 V to 28 V, R_L = 60 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Pin VBAT (Supply from battery)						
V_{BAT_R}	Power-on Detection on VBAT for Protected Mode	V_{BAT} rising	4.15	-	4.65	V
V_{BAT_F}	Power-off Detection on VBAT for Protected Mode	V_{BAT} falling	2.7	-	3.15	V
UV_{BAT_R}	Undervoltage Recovery on VBAT for Protected Mode	V_{BAT} rising	4.5	-	5	V
UV_{BAT_F}	Undervoltage Detection on VBAT for Protected Mode	V_{BAT} falling	4.15	-	4.65	V
V_{HYS_UVBAT}	Hysteresis Voltage on U_{VBAT} (1)		-	350	-	mV
I_{BAT}	Battery Supply Current	Normal mode	-	1	1.5	mA
		Sleep mode, CAN Offline Mode, 4.5V ≤ V_{BAT} ≤ 28V	-	45	70	μA
		Standby mode, CAN Offline Mode, 4.5V ≤ V_{BAT} ≤ 28V	-	50	73	μA
		Additional current in CAN Offline Bias Mode, CAN bus is connected to 2.5V	-	40	70	μA
		Additional current in CAN Offline Bias Mode when selective wake is enabled and CAN bus active(1)	-	0.4	0.55	mA
		Additional current from WAKE input	-	1	2	μA
Pin VCC (Power Supply)						
V_{CC}	Supply Voltage		4.5	-	5.5	V
UV_{VCC_R}	Undervoltage Recovery on V_{CC} for Protected Mode	V_{CC} Rising	-	4.6	4.8	V
UV_{VCC_F}	Undervoltage Detection on V_{CC} for Protected Mode	V_{CC} Falling	4.25	4.4	-	V
V_{HYS_UVVCC}	Hysteresis Voltage on U_{VVCC} (1)		-	200	-	mV
I_{CC}	Supply Current	Normal mode (recessive), V_{TXD} = V_{IO}, R_L = 50 Ω, C_L = open	-	3	6	mA

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
		Normal mode (dominant), V_{TXD} = 0 V, R_L = 50 Ω, C_L = open	-	40	70	mA
		Standby/Normal mode, CAN inactive, V_{TXD} = V_{CC}, selective wake off, R_L = 50 Ω, C_L = open	-	4	8.5	μA
		Sleep mode, CAN inactive, TXD = V_{CC}, R_L = 50 Ω, C_L = open	-	1.2	6	μA
		Dominant with bus fault, short circuit on bus line, V_{TXD} = 0 V, −3V < (V_{CANH} = V_{CANL}) < +18V, R_L = Open, C_L = open	-	50	70	mA
Pin VIO (I/O Supply)						
V_{IO}	Supply Voltage on V_{IO} Pin		2.8	-	5.5	V
UV_{VIO_R}	Undervoltage Recovery on V_{IO} for Protected Mode	V_{IO} Rising	-	2.8	2.85	V
UV_{VIO_F}	Undervoltage Detection on V_{IO} for Protected Mode	V_{IO} Falling	2.45	2.6	-	V
V_{HYS_UVVIO}	Hysteresis Voltage on U_{VVIO} for Protected Mode (1)		-	200	-	mV
I_{IO}	Supply Current from VIO	Normal and Standby mode, V_{TXD} = V_{IO}	-	7	11	μA
		Sleep mode	-	3	8	μA
Pin SDI, SCK, CS_N (Serial Peripheral Interface Inputs)						
V_{IH_SPI}	High-Level Input Voltage	3 V ≤ V_{IO} ≤ 5.5 V	0.7 x V_{IO}	-	-	V
V_{IL_SPI}	Low-Level Input Voltage	3 V ≤ V_{IO} ≤ 5.5 V	-	-	0.3 x V_{IO}	
V_{HYS_SPI}	Hysteresis Voltage on SPI Inputs (1)	3 V ≤ V_{IO} ≤ 5.5 V	0.05 x V_{IO}	-	-	V
I_{IH}	High-Level Input Leakage Current(1)	3 V ≤ V_{IO} ≤ 5.5 V	−1	-	1	μA
I_{IL}	Low-Level Input Leakage Current(1)	Input = 0 V, 3 V ≤ V_{IO} ≤ 5.5 V	−30	-	-2	μA
I_{IL_CSN}	Low-Level Input Leakage Current for CS_N(1)	Input = 0 V, 3 V ≤ V_{IO} ≤ 5.5 V	−50	-	-2	μA
I_{LKG_OFF}	Unpowered Leakage Current	V_{BAT} = V_{CC} = V_{IO} = 0 V	−1	-	1	μA
C_{IN}	Input Capacitance (1)	At 20MHz	4	-	15	pF
R_{PD_SCK}	SCK Pin Pull-Down Resistance		40	60	80	kΩ
R_{PU_CSN}	CS_N Pin Pull-Up Resistance		40	60	80	kΩ
R_{PD_SDI}	SDI Pin Pull-Down Resistance		40	60	80	kΩ

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
R_{PU_SDI}	SDI Pin Pull-Up Resistance			40	60	80	kΩ
Pin SDO (Serial Peripheral Interface Outputs)							
V_{OH_SPI}	High-Level Output Voltage		I_{OH} = −4 mA	V_{IO} – 0.4	-	-	V
V_{OL_SPI}	Low-Level Output Voltage		I_{OH} = 4 mA	-	-	0.4	V
I_{LKG_OFF}	Unpowered Leakage Current		V_{CSN} = V_{IO}, 0V ≤ V_O ≤ V_{IO}	−5	-	5	μA
Pin INH (Inhibit high voltage output)							
V_{O_INH}	High-Level Output Voltage		I_{INH} = −180 μA	V_{BAT} – 0.8	-	V_{BAT}	V
R_{PD_INH}	INH Pin Pull-Down Resistance		Sleep mode	3	4	5	MΩ
Pin TXD (CAN transmit data input)							
V_{IH_TXD}	High-Level Input Voltage		3 V ≤ V_{IO} ≤ 5.5 V	0.7 x V_{IO}	-	-	V
V_{IL_TXD}	Low-Level Input Voltage		3 V ≤ V_{IO} ≤ 5.5 V	-	-	0.3 x V_{IO}	V
V_{HYS_TXD}	Hysteresis Voltage on TXD Inputs		3 V ≤ V_{IO} ≤ 5.5 V	0.05 x V_{IO}	-	-	V
R_{PU_TXD}	TXD Pin Pull-Up Resistance		V_{TXD}=V_{IO}-1.8V	40	60	80	kΩ
Pin RXD (CAN Receive Data Output)							
V_{OH_RXD}	High-Level Output Voltage		IO = −4 mA	VIO – 0.4	-	-	V
V_{OL_RXD}	Low-Level Output Voltage		IO = 4 mA	-	-	0.4	V
Pin WAKE (Local wake-up pin)							
V_{IH_WAKE}	High-Level Input Voltage			3	-	3.8	V
V_{IL_WAKE}	Low-Level Input Voltage			2.5	-	3.4	V
V_{HYS_WAKE}	Hysteresis Voltage on WAKE Inputs (1)			250	325	400	mV
I_{IL}	Low-Level Input Current		WAKE = 1 V	-	-	1.5	μA
Pin CANH, CANL (CAN Bus lines)							
$V_{O(DOM)}$	Dominant Bus Output Voltage	CANH	CAN active mode, VTXD = 0 V, 50 Ω ≤ RL ≤ 65 Ω, CL = open, t < $t_{to(dom)TXD}$	2.75	3.5	4.5	V
		CANL		0.5	1.5	2.25	V
V_{SYM_DC}	DC Output Symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$– $V_{O(CANL)}$)		VCC = 5 V, RL = 60 Ω, CL = open,	−0.4	-	0.84	V
V_{SYM}	Transient Symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$) / V_{CC} (1)		4.75 V ≤ VCC ≤ 5.25 V, RL = 60 Ω, CL = open, C_{SPLIT} = 4.7 nF, T_{XD} = 250 kHz, 1 MHz, 2.5 MHz	0.9	1.0	1.1	V/V

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OD_DOM}	Differential Output Voltage (dominant)		CAN active mode, t < $t_{to(dom)TXD}$, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TXD} = 0 V, 45 Ω ≤ R_L < 50 Ω, C_L = open	1.5	-	3	V
			CAN active mode, t < $t_{to(dom)TXD}$, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TXD} = 0 V, 50 Ω ≤ R_L < 65 Ω, C_L = open	1.5	-	3	V
			CAN active mode, t < $t_{to(dom)TXD}$, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TXD} = 0 V, 65 Ω ≤ R_L ≤ 70 Ω, C_L = open	1.5	-	3.3	V
			CAN active mode, t < $t_{to(dom)TXD}$, 4.75 V ≤ V_{CC} ≤ 5.25 V, V_{TXD} = 0 V, R_L = 2240 Ω, C_L = open	1.5	-	5.5	V
V_{OD_REC}	Differential Output Voltage (recessive)		CAN active mode, V_{TXD} = V_{IO}, no load	−50	-	50	mV
			CAN Offline mode, no load	−0.2	-	0.2	V
V_{O_REC}	Recessive Output Voltage		CAN Active mode, V_{TXD} = V_{IO} = V_{CC}, no load	2	0.5 x VCC	3	V
			CAN Offline mode; no load	−0.1	-	0.1	V
			CAN Offline Bias and Silent modes; no load; V_{CC} = 0 V	2	2.5	3	V
$I_{O\_SC\_DOM}$	Dominant Short-Circuit Output Current	CANH	CAN active mode, −15 V ≤V_{CANH} ≤ 18 V, CANL = open, V_{TXD} = 0 V	−115	-	-	mA
		CANL	CAN active mode, −15 V ≤V_{CANL} ≤ 18 V CANH = open, V_{TXD} = 0 V	-	-	115	mA
$I_{O\_SC\_REC}$	Recessive Short-Circuit Output Current		−27 V ≤V_{CANH} / V_{CANL} ≤ 32 V, V_{TXD} = VCC, normal modes	−5	-	5	mA
$V_{TH\_RX\_DIF}$	Differential Receiver Threshold Voltage		CAN active mode or Silent mode −12 V ≤ V_{CANH} / V_{CANL} ≤ 12 V	0.5	0.7	0.9	V
			CAN offline mode, −12 V ≤ V_{CANH} / V_{CANL} ≤ 12 V	0.4	0.7	1.15	V
V_{REC_RX}	Receiver Recessive Voltage		CAN active mode or Silent mode, Bus bias active −12 V ≤V_{CANH} / V_{CANL} ≤ 12 V	−3	-	0.5	V
			CAN offline mode, Bus bias inactive	−3	-	0.4	V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
		−12 V ≤V_{CANH} / V_{CANL} ≤ 12 V				
V_{DOM_RX}	Receiver Dominant Voltage	CAN active mode or Silent mode, Bus bias active −12 V ≤ V_{CANH} / V_{CANL} ≤ 12 V	0.9	-	8	V
		CAN offline mode, Bus bias inactive −12 V ≤V_{CANH} / V_{CANL} ≤ 12 V	1.15	-	8	V
$V_{HYS\_RX\_DIF}$	Differential Receiver Hysteresis Voltage(1)	CAN active mode or Silent mode, −12 V ≤V_{CANH} / V_{CANL} ≤ 12 V	1	30	100	mV
R_{IN}	Input Resistance (CANH or CANL)	V_{TXD} = V_{CC} = V_{IO} = 5 V, −2 V ≤V_{CANH} / V_{CANL} ≤ 7 V	10	23	35	kΩ
R_{IN_M}	Input Resistance Matching: [1 − $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%	V_{TXD} = V_{CC} = V_{IO}= 5 V	−2	-	+2	%
R_{ID}	Differential Input Resistance	V_{TXD} = V_{CC} = V_{IO} = 5 V, −2 V ≤V_{CANH} / V_{CANL} ≤ 7 V	30	47	60	kΩ
C_I	Input Capacitance to Ground (CANH or CANL) (1)		-	-	20	pF
C_{ID}	Differential Input Capacitance (1)		-	-	10	pF
I_L	Leakage Current	V_{BAT} = V_{CC}= 0 V or V_{BAT} = V_{CC} shorted to ground via 47 kΩ; V_{CANH} = 5 V, V_{CANL} = 5 V	−5	-	5	μA

(1) The typical data is based on bench test and design simulation. V_{sym} = 0.9 ~ 1.1 V/V at 250 kbps.

AC Timing Requirements

All test conditions: V_{CC} = 4.5 V to 5.5 V, V_{IO} = 2.8 V to 5.5 V, V_{BAT} = 4.5 V to 28 V, R_L = 60 Ω, T_A = −40°C to 125°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Pin BAT, VCC, VIO (Power supply)						
t_{PWRUP}	Power-up Time	Time from V_{BAT}exceeding the power-on detection threshold(V_{BAT_R}) until INH active	-	2.8	4.7	ms
t_{d_UV}	Under Voltage Detection Delay Time		20	-	60	µs
t_{d_UVSLP}	Delay from Undervoltage Detection to Sleep Mode(1)	Time from $U_{VCC}$and/or U_{VIO}event until transition to Sleep mode	200	-	400	ms
Pin CS_N, SCLK, SDI, SDO (SPI timing)						
f_{SCLK}	SPI Clock Frequency(1)	Normal, Standby mode, Sleep mode	-	-	4	MHz
t_{SCLK}	SPI Clock Period(1)	Normal, Standby mode, Sleep mode	250	-	-	ns
t_{CSS}	SPI Chip Select Setup Time(1)	Normal and Standby mode	100	-	-	ns
		Sleep mode	500	-	-	ns
t_{CSH}	SPI Chip Select Hold Time(1)	Normal and Standby mode	100	-	-	ns
		Sleep mode	500	-	-	ns
t_{CLK_H}	SPI Clock High Time(1)	Normal and Standby mode	100	-	-	ns
		Sleep mode	500	-	-	ns
t_{CLK_L}	SPI Clock Low Time(1)	Normal and Standby mode	100	-	-	ns
		Sleep mode	500	-	-	ns
t_{DI_SU}	SPI Data Input Setup Time(1)	Normal and Standby mode	50	-	-	ns
		Sleep mode	200	-	-	ns
t_{DI_H}	SPI Data Input Hold Time(1)	Normal and Standby mode	50	-	-	ns
		Sleep mode	200	-	-	ns
t_{DO_V}	SPI Data Output Valid Time	pin SDO; C_L= 20 pF; Normal and Standby modes	-	-	100	ns
		pin SDO; C_L= 20 pF; Sleep modes	-	-	100	ns
$t_{d\_SDI-SDO}$	SDI to SDO Delay Time	SPI address bits and read-only bit; C_L = 20 pF(1)	-	-	50	ns
t_{CS_WH}	SPI Chip Select Pulse Width High(1)	pin SDO; Normal and Standby modes	250	-		ns
		pin SDO; Sleep mode	1	-		µs

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d\_SCLKL-CSL}$	Delay Time from SCLK Low to CS_N Low(1)		50	-	-	ns
Transceiver Switching Characteristics						
t_{pLD}	Propagation Delay Time, Low TXD to Driver Dominant (recessive to dominant)(1)	Normal mode, R_L= 60 Ω, C_L = 100 pF	-	60	100	ns
t_{pHR}	Propagation Delay Time, High TXD to Driver Recessive (dominant to recessive)(1)		-	60	100	ns
t_{SK_P}	Pulse Skew ($\|t_{pHR} - t_{pLD}\|$) (1)		-	10	35	ns
t_R	Differential Output Signal Rise Time(1)		-	45	-	ns
t_F	Differential Output Signal Fall Time(1)		-	45	-	ns
t_{pRH}	Propagation Delay Time, Bus Recessive Input to RXD High Output (Dominant to Recessive)(1)	V_{STB}= 0 V, $C_{L(RXD)}$= 15 pF	-	90	120	ns
t_{pDL}	Propagation Delay Time, Bus Dominant Input to RXD Low Output (Recessive to Dominant)(1)		-	90	120	ns
t_{R_R}	RXD Output Signal Rise Time(1)		-	20	-	ns
t_{R_F}	RXD Output Signal Fall Time(1)		-	20	-	ns
$t_{PROP\_TXDL-RXDL}$	Total loop delay, driver input (TXD) low to receiver output (RXD) low, recessive to dominant(1)	Normal mode, R_L= 60 Ω, C_L = 100 pF, $C_{L(RXD)}$= 15 pF,	-	110	220	ns
$t_{PROP\_TXDH-RXDH)}$	Total loop delay, driver input (TXD) high to receiver output (RXD) high, dominant to recessive(1)		-	140	220	ns
FD Timing Parameters						
t_{BIT_BUS}	Bit time on CAN bus output pins with t_{BIT_TXD} = 500 ns(1)	R_L= 60 Ω, C_L= 100 pF, $C_{L(RXD)}$= 15 pF, Δt_{REC}= t_{BIT_RXD} − t_{BIT_BUS}	435	-	530	ns
	Bit time on CAN bus output pins with t_{BIT_TXD} = 200 ns(1)		155	-	210	ns
t_{BIT_RXD}	Bit time on RXD output pins with t_{BIT_TXD} = 500 ns		400	-	550	ns
	Bit time on RXD output pins with t_{BIT_TXD} = 200 ns		120	-	220	ns
Δt_{REC}	Receiver timing symmetry with t_{BIT_TXD} = 500 ns(1)		−65	-	40	ns

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Receiver timing symmetry with $t_{BIT(TXD)}$= 200 ns(1)		−45	-	15	ns
Device Timing Parameters						
t_{WAKE_FILT}	Bus time to meet filtered bus requirement for wake-up request	Pulse for wake-up on pins CANH and CANL	0.5	-	1.8	µs
t_{WAKE_TO}	Bus wake-up time out-time	Between first and second dominant pulses; CAN Offline mode	0.8	-	10	ms
t_{TXD_DTO}	TXD dominant time-out time	normal mode, R_L= 60 Ω, C_L = open, V_{TXD}= 0V	2.7	-	3.3	ms
$t_{SILENCE}$	Bus Silence time-out time(1)	Timeout for bus inactivity. Timer is reset and restarted when bus changes from dominant to recessive or vice versa.	0.95	-	1.2	s
$t_{d\_ACT-BIAS}$	Delay time form bus active to bias		-	-	200	µs
t_{SU_CAN}	CAN start-up time	When switching to Active mode	-	-	220	µs
CAN Partial Networking						
N_{idle_bits}	Number of idle bits(1)	Before a new SOF is accepted	6	-	10	
t_{fltr_dom}	Dominant bit filter time(1)	arbitration data rate ≤ 500 kbps	5	-	8.75	%
Pin RXD Interrupt/wake-up Timing						
t_{d_event}	Event capture delay time	CAN offline mode	0.9	-	1.1	ms
t_{blank}	Blanking time	Switching from Offline mode to Active or Silent mode	-	-	30	µs
Pin WAKE						
t_{WAKE}	Wake up time		50	-	-	µs
Pin INH						
t_{d_BW-INH}	Delay time from bus wake-up to INH high		-	-	100	µs

(1) The test data is based on bench test and design simulation.

Parameter Measurement Information

Test Circuit

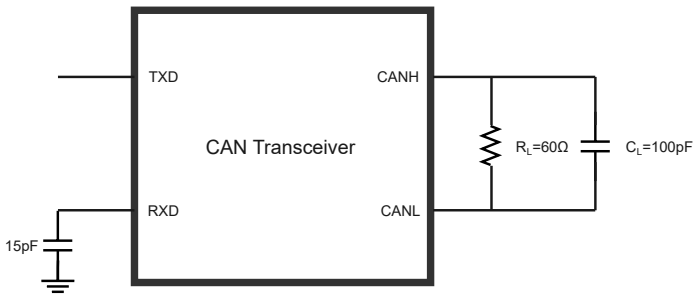


Figure 1. CAN Transceiver Timing Parameter Test Circuit

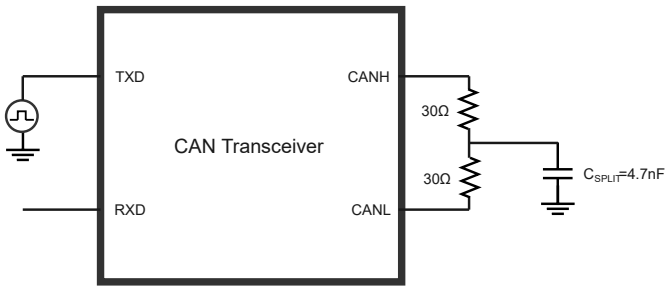


Figure 2. CAN Transceiver Driver Symmetry Test Circuit

Parameter Diagram

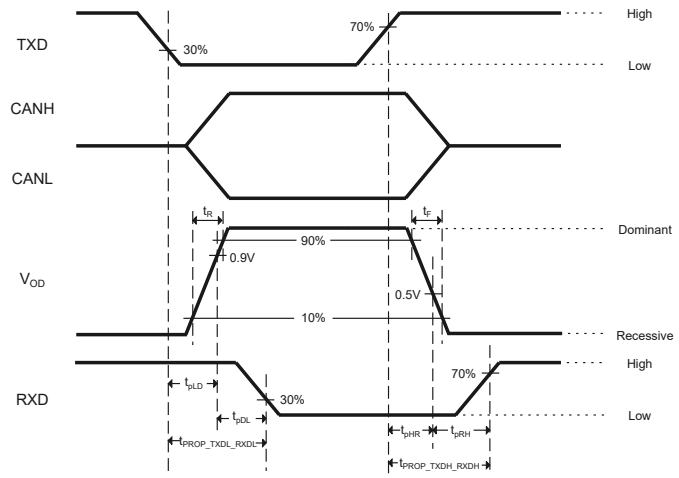


Figure 3. CAN Transceiver Timing Diagram

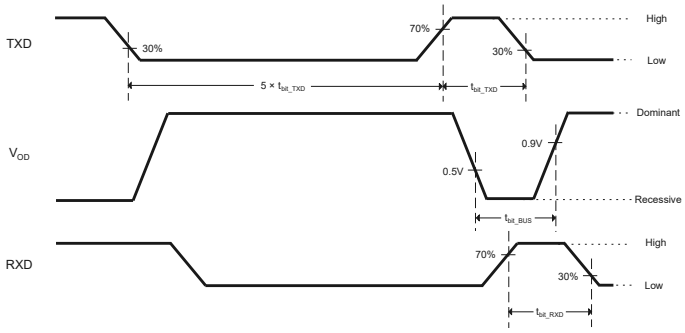


Figure 4. CAN FD Timing Parameter Diagram

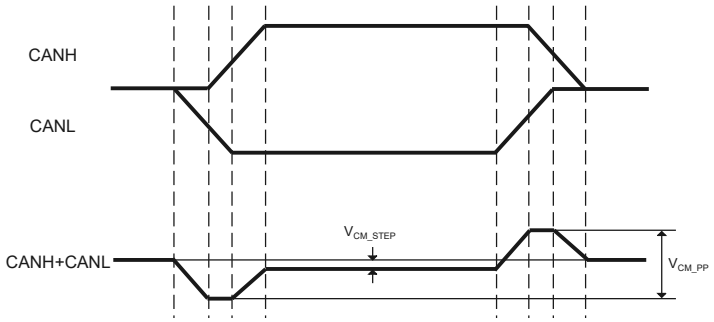


Figure 5. CAN Bus Common-Mode Voltage

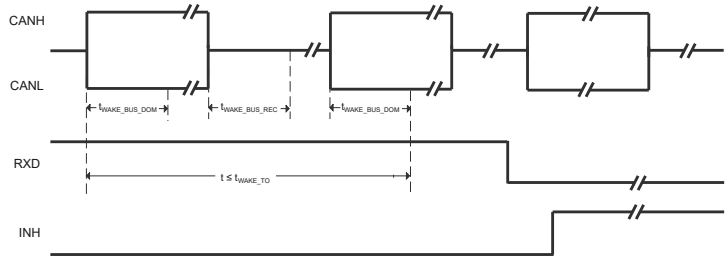


Figure 6. Wake-up timing Diagram

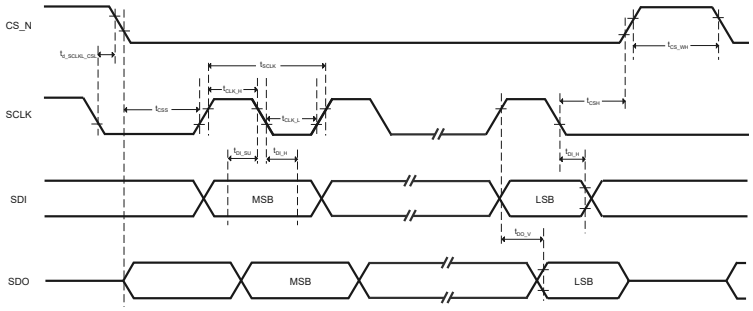


Figure 7. SPI Timing Parameter Diagram

Detailed Description

Overview

The TPT1145 is a CAN transceiver which meets the ISO11898 High Speed CAN (Controller Area Network) physical layer standard. The device is designed to be used in CAN FD networks up to 5 Mbps, with enhanced timing margin and higher data rates in long and highly loaded networks. As designed, the device features crosswire, overvoltage and loss of ground protection from −70 V to +70 V, overtemperature shutdown, and a −30 V to +30 V common-mode input voltage range. The TPT1145 has a secondary power supply input for I/O level shifting the input pin thresholds and the RXD output level. A serial peripheral interface (SPI) is provided for configuration and status retrieve. TPT1145 supports selective wake up and enables the Electronic Control Unit (ECU) to implement the Partial Networking function which is operating in an active state while it is in a low-power sleep mode. The device comes with the standby mode, which can be waked up from CAN BUS, and ultra-low power management controls the ECU in standby and sleep modes, then enables the power supply by inhibit output through the local or remote wake-up via wake-up pattern or wake-up frame identification. TPT1145 includes many protection features to enhance device and network robustness. There are two versions of the device, TPT1145Q and TPT1145NQ, the difference between the two versions is that the Device ID is different.

Functional Block Diagram

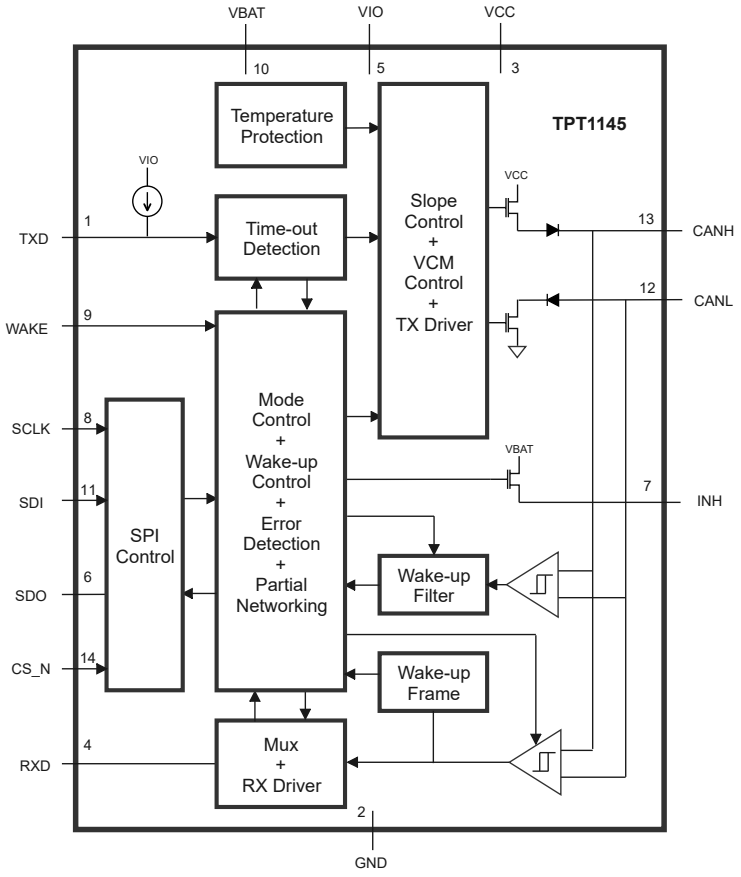


Figure 8. Functional Block Diagram

Feature Description

Table 2. Driver Function Table

Device Mode	Inputs	Outputs		Driven BUS State
	TXD	CANH	CANL	
Normal	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Standby	X	Z	Z	Biased to GND
Silent	X	Z	Z	Biased to 2.5V
Sleep	X	Z	Z	Biased to GND

Table 3. Receiver Function Table

Device Mode	CAN Differential Inputs VID = VCANH – VCANL	BUS State	RXD Terminal
Normal or Standby	$V_{ID} \geq V_{IT+(MAX)}$	Dominant	L
	$V_{IT-(MIN)} < V_{ID} < V_{IT+(MAX)}$	Indeterminate	Indeterminate
	$V_{ID} \leq V_{IT-(MIN)}$	Recessive	H
	Open ($V_{ID} \approx 0$ V)	Open	H

System Controller Operating Modes

The device system controller has 5 operating modes: normal mode, standby mode, sleep mode, off mode, and over-temperature mode.

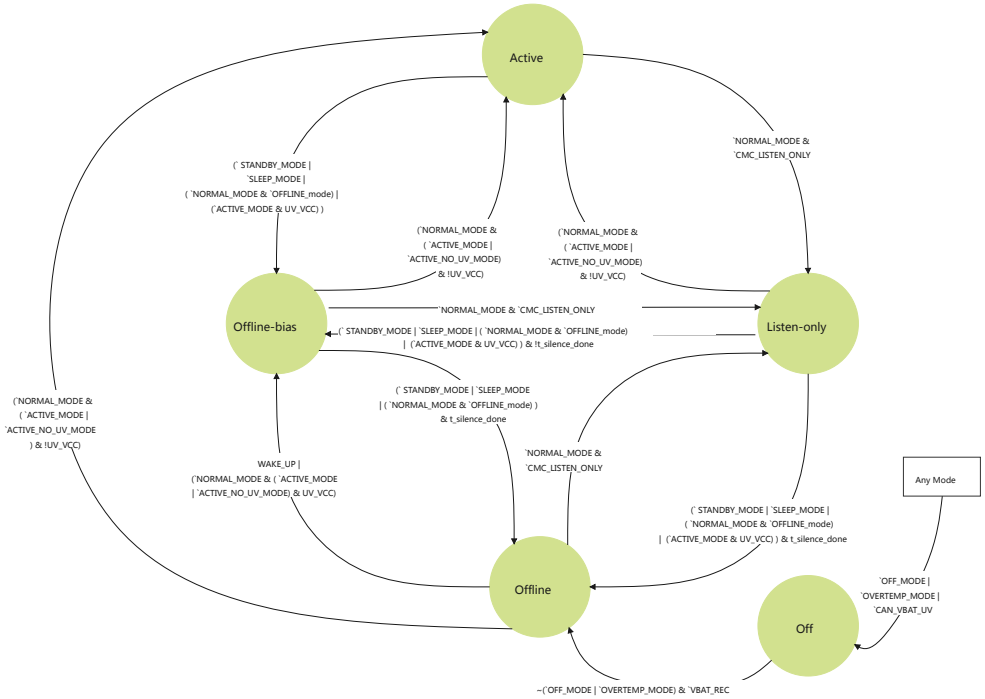


Figure 9. Mode Transition State Diagram

Normal Mode

This is the normal operating mode of the device. In the normal mode, the device is fully operational, and all block is available.

Standby Mode

This is the first level of the low-power mode. In the standby mode, the driver and receiver of the CAN transceiver are disabled, and the device is unable to transmit or receive data. The low-power receiver is monitoring bus activity for valid wake-up requirements. The CAN bus pin is biased to the ground. The INH pin is active to enable the voltage regulator controlled by the INH pin. The pins RXD will reflect active wake-up requests as that V_{IO} and V_{BAT} are powered.

Sleep Mode

This is the second level of low-power mode as well as the lowest power mode. In the sleep mode, the driver and receiver of the CAN transceiver are disabled, and the device is unable to transmit or receive data, the low-power receiver is monitoring bus activity for valid wake-up requirements. The CAN bus pin is biased to the ground. The INH pin is floating to disable the voltage regulator controlled by the INH pin for additional system-level power saving.

Off Mode

This is the default mode when V_{BAT} is first powered, and the device will switch to the off mode if V_{BAT} drops below the power off threshold V_{BAT_F}. The CAN bus pins and INH pin are in High-Z state in off mode. When V_{BAT} rises above the power on the threshold V_{BAT_R}, the device will re-boot and will switch to standby mode after t_{SU_CAN}.

Over-Temperature Mode

Over-temperature mode will prevent the device from over-heated induced damage. The device will switch to over-temperature mode as soon as the junction temperature rises above the over-temperature warning threshold T_{OTW}. The CAN driver and receiver are disabled, and CAN bus pins are High-Z state in over-temperature mode.

High-Speed CAN Transceiver Operating Mode

The high-speed CAN transceiver has 4 operating modes: active mode, silent mode, offline mode, and Offline bias mode. Operating mode selection is made via register setting of bits CMC.The CAN transceiver operating mode can be selected

among the offline mode, active mode, and silent mode via register setting in the normal mode. The CAN transceiver is forced to go into the offline mode or offline bias mode when the device is in the standby mode or sleep mode.

Active Mode

In the active mode, the CAN driver and receiver block are fully operational, the transceiver will transmit and receive data via the bus lines CANH and CANL. The driver translates the digital input data on the TXD pin to differential analog output on the CAN bus. The receiver translates the differential analog data on the CAN bus to digital data output to the RXD pin. The slopes of the CAN bus output signals are controlled by the internal circuit that optimized the Electro Magnetic Emission (EME) performance.

Silent Mode

This is the listen-only mode and receive-only mode of the device. In the silent mode, the driver is disabled, releasing the bus pins to a recessive state. All other blocks, including the receiver, continue to operate in the normal mode. The silent mode can be used to prevent a faulty CAN controller from disrupting CAN bus network communications.

Offline Mode and Offline Bias Mode

The transceiver monitors the CAN bus for wake-up event in the offline mode if the CAN wake-up detection function is enabled. The CAN bus are biased to ground.The transceiver monitors the CAN bus for wake-up event in the offline mode if the CAN wake-up detection function is enabled. The CAN bus are biased to 2.5 V. The offline bias mode is activated automatically when the activity is detected on the CAN bus while the transceiver in the CAN offline mode. The transceiver will return to the offline mode if there is no edges on the CAN bus for longer than $t_{SILENCE}$.

Device Local Faults

TXD Dominant Time-out

The device is featured with the TXD dominant time-out detection function. This function prevents a permanent low on the TXD pin, resulting in the CAN bus being driven into permanent dominant, which will cause the CAN bus network communication blocked. If the TXD remains low for longer than t_{TXD_DTO}, the transmitter will be disabled until the fault flag has been cleared.

TXD Shorted to RXD Detection

The device is featured with the function of a short circuit between TXD and RXD detection. This function prevents the CAN bus from being locked in permanent dominance, which will result in the CAN bus network communication blocked. The transmitter will be disabled until the fault flag has been cleared.

Under-Voltage Lockout (UVLO)

The device integrates an under-voltage detect and lockout circuit of the supply terminal to keep the device in the protected mode if the supply voltage drops below the threshold until the supply voltage is higher than the UVLO threshold. This protects the device and system during under-voltage events on supply terminals.

Over-Temperature Protection (OTP)

The device integrates over-temperature protection circuit to prevent the device from over-heated induced damage. When the junction temperature is higher than the over-temperature protection threshold T_{OTP}, the device will shut down until the junction temperature T_J drops below T_{OTW}.

CAN Partial Networking Configuration Registers

Dedicated registers are provided for configuring CAN partial networking.

Table 4. Data rate register (address 26h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

Table 5. ID registers 0 to 3 (addresses 27h to 2Ah)

Addr.	Bit	Symbol	Access	Value	Description
27h	7:0	ID7:ID0	R/W	-	bits ID7 to ID0 of the extended frame format
28h	7:0	ID15:ID08	R/W	-	bits ID15 to ID8 of the extended frame format
29h	7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format
	1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format
2Ah	7:5	reserved	R	-	
	4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format

Table 6. ID mask registers 0 to 3 (addresses 2Bh to 2Eh)

Addr.	Bit	Symbol	Access	Value	Description
2Bh	7:0	M7:M0	R/W	-	ID mask bits 7 to 0 of extended frame format
2Ch	7:0	M15:M8	R/W	-	ID mask bits 15 to 8 of extended frame format

Table 7. ID mask registers 0 to 3 (addresses 2Bh to 2Eh)

Addr.	Bit	Symbol	Access	Value	Description
2Dh	7:2	M23:M18	R/W	-	ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format
	1:0	M17:M16	R/W	-	ID mask bits 17 to 16 of extended frame format
2Eh	7:5	reserved	R	-	
	4:0	M28:M24	R/W	-	ID mask bits 28 to 24 of extended frame format ID mask. bits 10 to 6 of standard frame format

Table 8. Frame control register (address 2Fh)

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are ‘don’t care’ for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected

Table 9. Data mask registers (addresses 68h to 6Fh)

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	data mask 0 configuration
69h	7:0	DM1	R/W	-	data mask 1 configuration
6Ah	7:0	DM2	R/W	-	data mask 2 configuration
6Bh	7:0	DM3	R/W	-	data mask 3 configuration
6Ch	7:0	DM4	R/W	-	data mask 4 configuration
6Dh	7:0	DM5	R/W	-	data mask 5 configuration
6Eh	7:0	DM6	R/W	-	data mask 6 configuration
6Fh	7:0	DM7	R/W	-	data mask 7 configuration

DM_SEQ_SEL = 0, DLC = 8, DM0 is compared with Data0, while DM7 is compared with Data7, DLC = 1, DM7 is compared with Data0

DM_SEQ_SEL = 1, DLC = 8, DM0 is compared with Data7, while DM7 is compared with Data0, DLC = 0, DM7 is compared with Data0

r_dm_seq_sel = 0

DLC > 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7
		Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7
DLC = 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7
		Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7
DLC = 7			DM1	DM2	DM3	DM4	DM5	DM6	DM7
			Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6
DLC = 6				DM2	DM3	DM4	DM5	DM6	DM7
				Data 0	Data 1	Data 2	Data 3	Data 4	Data 5
DLC = 5					DM3	DM4	DM5	DM6	DM7
					Data 0	Data 1	Data 2	Data 3	Data 4
DLC = 4						DM4	DM5	DM6	DM7
						Data 0	Data 1	Data 2	Data 3
DLC = 3							DM5	DM6	DM7
							Data 0	Data 1	Data 2
DLC = 2								DM6	DM7
								Data 0	Data 1
DLC = 1									DM7
									Data 0

r_dm_seq_sel = 1

DLC > 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7
		Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
DLC = 8		DM0	DM1	DM2	DM3	DM4	DM5	DM6	DM7
		Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
DLC = 7			DM1	DM2	DM3	DM4	DM5	DM6	DM7
			Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
DLC = 6				DM2	DM3	DM4	DM5	DM6	DM7
				Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
DLC = 5					DM3	DM4	DM5	DM6	DM7
					Data 4	Data 3	Data 2	Data 1	Data 0
DLC = 4						DM4	DM5	DM6	DM7
						Data 3	Data 2	Data 1	Data 0
DLC = 3							DM5	DM6	DM7
							Data 2	Data 1	Data 0
DLC = 2								DM6	DM7
								Data 1	Data 0
DLC = 1									DM7
									Data 0

Device ID

A byte A byte is reserved at address 0x7E for a TPT1145 identification code.

Table 10. Identification register (address 7Eh)

Bit	Symbol	Access	Value	Description
7:0	IDS[7:0]	R		Device identification code
			04h	TPT1145Q
			74h	TPT1145NQ

Register Map

The addressable register space contains 128 registers with addresses from 0x00 to 0x7F. An overview of the register mapping is provided below.

Register name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit description
MODE_CONTROL(1)	0x01	7:3	Reserved	Null	5'h0	
		2:0	MC	CRW	3'h4	mode control 001: sleep 100: standby 111: normal
MAIN_STATUS	0x03	7	FSMS	R/O	1'h0	sleep mode transceiver status 0:by SPI 1:by VCC/VIO undervoltage. bus only can read. Logic can write
		6	OTWS	R/O	1'h0	overtemperature warning status 0: below 1: above. Bus only can read. Logic can write
		5	NMS	R/O	1'h1	normal mode status 0: entered normal mode(power-up) 1: not enter normal mode. Bus only can read. Logic can configuration
		4:0	Reserved	Null	5'h0	
SYSTEM_EVENT_ENABLE	0x04	7:3	Reserved	Null	5'h0	
		2	OTWE	R/W	1'h0	1: overtemperature warning enable 0: overtemperature warning disable
		1	SPIFE	R/W	1'h0	1: SPI failure enable. 0: SPI failure disable
		0	Reserved	Null	1'h0	
GPM_07_00	0x06	7:0	GPM_07_00	R/W	8'h0	memory0
GPM_15_08	0x07	7:0	GPM_15_08	R/W	8'h0	memory1
GPM_23_16	0x08	7:0	GPM_23_16	R/W	8'h0	memory2

Register name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit description
GPM_31_24	0x09	7:0	GPM_31_24	R/W	8'h0	memory3
LOCK_CONTROL	0x0a	7	Reserved	Null	1'h0	
		6	LK6C	R/W	1'h0	lock 0x68-0x6F 0: SPI write-access enable 1: SPI write-access disable
		5	LK5C	R/W	1'h0	lock 0x50-0x5F. 0: SPI write-access enable 1: SPI write-access disable
		4	LK4C	R/W	1'h0	lock 0x40-0x4F 0: SPI write-access enable 1: SPI write-access disable
		3	LK3C	R/W	1'h0	lock 0x30-0x3F 0: SPI write-access enable 1: SPI write-access disable
		2	LK2C	R/W	1'h0	lock 0x20-0x2F 0: SPI write-access enable 1: SPI write-access disable
		1	LK1C	R/W	1'h0	lock 0x10-0x1F 0: SPI write-access enable 1: SPI write-access disable
		0	LK0C	R/W	1'h0	lock 0x06-0x09 0: SPI write-access enable 1: SPI write-access disable
CAN_CONTROL	0x20	7	Reserved	Null	1'h0	
		6	CFDC	R/W	1'h0	CAN FD tolerance 0: disable 1: enable
		5	PNCOK	RWC	1'h0	CAN partial networking configurate 0: invalid. Only WUP enable 1: partial network config ok. Bus can write and read. and logic can clear it

Register name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit description
		4	CPNC	RWC	1'h0	CAN selective wake-up 0: disable CAN selective wake-up 1: enable CAN selective wake-up. Bus can write and read. and logic can clear it
		3:2	Reserved	Null	2'h0	
		1:0	CMC	R/W	2'h1	CAN transceiver mode 00: offline 01: active-Vcc undervoltage detection active 10: active-Vcc undervoltage detection inactive 11: listen only
TRANSCEIVER_STATUS	0x22	7	CTS	R/O	1'h0	CAN transceiver status 0: not in active 1: in active. Bus only can read. logic can write
		6	CPNERR	R/O	1'h1	CAN partial networking err status 0:no err detected 1:err detected. Bus only can read. Logic can write
		5	CPNS	R/O	1'h0	CAN partial networking status 0: configuration error detected 1: configuration ok. Bus only can read. Logic can write
		4	COSCS	R/O	1'h0	CAN oscillator status 0: not running at target frequency 1: running at target frequency. Bus only can read. Logic can write
		3	CBSS	R/O	1'h1	CAN bus silence status 0: CAN bus active

Register name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit description
						1: CAN bus inactive. Bus only can read. Logic can write
		2	Reserved	Null	1'h0	
		1	VCS	R/O	1'h0	Vcc supply voltage status 0: above threshold 1: below threshold. Bus only can read. Logic can write
		0	CFS	R/O	1'h0	CAN failures tatus 0: no TXD dominant timeout event detected 1: CAN transmitter disabled due the event. bus only can read. Logic can write
TRANSCEIVER_EVENT_ENABLE	0x23	7:5	Reserved	Null	3'h0	
		4	CBSE	R/W	1'h0	CAN bus silence enable 0: disable 1: enable
		3:2	Reserved	Null	2'h0	
		1	CFE	R/W	1'h0	CAN failure enable 0: disable 1: enable
		0	CWE	RWS	1'h0	CAN wake-up enable 0: disable 1: enable
DATA_RATE	0x26	7:3	Reserved	Null	5'h0	
		2:0	CDR	R/W	3'h5	CAN data rate 000: 50 kbit/s 001: 100 kbit/s 010: 125 kbit/s 011: 250 kbit/s 100: reserved 101: 500 kbit/s 110: reserved 111: 1000 kbit/s
ID_07_00	0x27	7:0	ID_07_00	R/W	8'h0	CAN frame ID bit 7:0 for patrial frame networking wake up

Register name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit description
ID_15_08	0x28	7:0	ID_15_08	R/W	8'h0	CAN frame ID bit 15:8 for partial frame networking wake up
ID_23_16	0x29	7:0	ID_23_16	R/W	8'h0	CAN frame ID bit 23:16 for partial frame networking wake up
ID_28_24	0x2a	7:5	Reserved	Null	2'h0	
		4:0	ID_28_24	R/W	5'h0	CAN frame ID bit 28:24 for partial frame networking wake up
M_07_00	0x2b	7:0	M_07_00	R/W	8'h0	CAN frame ID mask bit 7:0 for partial frame networking wake up
M_15_08	0x2c	7:0	M_15_08	R/W	8'h0	CAN frame ID mask bit 15:8 for partial frame networking wake up
M_23_16	0x2d	7:0	M_23_16	R/W	8'h0	CAN frame ID mask bit 23:16 for partial frame networking wake up
M_28_24	0x2e	7:5	Reserved	Null	2'h0	
		4:0	M_28_24	R/W	8'h0	CAN frame ID mask bit 28:24 for partial frame networking wake up
FRAME_CONTROL	0x2f	7	IDE	R/W	1'h0	identifier format 0: standard 1: extended
		6	PNDM	R/W	1'h1	PN data mask 0: data length and field are "don't care" 1: check data length and field
		5:4	Reserved	Null	2'h0	
		3:0	DLC	R/W	4'h0	data payload length in frame 0: data payload length is 0 1: data payload length is 1 2: data payload length is 2 3: data payload length is 3 4: data payload length is 4 5: data payload length is 5 6: data payload length is 6

Register name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit description
						7: data payload length is 7 others: data payload length is 8
WAKE_PIN_STATUS	0x4b	7:2	Reserved	Null	6'h0	
		1	WPVS	R/O	1'h0	wake pin status 0: below switching threshold 1: above switching threshold
		0	Reserved	Null	1'h0	
WAKE_PIN_ENABLE	0x4c	7:2	Reserved	Null	6'h0	
		1	WPRE	RWS	1'h0	wake pin rising edge enable 0: disable 1: enable
		0	WPFE	RWS	1'h0	wake pin falling edge enable 0: disable 1: enable
DM_SEQ_SEL	0x55	7	Reserved	Null	1'h0	
		6	DM_SEQ_SEL	R/W	1'h1	1: Data Mask sequence 1 0: Data Mask sequence 0 Refer to description below for detail
		5:9	Reserved	Null	6'h06	
EVENT_CAPTURE_STATUS	0x60	7:4	Reserved	Null	4'h0	
		3	WPE	R/O	1'h0	wake pin event 0:no pending wake pin event 1: wake pin event pending
		2	TRXE	R/O	1'h0	transceiver event 0: no pending transceiver event 1: transceiver event pending
		1	Reserved	Null	1'h0	
		0	SYSE	R/O	1'h1	system event 0:no pending system event

Register name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit description
						1: system event pending
SYSTEM_EVENT_STATUS	0x61	7:5	Reserved	Null	3'h0	
		4	PO	CRW	1'h1	power-on 0:no power-on 1: left off mode after power-on
		3	Reserved	Null	1'h0	
		2	OTW	CRW	1'h0	overtemperature warning 0: overtemperature not detected 1: exceed overtemperature warning threshold
		1	SPIF	CRW	1'h0	SPI failure 0: no SPI failure detected 1: SPI failure detected
		0	Reserved	Null	1'h0	
TRANSCEIVER_EVENT_STATUS	0x63	7:6	Reserved	Null	2'h0	
		5	PNFDE	CRW	1'h0	PN frame detection err 0:no err 1:err
		4	CBS	CRW	1'h0	CAN bus status 0:CAN bus active 1:no activity
		3:2	Reserved	Null	2'h0	
		1	CF	CRW	1'h0	CAN failure 0:no CAN failure detected 1: CAN failure event detected
		0	CW	CRW	1'h0	CAN wake up 0:no CAN wake-up event detected 1: CAN wake-up event detected
WAKE_PIN_EVENT_STATUS	0x64	7:2	Reserved	Null	6'h0	
		1	WPR	CRW	1'h0	wake pin rising edge 0:no rising edge 1: rising edge

Register name	Offset	Bit Width	Bit Name	Bit Type	Default Value	Bit description
		0	WPF	CRW	1'h0	wake pin falling edge 0:no falling edge 1: falling edge
DM0	0x68	7:0	DM0	R/W	8'hFF	match byte 0
DM1	0x69	7:0	DM1	R/W	8'hFF	match byte 1
DM2	0x6a	7:0	DM2	R/W	8'hFF	match byte 2
DM3	0x6b	7:0	DM3	R/W	8'hFF	match byte 3
DM4	0x6c	7:0	DM4	R/W	8'hFF	match byte 4
DM5	0x6d	7:0	DM5	R/W	8'hFF	match byte 5
DM6	0x6e	7:0	DM6	R/W	8'hFF	match byte 6
DM7	0x6f	7:0	DM7	R/W	8'hFF	match byte 7
ID_0	0x7e	7:0	ID_0	R/O	8'h04	chip id-1004
ID_1	0x7f	7:0	ID_1	R/O	8'h10	chip id-1004

(1) Recommend to add at least 50-μs delay after writing to ensure the mode transition is finished and read the right register value.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT1145x device is a CAN transceiver to support CAN FD function up to 5 Mbps, with BUS protection voltage from –70 V to +70 V, overtemperature shutdown, a −30 V to +30 V common-mode range. The VIO of TPT1145x can support the voltage level of TXD and RXD from 3.3 V to 5.0 V, and V_{BAT} is from battery power supply.

The following sections show a typical application of the TPT1145x.

Typical Application

shows the typical application schematic of the TPT1145x.

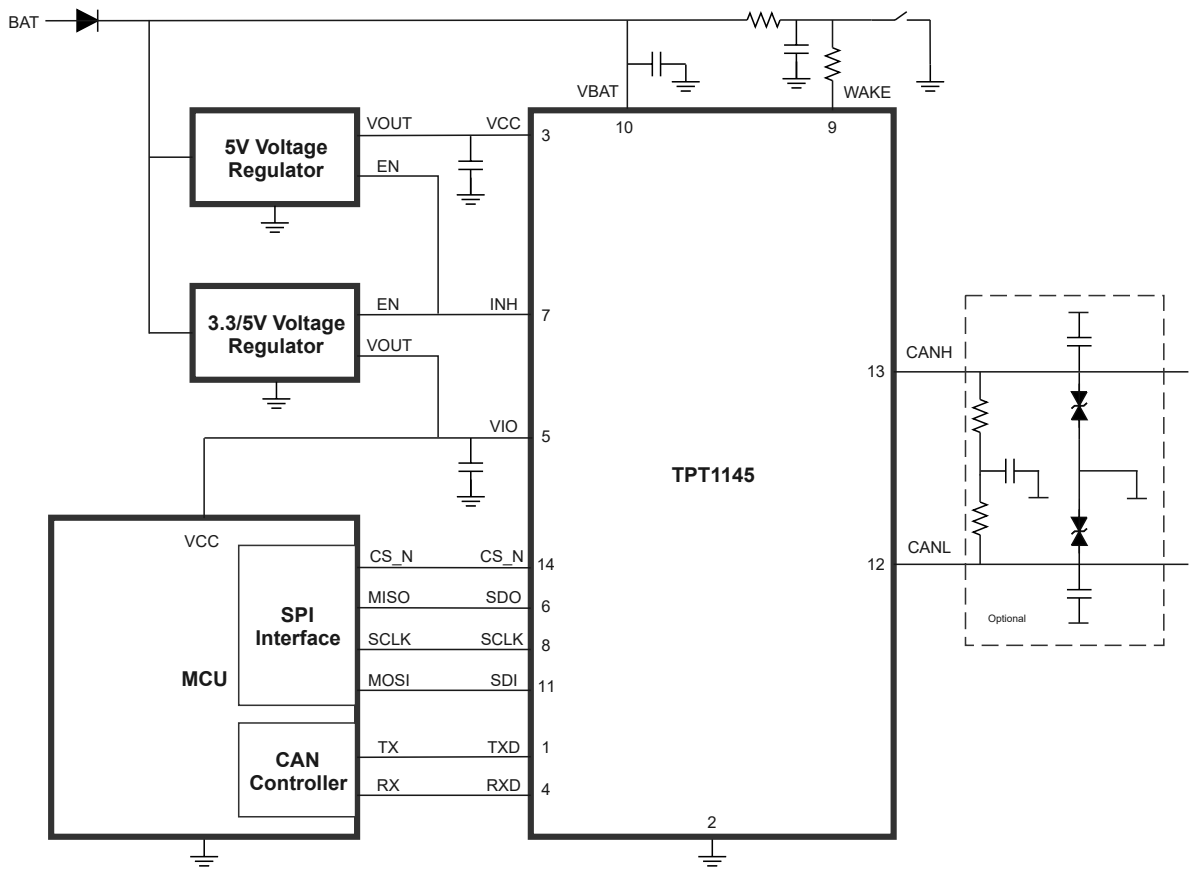
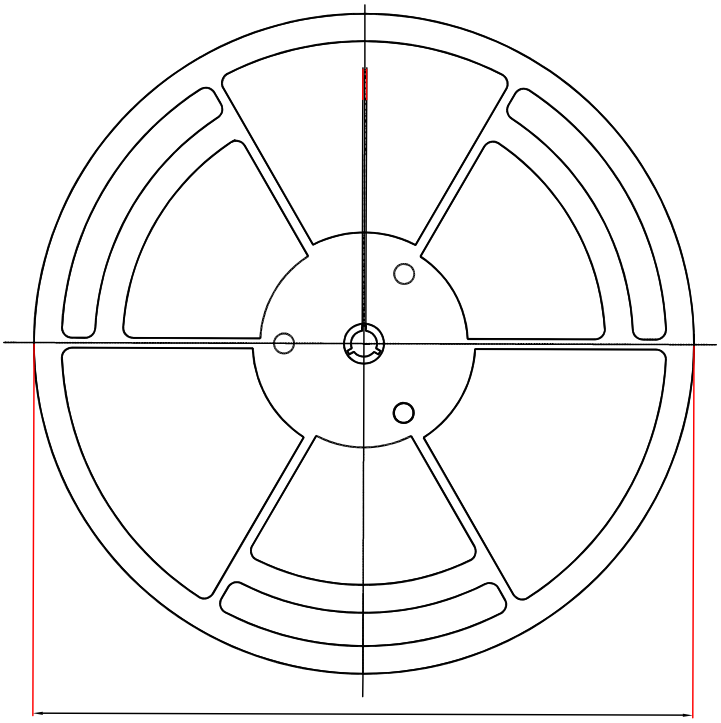
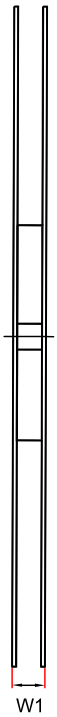
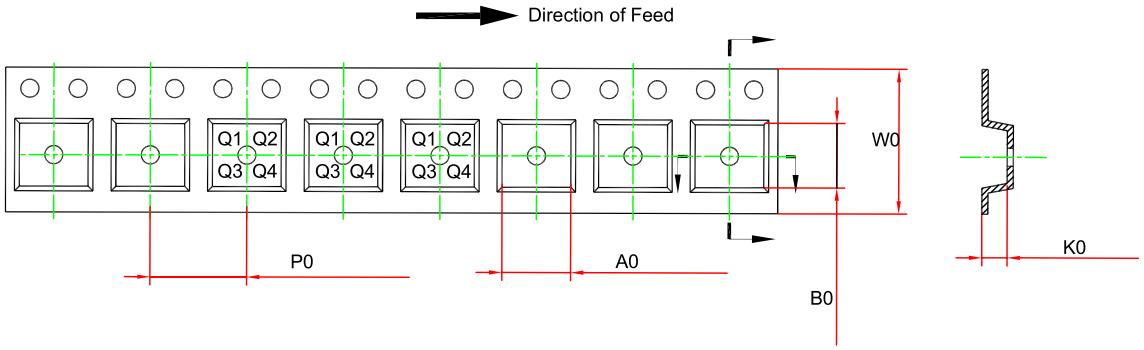


Figure 10. Typical Application Circuit

Tape and Reel Information





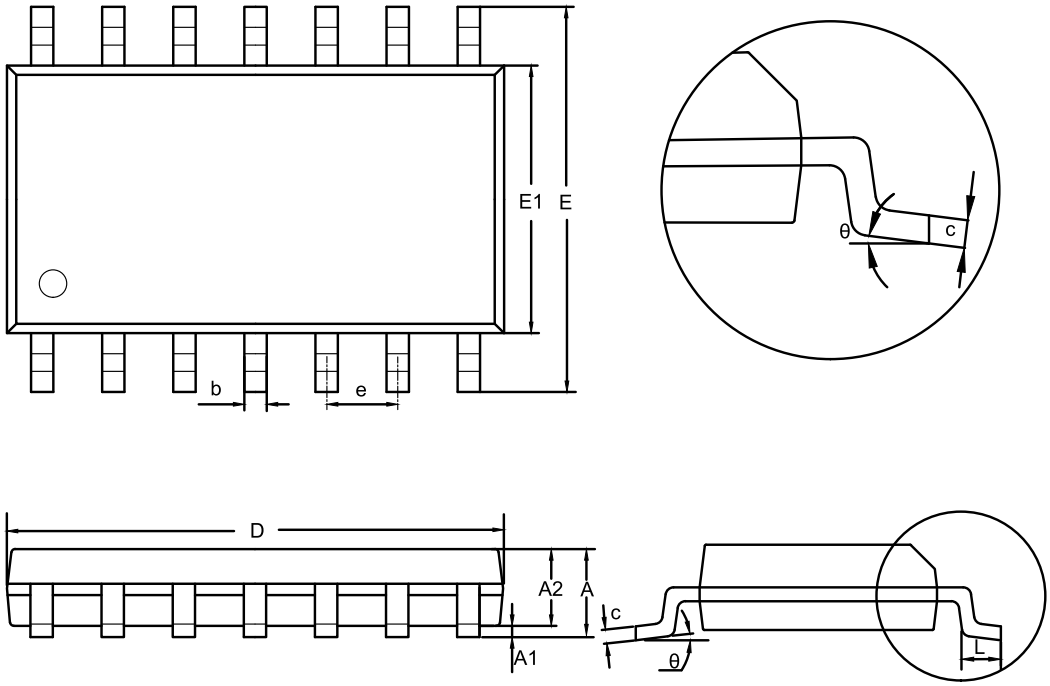


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT1145Q-SO2R-S	SOP14	330	21.6	6.5	9.0	2.1	8.0	16.0	Q1
TPT1145Q-DFKR-S	DFN3X3-14L	330	16.8	3.3	4.8	1.15	8.0	12.0	Q1
TPT1145NQ-SO2R-S	SOP14	330	21.6	6.5	9.0	2.1	8.0	16.0	Q1
TPT1145NQ-DFKR-S	DFN3X3-14L	330	16.8	3.3	4.8	1.15	8.0	12.0	Q1

Package Outline Dimensions

SOP14

Package Outline Dimensions SO2(SOP-14-A)



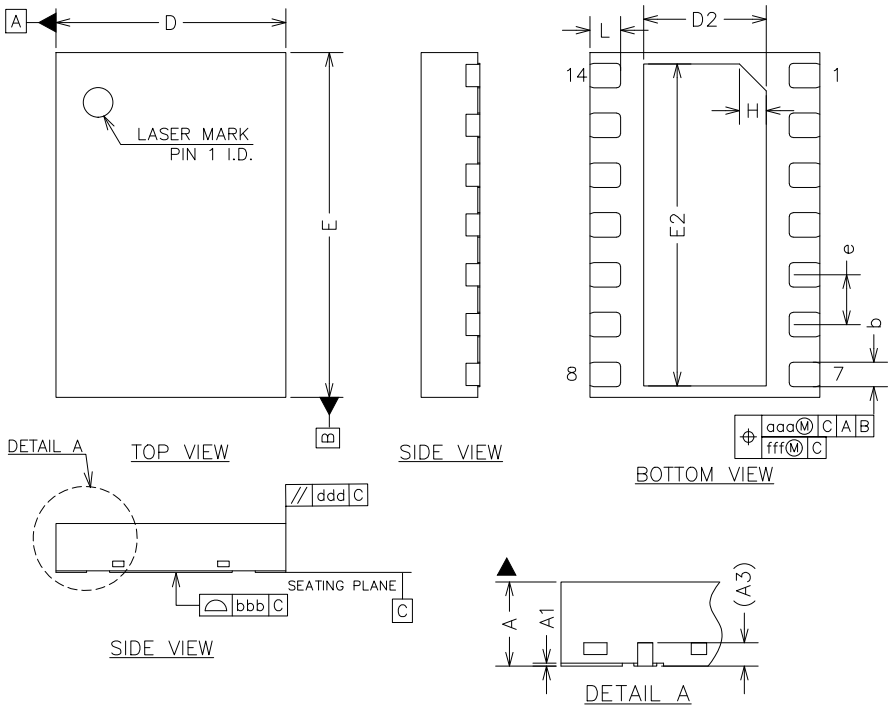
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN4.5X3-14

Package Outline Dimensions DFK(DFN4.5X3-14-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
b	0.270	0.370	0.011	0.015
A3	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
E	4.400	4.600	0.173	0.181
e	0.650 BSC		0.026 BSC	
H	0.350 REF		0.014 REF	
L	0.300	0.500	0.012	0.020
D2	1.500	1.700	0.059	0.067
E2	4.100	4.300	0.161	0.169

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT1145Q-SO2R-S	−40 to 125°C	SOP14	T1145Q	MSL1	Tape and Reel, 2500	Green
TPT1145Q-DFKR-S	−40 to 125°C	DFN4.5X3-14	1145Q	MSL1	Tape and Reel, 4000	Green
TPT1145NQ-SO2R-S	−40 to 125°C	SOP14	T45NQ	MSL1	Tape and Reel, 2500	Green
TPT1145NQ-DFKR-S	−40 to 125°C	DFN4.5X3-14	T45NQ	MSL1	Tape and Reel, 4000	Green

(1) MSL will be updated depending on qualification report.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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