

Features

- Input Voltage Range: 2.4 V to 5.5 V
- Output Voltage Options:
 - Fixed Voltage: 1.2 V, 1.8 V, 2.5 V, 2.8 V, 3 V, 3.3 V
 - Adjustable Voltage: 0.8 V to 5 V
- High Output Accuracy:
 - $\pm 1\%$ Typical Under Room Temperature
 - $\pm 2\%$ Through Operating Conditions
- Maximum Output Current: 500 mA
- Low Dropout Voltage: 400 mV at 500 mA
- Low Quiescent Current and Shutdown Current
- Foldback Current Limit and Thermal Protection
- Stable with 2.2- μ F Ceramic Capacitor
- Inrush Input Current Limitation During Start-up
- Thermal Shutdown Protection
- Junction Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Package Options: SOT23-5, SOT89-3, DFN1 \times 1-4

Applications

- Handheld Devices with Battery Power Supply
- POS
- Video Surveillance
- Wireless and IoT modules

Description

The TPL740 is a series of high-performance and low-dropout linear regulators. The TPL740 series supports a maximum 500-mA output current with low-quiescent current and high PSRR. The TPL740 series is stable with ceramic output capacitors from 2.2 μF to 10 μF .

The TPL740 series has a high PSRR with 60 dB at 1 kHz. This feature makes the TPL740 series very suitable for power-sensitive applications with high noise from the previous stage power supply. A quiescent current of as low as 49 μA and only 20-nA shutdown current make the TPL740 series ideal for portable devices with battery power supplies. The current limit foldback and thermal overload protection circuits improves the reliability under heavy load conditions.

The TPL740 series provides several output voltage options including the fixed and adjustable versions with $\pm 2\%$ output voltage accuracy over operating conditions. The TPL740 series is guaranteed over the junction temperature range from -40°C to $+125^{\circ}\text{C}$.

Typical Application Circuit

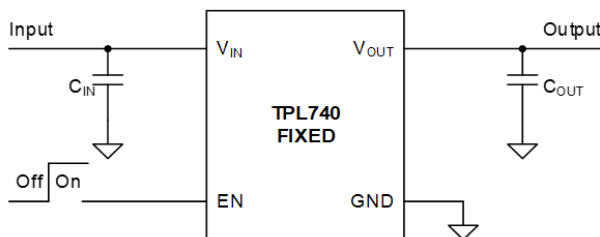


Figure 1. TPL740 Fixed Output Voltage

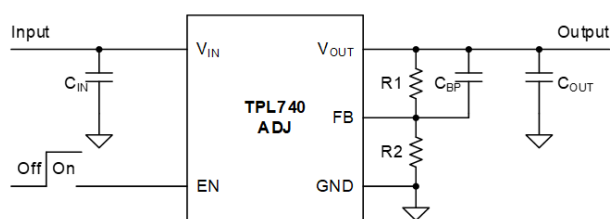


Figure 2. TPL740 Adjustable Output Voltage

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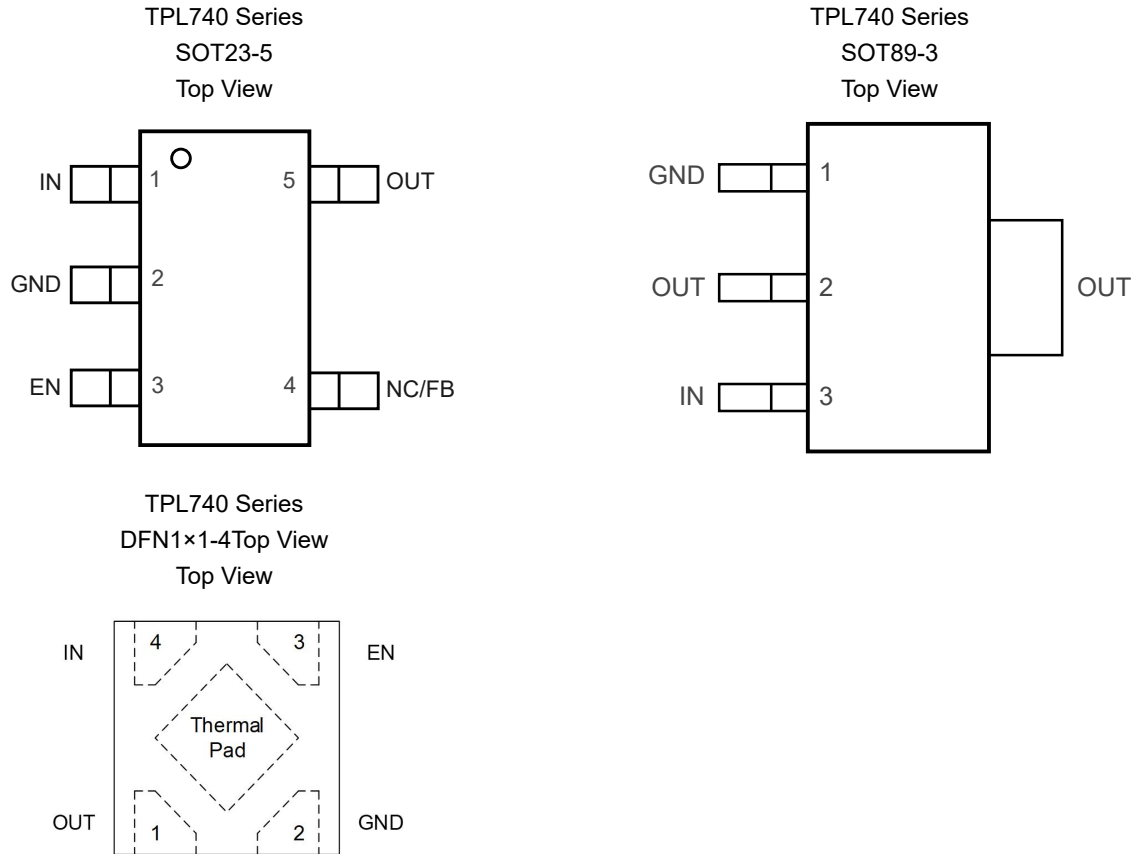
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Product Family Table

Order Number	Output Voltage (V)	Package
TPL740ADJ-5TR	Adjustable (0.8 V ~ 5 V)	SOT23-5
TPL740F12-5TR	Fixed 1.2 V	SOT23-5
TPL740F18-5TR	Fixed 1.8 V	SOT23-5
TPL740F25-5TR	Fixed 2.5 V	SOT23-5
TPL740F28-5TR	Fixed 2.8 V	SOT23-5
TPL740F30-5TR	Fixed 3.0 V	SOT23-5
TPL740F33-5TR	Fixed 3.3 V	SOT23-5
TPL740F33-89TR	Fixed 3.3 V	SOT89-3
TPL740F33-FR	Fixed 3.3 V	DFN1×1-4

Revision History

Date	Revision	Notes
2018-08-28	Rev.Pre.0	Preliminary version.
2018-11-26	Rev.A.0	Initial released version.
2019-02-11	Rev.A.1	1. Added voltage options of 1.5 V, 2.7 V, and 2.9 V. 2. Added the link to Figure 11 and Figure 12.
2019-08-08	Rev.A.2	Added the max limit of the item: I _{GND} , I _{SHDN} , UVLO, Load regulation, and V _{DO} .
2020-08-15	Rev.A.3	1. Changed the “Soft-start Limits Input Current Surge During Enable” to “Inrush Input Current Limitation During Start-up”. 2. Added the description of “Short-Circuit Protection”.
2021-03-09	Rev.A.4	1. Corrected the typical value of the current limit in the Feature Description. 2. Added Tape and Reel Information. 3. Updated Junction Temperature Range.
2022-05-15	Rev.A.5	Added Tape and Reel Information of the SC70-5 and DFN1×1-4 package.
2024-10-25	Rev.A.6	1. Updated to a new datasheet format. 2. Removed voltage options of 1.5 V, 2.7 V, and 2.9 V. 3. Removed voltage options of SC70-5 package. 4. Updated recommended C _{BP} range for adjustable output version.

Pin Configuration and Functions

Table 1. Pin Functions

Pin No.			Name	I/O	Description
SOT23-5	SOT89-3	DFN1x1-4			
1	3	4	IN	I	The input voltage pin. Bypass IN to GND with a 1- μ F or greater capacitor.
5	2	1	OUT	O	The regulated output voltage pin. Bypass OUT to GND with a 2.2- μ F or greater capacitor.
3	-	3	EN	I	The regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For the automatic startup, connect EN to IN directly.
2	1	2	GND	-	The ground reference pin. Connect the GND pin to the PCB ground plane directly.
4	-	-	NC	-	Not connected.
4	-	-	FB	I	The output feedback pin (adjustable version only). Connect to a resistor divider to adjust the output voltage. And connect CBP with capacitance from 1 nF to 200 nF between FB and OUT.

(1) The thermal pad must be connected to the PCB ground plane to maximize the thermal performance.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
V _{IN} , V _{EN}	Input Voltage	-0.3	6	V
V _{OUT}	Output Voltage	-0.3	6	V
V _{FB}	Feedback Voltage (Adjustable Version only)	-0.3	6	V
T _J	Maximum Junction Temperature	-40	150	°C
T _{STG}	Storage Temperature Range	-65	150	°C
T _L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V _{IN}	Input Voltage	2.4	5.5	V
V _{EN}	Enable Voltage	0	V _{IN}	V
V _{OUT}	Output Voltage	0	5	V
V _{FB}	Feedback Voltage (Adjustable Version Only)	0	V _{OUT}	V
I _{OUT}	Output Current	0	500	mA
C _{OUT}	Output Capacitor	2.2	10	μF
C _{BP}	Bypass Capacitor	1	200	nF
T _J	Operating Junction Temperature Range	-40	125	°C

Thermal Information

Package Type	θ _{JA}	θ _{JC}	Unit
SOT23-5	280	62	°C/W
SOT89-3	55	88	°C/W

500-mA Output, High PSRR, Low-Dropout Linear Regulator

Package Type	θ_{JA}	θ_{JC}	Unit
DFN1×1-4	210	110	°C/W

Electrical Characteristics

 All test conditions: $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 2.4 V , whichever is greater; $C_{OUT} = 2.2\text{ }\mu\text{F}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
V_{IN}	Input Voltage Range		2.4		5.5	V
I_{GND}	Ground Pin Current	$I_{OUT} = 0\text{ mA}$		49	200	μA
		$I_{OUT} = 100\text{ mA}$		200	2000	μA
I_{SHDN}	Shutdown Current	EN = GND		0.02	2	nA
UVLO	V_{IN} Under-Voltage Lock-out	V_{IN} Rising	1.5	1.9	2.4	V
		Hysteresis		200		mV
Enable Input Voltage and Current						
$V_{IH(EN)}$	EN Logic-Input High Level (Enable)		1.2		V_{IN}	V
$V_{IL(EN)}$	EN Logic-Input Low Level (Disable)		0		0.4	V
I_{EN}	EN Pin Leakage Current	EN = 5 V		1	3	μA
Regulated Output Voltage and Current						
V_{OUT}	Output Voltage Accuracy	$T_J = +25^\circ\text{C}$		1%		
		$-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	-2%		2%	
V_{FB}	Feedback Pin Voltage	ADJ Version Only	0.784	0.8	0.816	V
ΔV_{OUT}	Line Regulation	$V_{IN} = 2.4\text{ V}$ or $V_{OUT(NOM)} + 0.5\text{ V}$ to 5.5 V , or $V_{IN} \geq 2.4\text{ V}$, $I_{OUT} = 1\text{ mA}$		1	5	mV
	Load Regulation	$I_{OUT} = 1\text{ mA}$ to 500 mA		20	60	mV
$V_{DO}^{(1)}$	Dropout Voltage	$V_{IN} = 0.98 \times V_{OUT(NOM)}$, $I_{OUT} = 100\text{ mA}$		75	100	mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$, $I_{OUT} = 300\text{ mA}$		200	250	mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$, $I_{OUT} = 500\text{ mA}$		300	400	mV
I_{OUT}	Output Current	V_{OUT} in Regulation	0		500	mA
I_{CL}	Output Current Limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	550	1000	1400	mA
Regulated Output Voltage and Current						
PSRR	Power Supply Rejection Ratio (Fixed Version)	$I_{OUT} = 100\text{ mA}$, $f = 1\text{ kHz}$		60		dB
		$I_{OUT} = 100\text{ mA}$, $f = 100\text{ kHz}$		40		dB
		$I_{OUT} = 100\text{ mA}$, $f = 1\text{ MHz}$		40		dB
	Power Supply Rejection Ratio (ADJ Version)	$I_{OUT} = 100\text{ mA}$, $f = 1\text{ kHz}$, $C_{BP} = 100\text{ nF}$		65		dB
		$I_{OUT} = 100\text{ mA}$, $f = 100\text{ kHz}$, $C_{BP} = 100\text{ nF}$		60		dB

500-mA Output, High PSRR, Low-Dropout Linear Regulator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PSRR	Power Supply Rejection Ratio (ADJ Version)	$I_{OUT} = 100\text{ mA}$, $f = 1\text{ MHz}$, $C_{BP} = 100\text{ nF}$		45		dB
V_N	Output Noise Voltage (Fixed Version)	$I_{OUT} = 100\text{ mA}$, $BW = 100\text{ Hz to }80\text{ kHz}$		130		μV_{RMS}
	Output Noise Voltage (ADJ Version)	$I_{OUT} = 100\text{ mA}$, $BW = 100\text{ Hz to }80\text{ kHz}$, $C_{BP} = 100\text{ nF}$		40		μV_{RMS}
$T_{STR}^{(2)}$	Start-up Time (Fixed Version)	$I_{OUT} = 500\text{ mA}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$		150		μs
	Start-up Time (ADJ Version)	$I_{OUT} = 500\text{ mA}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{BP} = 100\text{ nF}$		15		ms
Temperature Range						
T_{SD}	Thermal Shutdown Temperature			170		$^{\circ}\text{C}$
	Thermal Shutdown Hysteresis			30		$^{\circ}\text{C}$

(1) Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to $V_{IN} - V_{DROPOUT}$.

(2) The start-up time from EN assertion to $0.98 \times V_{OUT(NOM)}$.

Typical Performance Characteristics

All test conditions: $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$ or 2.4 V , whichever is greater; $C_{OUT} = 2.2\text{ }\mu\text{F}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

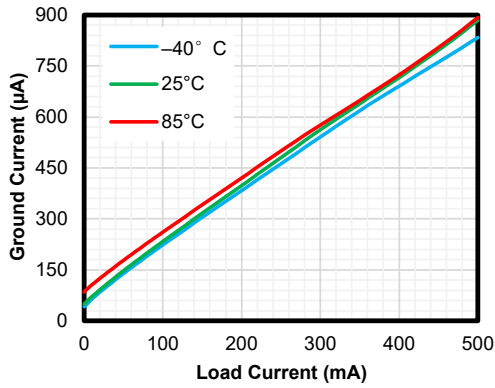


Figure 3. Quiescent Current vs. Output Current

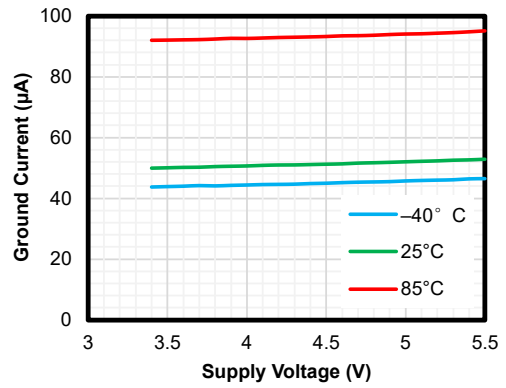


Figure 4. Quiescent Current vs. Input Voltage

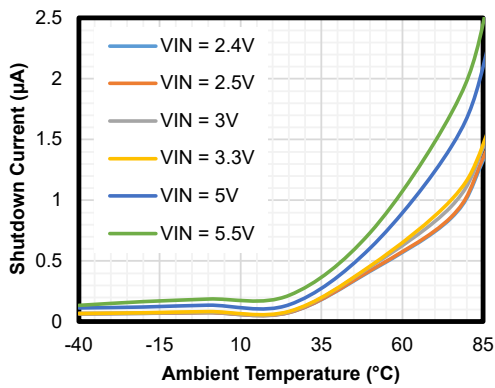


Figure 5. Shutdown Current vs. Ambient Temperature

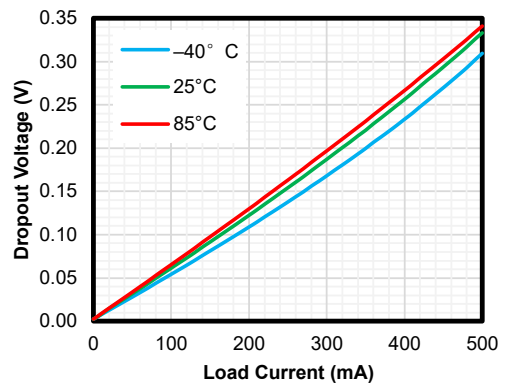


Figure 6. Dropout Voltage vs. Output Current

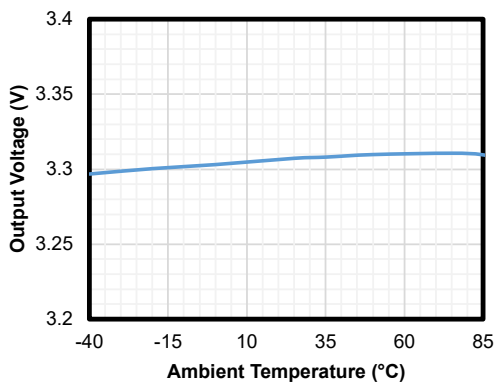


Figure 7. Output Accuracy vs. Ambient Temperature

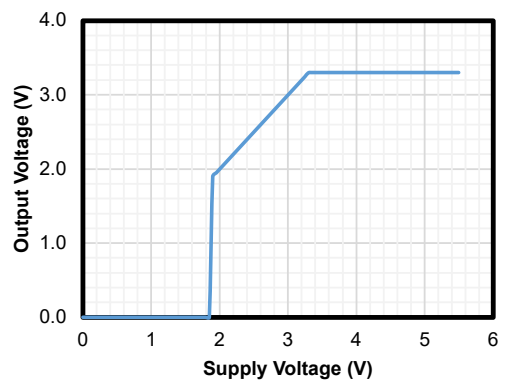


Figure 8. Output Voltage vs. Supply Voltage

500-mA Output, High PSRR, Low-Dropout Linear Regulator

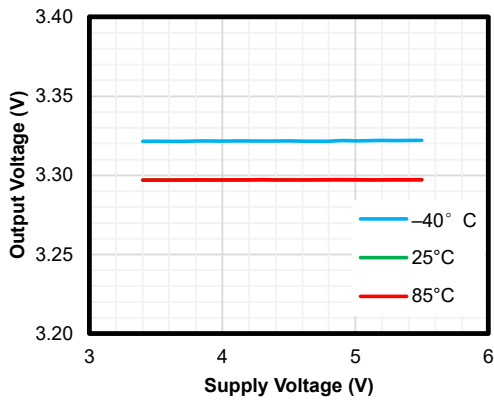


Figure 9. Line Regulation

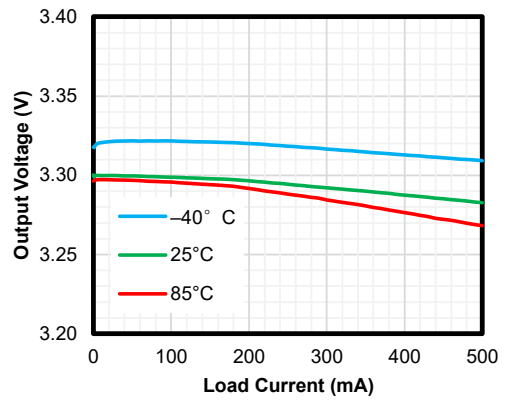


Figure 10. Load Regulation

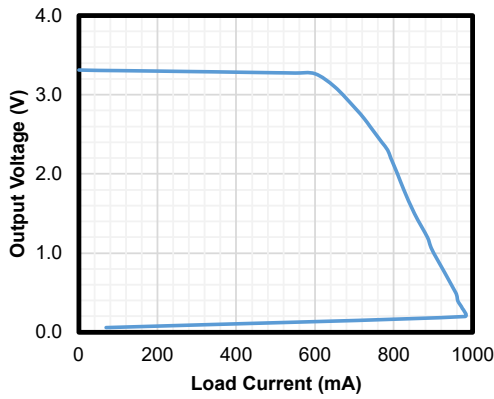


Figure 11. Foldback Current Limit

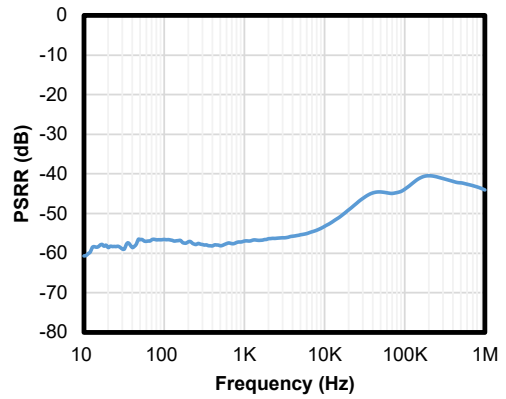


Figure 12. PSRR

Detailed Description

Overview

The TPL740 is a series of 500-mA high PSRR, low-dropout linear regulators with a very low quiescent current. It operates from 2.4 V to 5.5 V and consumes a quiescent current of 49 μA at no load and only 20 nA in shutdown mode.

The TPL740 series is available in fixed voltage versions of 1.2 V, 1.8 V, 2.5 V, 2.8 V, 3 V, and 3.3 V, and adjustable voltage versions of 0.8 V to 5 V with $\pm 2\%$ output voltage accuracy over operating conditions.

Functional Block Diagram

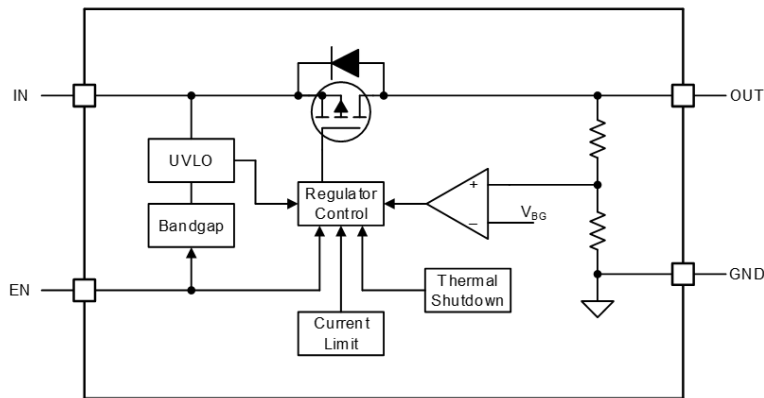


Figure 13. TPL740 Series Fixed Output Version

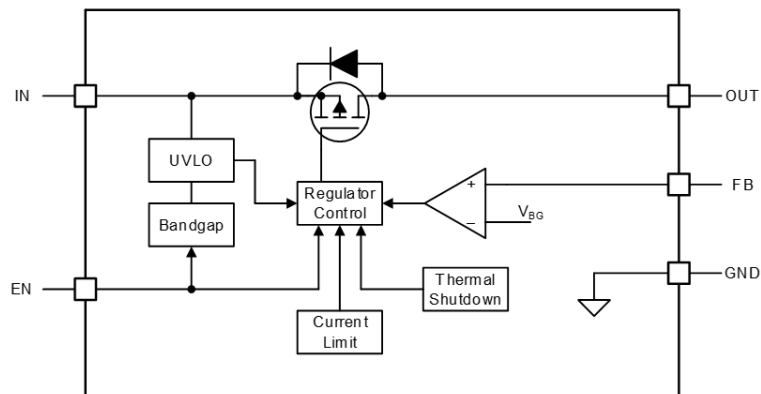


Figure 14. TPL740 Series Adjustable Output Version

Feature Description

Enable

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

500-mA Output, High PSRR, Low-Dropout Linear Regulator

Under-Voltage Lockout (UVLO)

The TPL740 series uses an under-voltage lockout circuit (UVLO = 1.9 V) to keep the output shut off until the internal circuitry operates properly.

Regulated Output Voltage

The TPL740 series is available in fixed voltage versions of 1.2 V, 1.8 V, 2.5 V, 2.8 V, 3 V, and 3.3 V. When the input voltage is higher than $V_{OUT(NOM)} + V_{DO}$ or 2.4 V, the output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT(NOM)} + V_{DO}$ or 2.4 V, the output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below the UVLO threshold, the output keeps shut off.

Adjustable Output Voltage

The TPL740 series is also available in adjustable voltage versions of 0.8 V to 5 V by selecting suitable external resistor dividers. Use [Equation 1](#) to calculate the output voltage ($V_{FB} = 0.8$ V). Suggest selecting the resistor value of (R1 + R2) between 10 k Ω and 100 k Ω .

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Current Limit

The TPL740 series integrates an internal foldback current limit that helps to protect the regulator during fault conditions. When the output is shorted, the LDO supplies a typical current of 1000 mA. The output voltage is not regulated when the device is in current limit and is $V_{OUT} = I_{CL} \times R_{LOAD}$.

Short-Circuit Protection

The TPL740 series integrates the short-circuit protection. When the output pin is shorted to ground or forced to a voltage below 0.2 V, the output current of the TPL740 series is limited to a typical value of 150 mA.

Thermal Shutdown

During normal operation, the LDO junction temperature should not exceed 125°C. When the junction temperature exceeds the thermal shutdown threshold, the LDO shuts down the output immediately. When the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the output turns on again.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL740 is a series of 500-mA high PSRR, low-dropout linear regulators with a low quiescent current. The following application schematic shows a typical usage of the TPL740 series.

Typical Application

Figure 15 and Figure 16 show the typical application schematic of the TPL740 series.

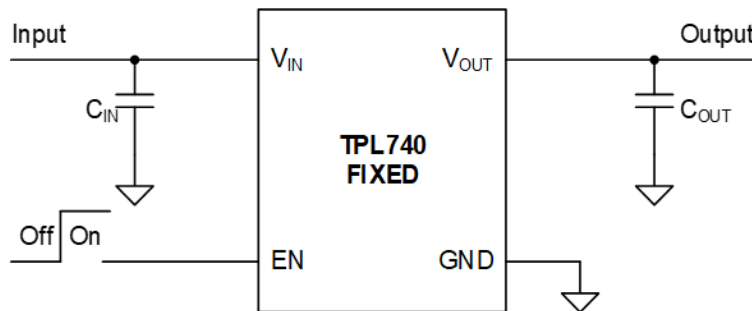


Figure 15. TPL740 Fixed Output Voltage

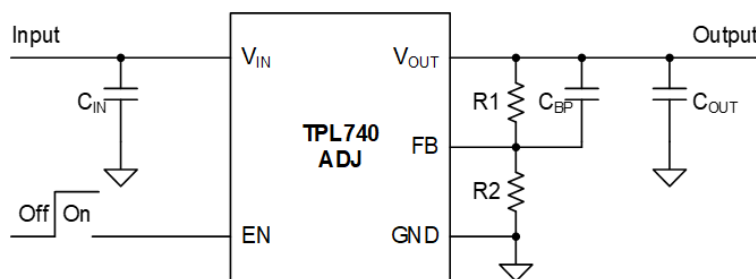


Figure 16. TPL740 Adjustable Output Voltage

Input Capacitor and Output Capacitor

3PEAK recommends adding a 1- μF or greater capacitor with a 0.1- μF bypass capacitor in parallel at the IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL740 series requires an output capacitor with a minimum effective capacitance value of 2.2 μF . 3PEAK recommends selecting an X5R- or X7R-type ceramic capacitor with low ESR over temperature.

The TPL740 adjustable output version requires a bypass capacitor C_{BP} with a capacitance value from 1 nF to 200 nF to ensure loop stability.

500-mA Output, High PSRR, Low-Dropout Linear Regulator

Both input capacitors and output capacitors must be placed as close to the pins of the device as possible.

Power Dissipation

During normal operation, the LDO junction temperature should not exceed 125°C. Use the below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using [Equation 2](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (2)$$

The junction temperature can be estimated using [Equation 3](#). θ_{JA} is the junction-to-ambient thermal resistance (See [Thermal Information](#)).

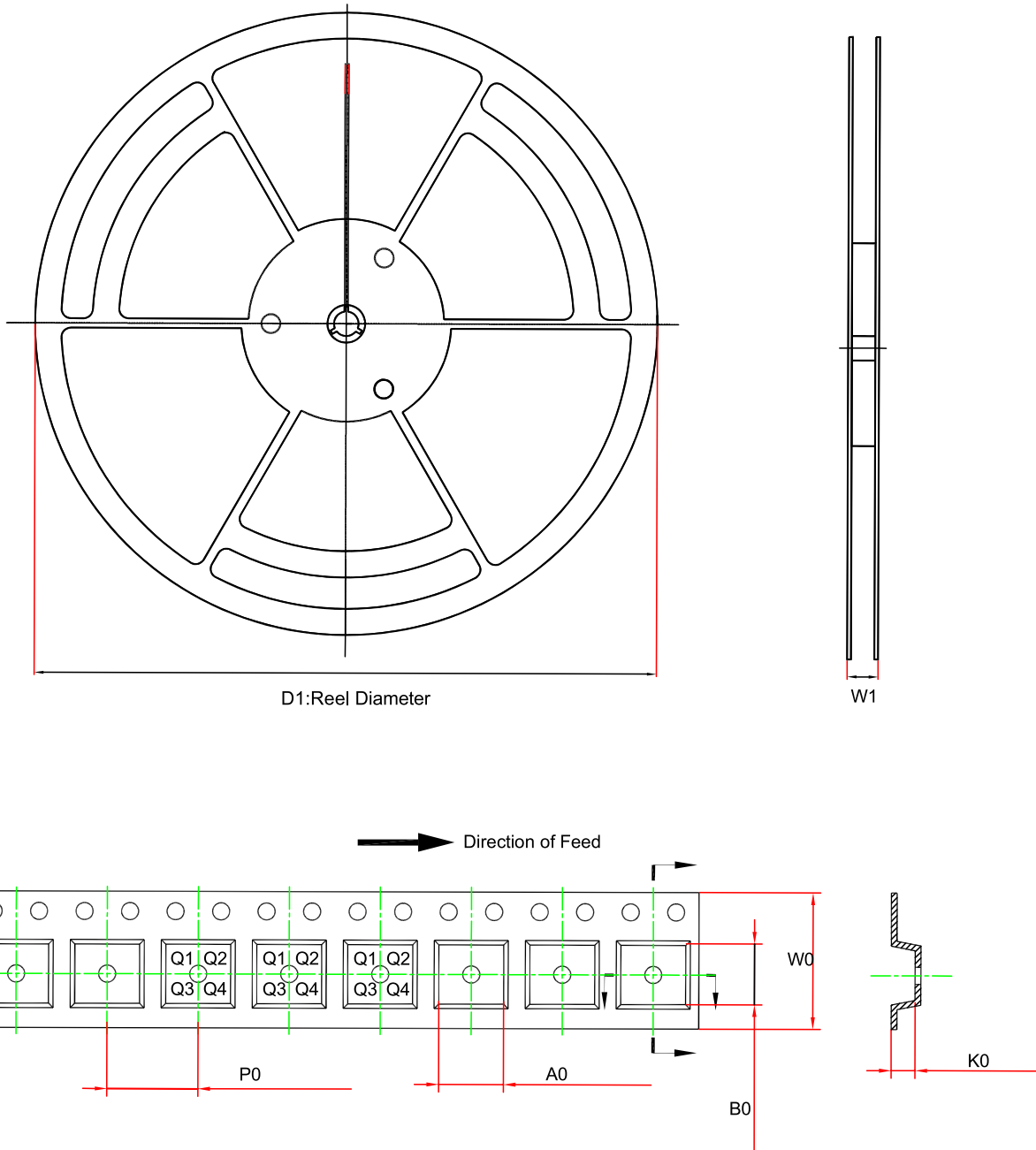
$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

Layout

Layout Guideline

- Both input capacitors and output capacitors must be placed as close to the pins of the device as possible.
- It is recommended to bypass the input pin to ground with a 0.1- μ F bypass capacitor. The loop area formed by the bypass capacitor connection, the IN pin, and the GND pin of the system must be as small as possible.
- It is recommended to use wide trace lengths or thick copper weight to minimize $I \times R$ drop and heat dissipation.

Tape and Reel Information

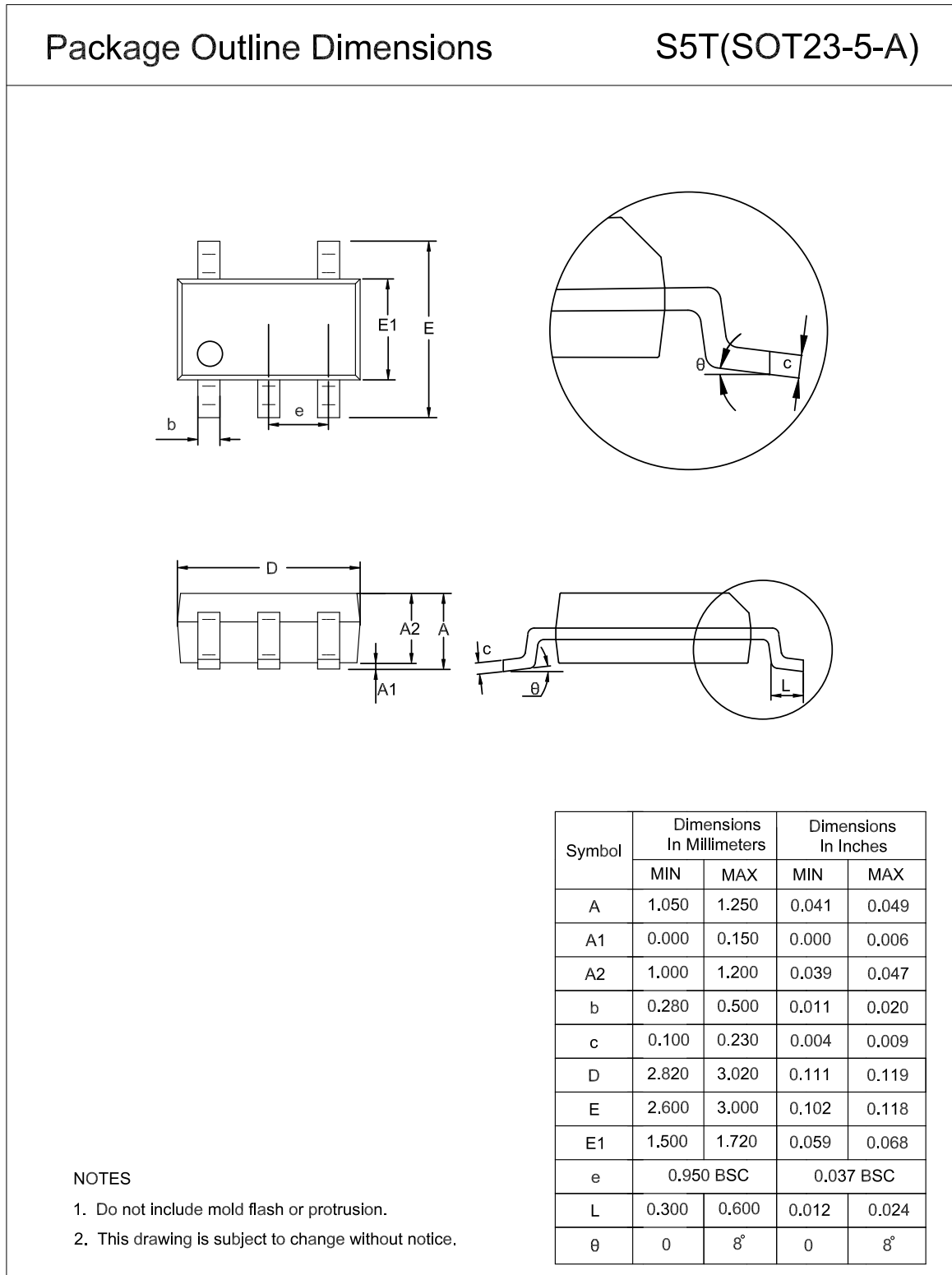


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL740ADJ-5 TR	SOT23-5	180.0	13.1	3.2	3.2	1.4	4.0	8.0	Q3
TPL740Fxx-5TR	SOT23-5	180.0	13.1	3.2	3.2	1.4	4.0	8.0	Q3
TPL740F33-89 TR	SOT89-3	330	17.6	4.8	4.4	1.8	8.0	12.0	Q3

500-mA Output, High PSRR, Low-Dropout Linear Regulator

Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPL740F33- FR	DFN1×1-4	180.0	10.0	1.16	1.16	0.5	2.0	8.0	Q1

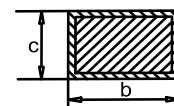
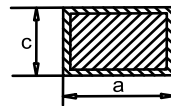
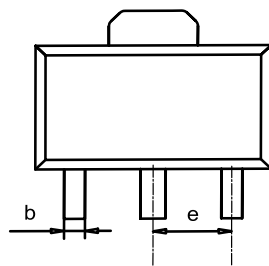
(1) The output voltage value, xx = 12 to 33, e.g., 33 means 3.3-V output voltage.

Package Outline Dimensions
SOT23-5


SOT89-3

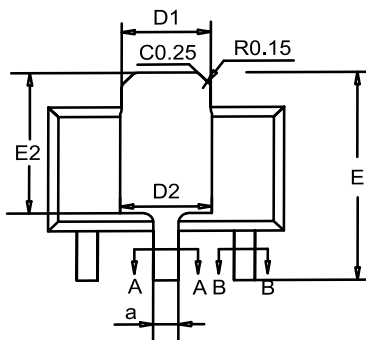
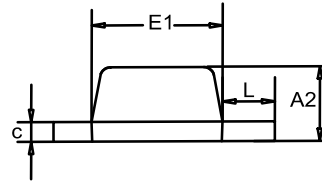
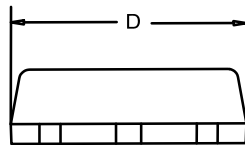
Package Outline Dimensions

89T(SOT89-3-A)



SECTION A-A

SECTION B-B

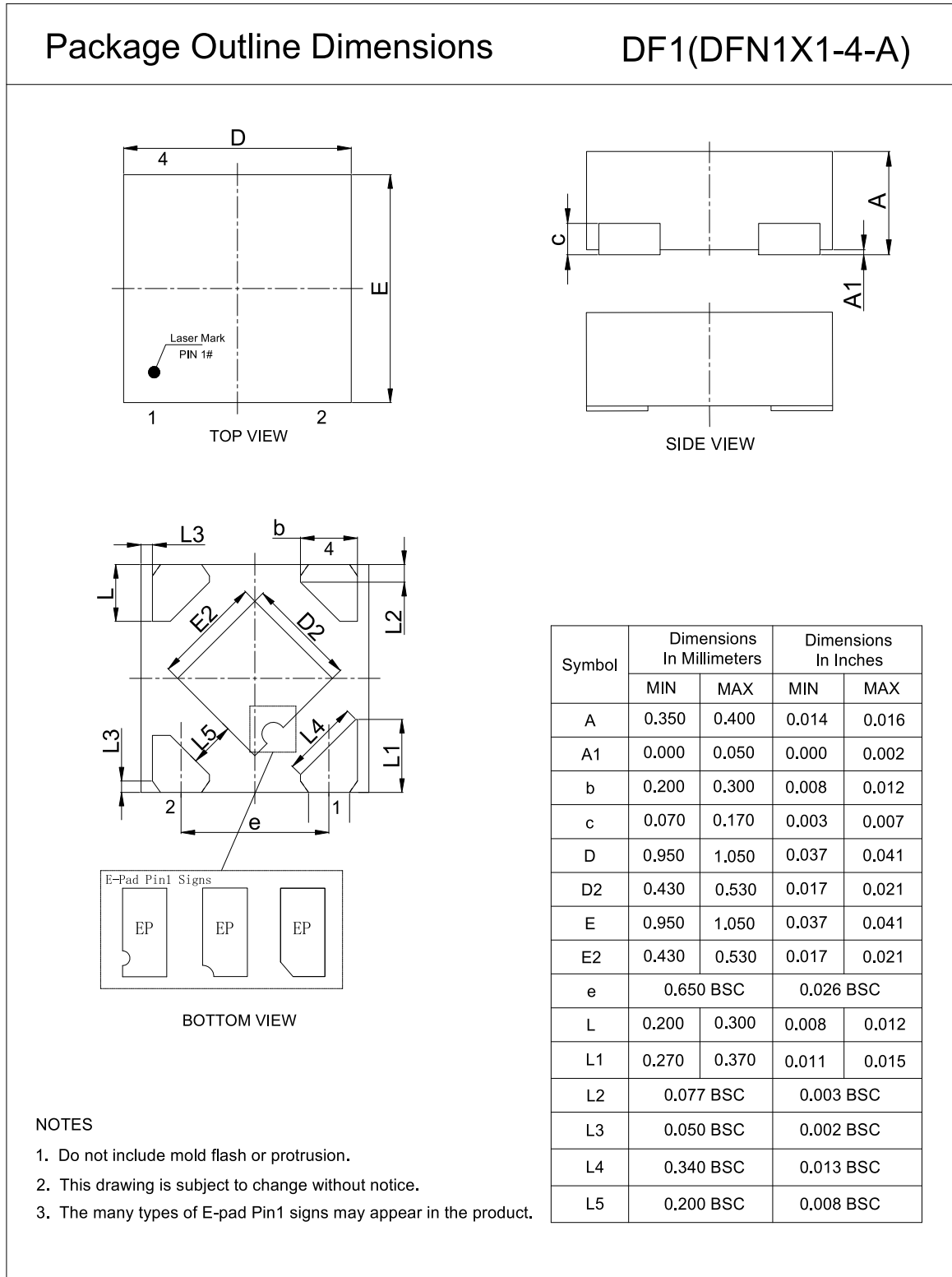


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A2	1.400	1.600	0.055	0.063
a	0.460	0.560	0.018	0.022
b	0.380	0.470	0.015	0.019
c	0.380	0.440	0.015	0.017
D	4.400	4.600	0.173	0.181
D1	1.600	1.830	0.063	0.072
E	3.950	4.250	0.156	0.167
E1	2.400	2.600	0.094	0.102
e	1.500 BSC		0.059 BSC	
D2	1.600	1.900	0.063	0.075
E2	2.700	3.100	0.106	0.122
L	0.890	1.200	0.035	0.047

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN1×1-4



Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPL740ADJ-5TR	-40 to 125°C	SOT23-5	L2A	3	Tape and Reel, 3,000	Green
TPL740F12-5TR	-40 to 125°C	SOT23-5	L2D	3	Tape and Reel, 3,000	Green
TPL740F18-5TR	-40 to 125°C	SOT23-5	L2F	3	Tape and Reel, 3,000	Green
TPL740F25-5TR	-40 to 125°C	SOT23-5	L2G	3	Tape and Reel, 3,000	Green
TPL740F28-5TR	-40 to 125°C	SOT23-5	L2H	3	Tape and Reel, 3,000	Green
TPL740F30-5TR	-40 to 125°C	SOT23-5	L2I	3	Tape and Reel, 3,000	Green
TPL740F33-5TR	-40 to 125°C	SOT23-5	L2J	3	Tape and Reel, 3,000	Green
TPL740F33-89TR	-40 to 125°C	SOT89-3	L2J	3	Tape and Reel, 4,000	Green
TPL740F33-FR	-40 to 125°C	DFN1×1-4	L2J	3	Tape and Reel, 12,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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