Features

- Input Voltage Range: 1.7 V to 5.5 V
- Output Voltage Range: 0.6 V to 5.3 V
- ±1.5% Output Accuracy Over Line Regulation, Load Regulation, and Operating Temperature Range
- 500 mA Maximum Output Current
- Low Dropout Voltage: 150 mV Typical at 500 mA
- High PSRR:
  - 89 dB at 1kHz
  - 63 dB at 100kHz
  - 55 dB at 1MHz
- 5.7 μV_{RMS} Output Voltage Noise
- Excellent Transient Response
- Stable with a 4.7 µF or Larger Ceramic Output Capacitor
- Over-Current and Over-Temperature Protection
- Output Reverse Current Protection
- Junction Temperature Range: –40°C to +125°C
- Package Options: 2×2 DFN-8

Applications

- Portable and Battery-Powered Equipment
- Mobile Phones and Tablets
- Digital Cameras and Audio Devices Power Supply
- Video Surveillance

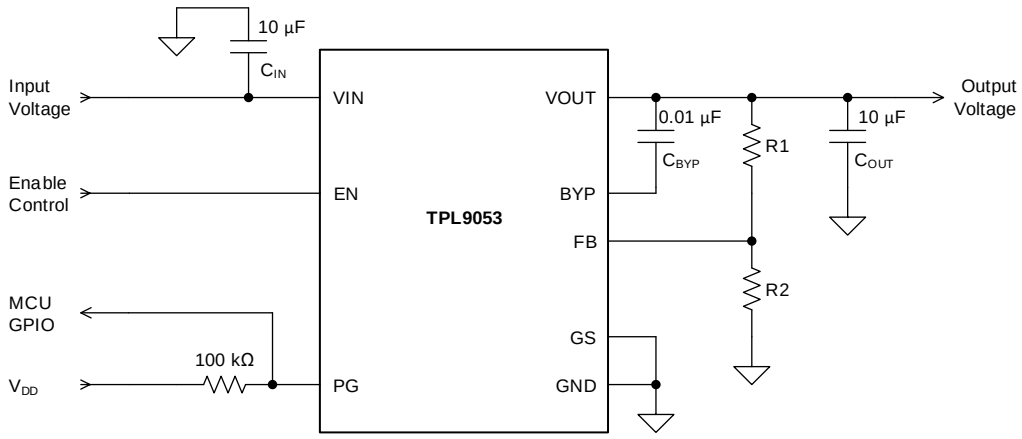
Description

The TPL9053 series products are 500-mA high PSRR, ultra-low noise, low dropout linear regulators with high output accuracy. The TPL9053 series products support adjustable output voltage ranges from 0.6 V to 5.3 V with external resistor divider and is stable with 4.7 µF or larger ceramic output capacitor.

The TPL9053 series products have high PSRR with 89 dB at 1kHz and 5.7 μV_{RMS} ultra-low noise. These features make TPL9053 series products very suitable for noise-sensitive applications with high noise from previous stage power supply, such as high-performance analog devices, or high-definition imaging equipment. Output shortage protection and thermal overload protection circuits improves the reliability under heavy load conditions.

The TPL9053 series products provide 2×2 DFN-8 package with guaranteed operating junction temperature range (T_J) from –40°C to +125°C.

Typical Application Schematic



Product Family Table

Part Number	Orderable Number	Output Voltage	Package	Transport Media, Quantity	MSL	Marking information
TPL9053	TPL9053AD-DF4R	Adjustable	2×2 DFN-8	Tape and Reel, 3,000	MSL3	L905

Table of Contents

Revision History

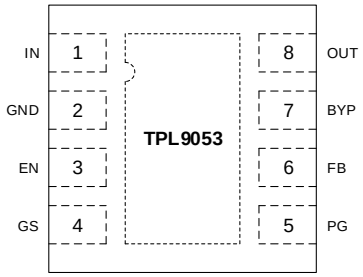
Date	Revision	Notes
2019/08/31	Rev.Pre	Preliminary Version
2020/04/08	Rev.A.0	Initial Released
2020/10/18	Rev.A.1	Add more details to PG pin description (Page 5) and PG function description (Page 12)

Pin Configuration and Functions

TPL9053 Series

8-Pin 2×2 DFN

Top View



Pin Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
BYP	7	I	Bypass input pin. Connect a 10-nF ceramic capacitor from BYP to OUT to reduce output noise.
EN	3	I	Regulator enable pin. Drive EN high to turn on the regulator; and drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
FB	6	I	Output voltage feedback pin. Connect to a resistor divider to adjust the output voltage.
GND	2	–	Ground reference pin. Connect GND pin to PCB ground plane directly.
GS	4	–	Internal reference pin. MUST connect GS pin to PCB ground plane directly.
IN	1	I	Input voltage pin. Bypass IN to GND with a 10 μF or greater capacitor.
OUT	8	O	Regulated output voltage pin. Bypass OUT to GND with a 4.7 μF or greater capacitor.
PG	5	O	Open-drain power-good output pin. Connect a 100-kΩ pull-up resistor to the logic voltage supply, or leave this pin open if not used. PG goes **LOW** after the output voltage ramps above $V_{PG,TH}$, and PG keeps **HIGH** when the output voltage is below the threshold.

(1) Thermal Pad MUST be connected to PCB ground plane directly.

Specifications

Absolute Maximum Ratings

		MIN	MAX	UNIT
EN, IN		–0.3	6	V
BYP, FB, GS, OUT, PG		–0.3	6	V
T_J	Junction Temperature Range	–40	150	°C
T_{STG}	Storage Temperature Range	–65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond the Absolute Maximum Ratings may permanently damage the device.

(2) All voltage values are with respect to GND.

ESD Ratings

		Condition	Minimum Level	UNIT
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±6000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1500	V

Recommended Operating Conditions

		MIN	MAX	UNIT
IN		1.7	5.5	V
EN		0	V_{IN}	V
OUT		0	5.5	V
BYP, FB, PG		0	V_{OUT}	V
C_{BYP}		1	100	nF
C_{OUT}		4.7		μF
ESR		1	100	mΩ
T_J	Junction Temperature Range	–40	125	°C
P_D	Power Dissipation	0	400	mW

Thermal Information

PACKAGE	θ_{JA}	θ_{JC}	UNIT
2×2 DFN-8	120	20.3	°C/W

Electrical Characteristics

All test condition: V_{IN} = $V_{OUT(NOM)}$ + 1V, C_{IN} = 10 µF, C_{OUT} = 10 µF, –40°C ≤ T_J ≤ +125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Input Voltage and Current						
V_{IN}	Input supply voltage range		1.7		5.5	V
I_{GND}	Ground pin current	I_{OUT} = 0 mA		130	180	µA
I_{SHDN}	Shutdown current	EN = GND		0.05	2	µA
Enable Input Voltage and Current						
$V_{IN(EN)}$	EN logic-input high level (enable)		1.2		V_{IN}	V
$V_{IL(EN)}$	EN logic-input low level (disable)		0		0.4	V
I_{EN}	EN pin leakage current	V_{EN} = 5 V		1	2	µA
Regulated Output Voltage and Current						
V_{OUT}	Output voltage accuracy	–40°C ≤ T_J ≤ +125°C	–1.5%		1.5%	
ΔV_{OUT}	Line regulation	V_{IN} = $V_{OUT(NOM)}$ + 1 V to 5.5 V		1		mV/V
	Load regulation	V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA to 500 mA		0.005		mV/mA
V_{DO} (1)	Dropout voltage	V_{IN} ≥ 3.6 V, I_{OUT} = 100 mA		30	60	mV
		V_{IN} ≥ 3.6 V, I_{OUT} = 500 mA		150	280	mV
		V_{IN} = 1.7 V, I_{OUT} = 500mA		300		mV
I_{OUT}	Output voltage	V_{OUT} in regulation	0		500	mA
I_{LIM}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	550	720		mA
I_{SC}	Short-circuit to ground current limit	V_{OUT} is forced to ≤ 50 mV, T_A = 25°C		100		mA
PSRR	Power supply rejection ratio	I_{OUT} = 20 mA, f = 100 Hz		82		dB
		I_{OUT} = 20 mA, f = 1 kHz		89		dB
		I_{OUT} = 20 mA, f = 100 kHz		63		dB
		I_{OUT} = 20 mA, f = 1 MHz		55		dB
V_N	Output noise voltage	I_{OUT} = 150 mA, BW = 100Hz to 80 kHz		5.7		μV_{RMS}
t_{STR}	Start-up time	V_{OUT} reaches 95% of nominal output voltage after EN = high		0.8	3	ms
Feedback and Bypass						
V_{FB}	Output feedback voltage		0.591	0.6	0.609	V
I_{FB}	Output feedback leakage current	V_{IN} = 5.5 V, V_{FB} = 0.75 V, T_A = 25°C		0.001	0.1	µA
I_{BYP}	BYP pin current during startup			1		mA
Power Good						
$V_{PG,TH}$	PG threshold	OUT rising until PG is toggled	88	91	94	% of V_{OUT}
	PG hysteresis			2.5		% of V_{OUT}
$V_{PG,IL}$	PG voltage low	1mA to PG pin		10	100	mV
I_{PG}	PG pin leakage current		–1	0.01	1	µA

(1) The dropout voltage is defined as V_{DO} = V_{IN} - V_{OUT}. For V_{IN} ≥ 3.6 V condition, dropout voltage is measured when the FB pin voltage is forced at 0.58 V. For VIN = 1.7 V condition, dropout voltage is guaranteed by design.

Electrical Characteristics (continued)

All test condition: V_{IN} = $V_{OUT(NOM)}$ + 1V, C_{IN} = 10 µF, C_{OUT} = 10 µF, –40°C ≤ T_J ≤ +125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transient Characteristics						
ΔV_{OUT}	Line Transient	V_{IN} = 3.8 V to 4.8 V, rising and falling slew rate is 1V/5µs, I_{OUT} = 500 mA		3		mVpp
	Load Transient	I_{OUT} = 2 mA to 100 mA in 1 µs		10		mVpp
		I_{OUT} = 50 mA to 500 mA in 1 µs		20		mVpp
$V_{REV,TH}$	IN-OUT Reverse voltage turnoff threshold	V_{OUT} – V_{IN} when input voltage falls		19		mV
Temperature Range						
T_{SD}	Thermal shutdown temperature			165		ºC
	Thermal shutdown hysteresis			15		ºC

Typical Performance Characteristics

All test condition: V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{OUT} = 2.8V, C_{IN} = 10 µF, C_{OUT} = 10 µF, T_J = 25°C, unless otherwise noted.

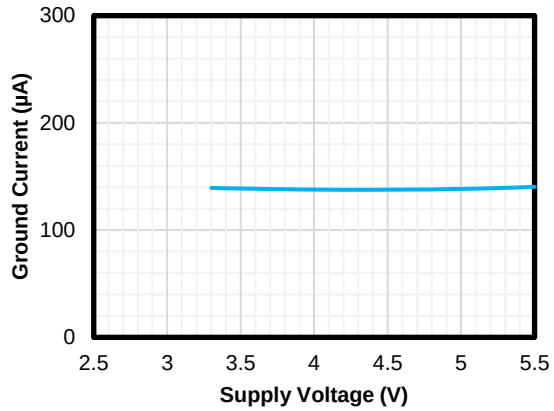
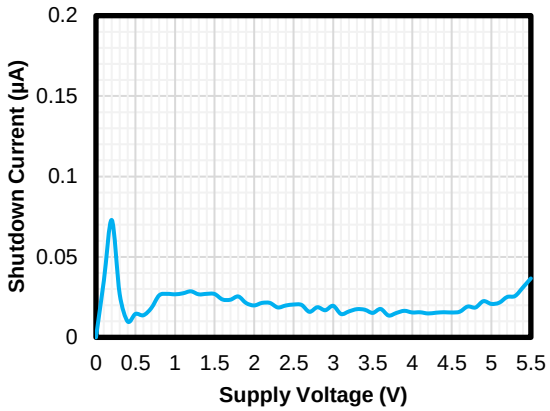
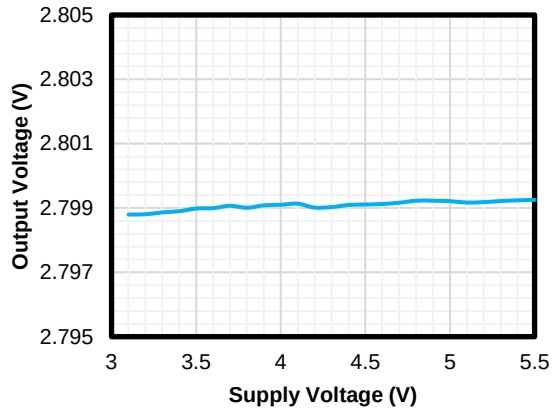


Figure 1 Quiescent Current vs Input Voltage



EN = GND

Figure 2 Quiescent Current vs Input Voltage



I_{OUT} = 1mA

Figure 3 Line Regulation

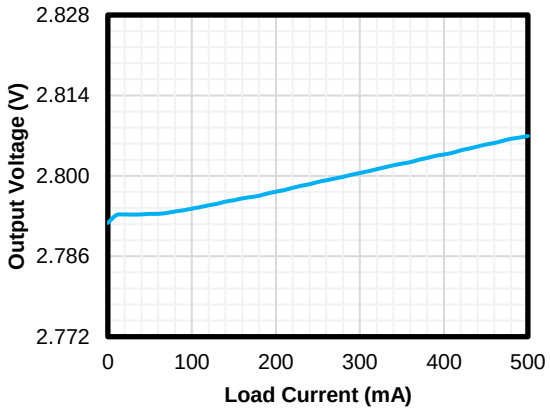
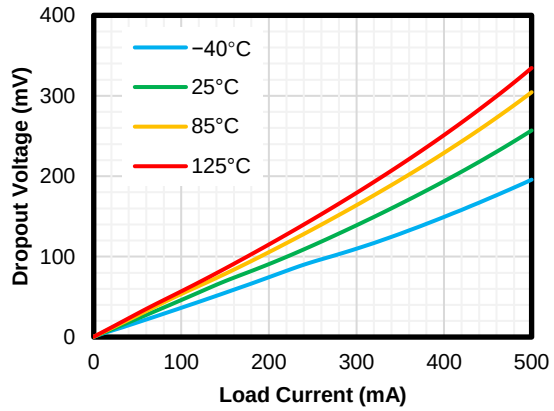
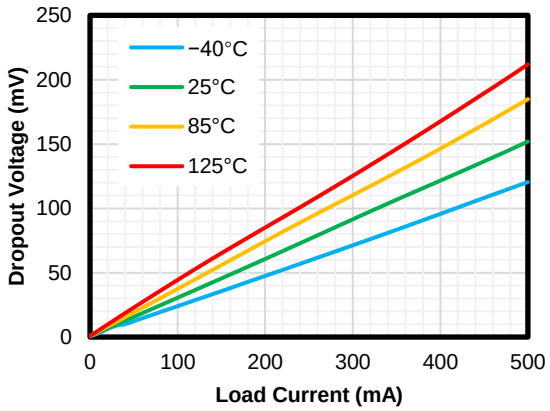


Figure 4 Load Regulation



V_{OUT} = 1.8 V

Figure 5 Dropout Voltage vs Output Current

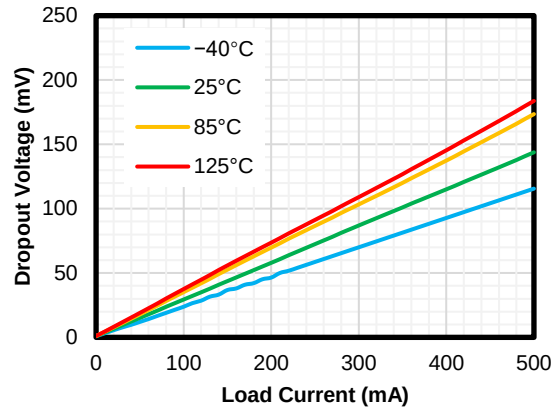


V_{OUT} = 2.8 V

Figure 6 Dropout Voltage vs Output Current

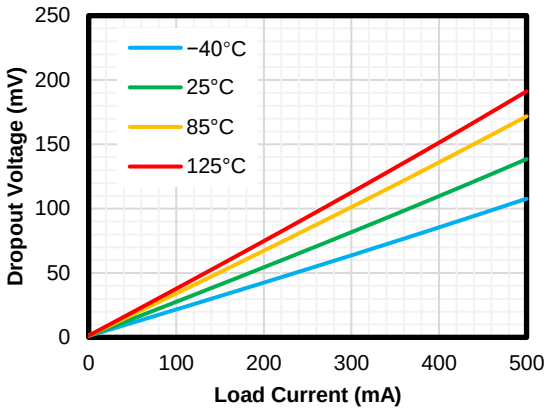
Typical Performance Characteristics (continued)

All test condition: V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{OUT} = 2.8V, C_{IN} = 10 µF, C_{OUT} = 10 µF, T_J = 25°C, unless otherwise noted.



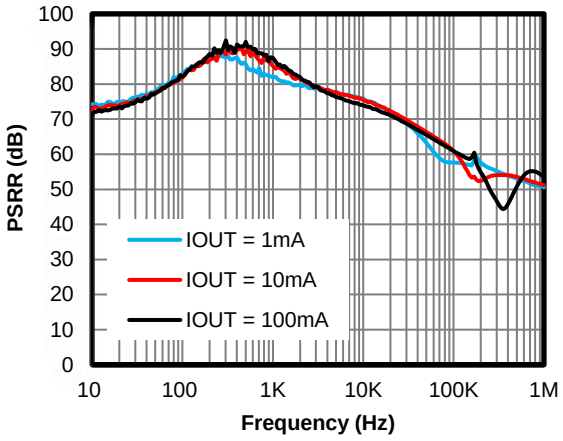
V_{OUT} = 3.3 V

Figure 7. Dropout Voltage vs Output Current



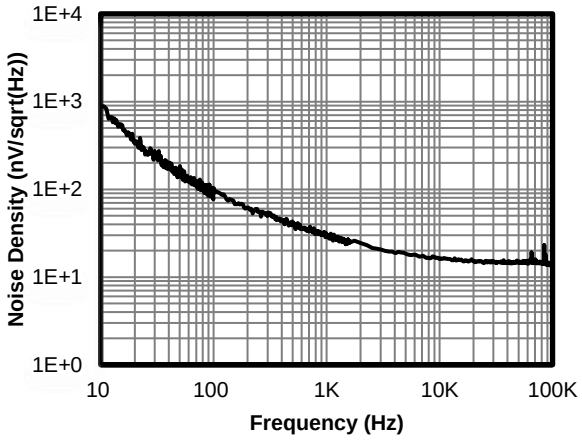
V_{OUT} = 5.0 V

Figure 8. Dropout Voltage vs Output Current



C_{BYP} = 10 nF

Figure 9. PSRR



I_{OUT} = 280 mA

Figure 10. Output Noise

Detailed Description

Overview

The TPL9053 series products are 500-mA high PSRR, ultra-low noise, low dropout linear regulators with high output accuracy. The TPL9053 series products support adjustable output voltage ranges from 0.6 V to 5.3 V with external resistor divider and is stable with 4.7 μF or larger ceramic output capacitor.

The TPL9053 series products have high PSRR with 89 dB at 1kHz and 5.7 μVRMS ultra-low noise. These features make TPL9053 series products very suitable for noise-sensitive applications with high noise from previous stage power supply, such as high-performance analog devices, or high-definition imaging equipment. Output shortage protection and thermal overload protection circuits improves the reliability under heavy load conditions.

Functional Block Diagram

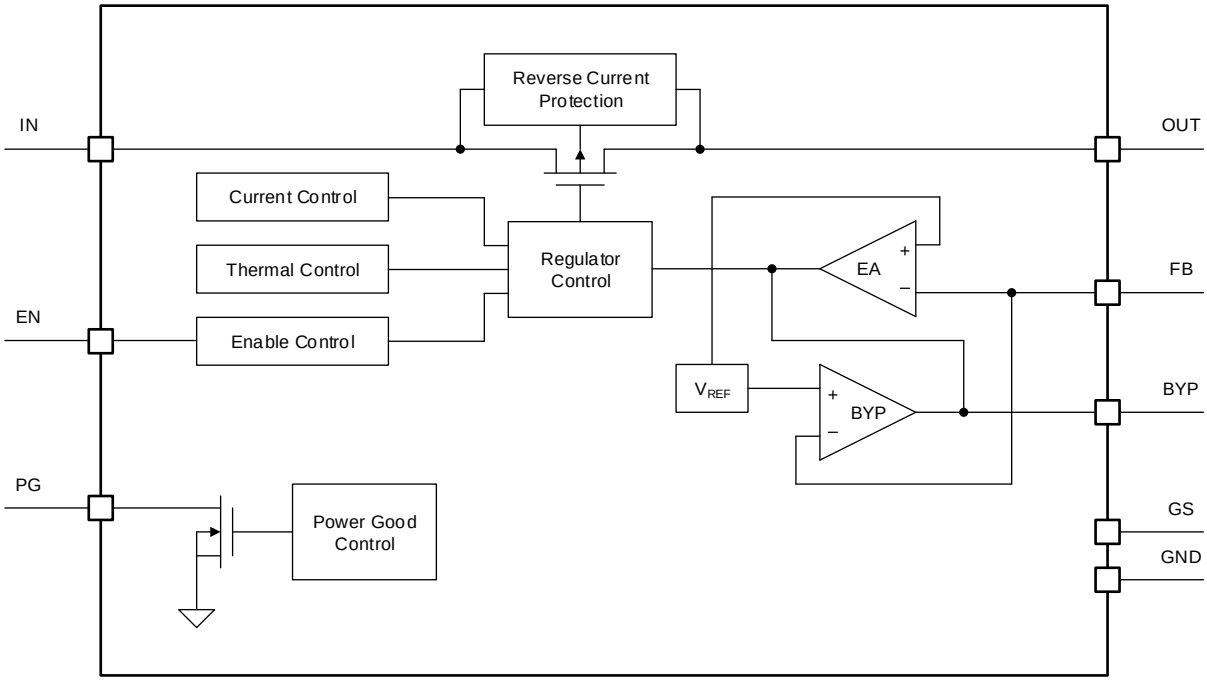


Figure 11 TPL9053 Functional Block Diagram

Feature Description

Enable (EN)

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Adjustable Output Voltage (FB and OUT)

The output voltage range of TPL9053 series can be set from 0.6 V to 5.3 V by selecting different external resistors as shown in Figure 12. Use Equation 1 to calculate the output voltage. Suggest setting the resistance of lower feedback resistor R2 between 50 kΩ and 120 kΩ to minimize FB input bias current error.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where the feedback voltage V_{FB} is 0.6 V.

Output Voltage Ramp-up Slew Rate Control

To avoid the start-up inrush current, the TPL9053 series integrate an output voltage ramp-up slew rate control. When the input voltage is ready and the device-enable signal asserts, the output voltage of TPL9053 ramps up with a fixed slew rate. Under room temperature condition, it takes 800 μs from the rising edge of enable signal to the V_{OUT} reaching 95% of nominal output voltage. This start-up time is independent with output capacitor and BYP capacitor, and the maximum 3-ms start-up time occurs under the –40°C ambient temperature condition.

Bypass (BYP)

The TPL9053 series provide the BYP pin to reduce the regulator output noise and offer a feed-back path to improve the transient response. Suggest connecting a capacitor from 1nF to 100nF from BYP to OUT.

Power-Good Indicator (PG)

The TPL9053 series integrate an open-drain output power good indicator. After regulator startup, the PG pin keeps high impendence until the output voltage reached the power good threshold $V_{PG,TH}$ (91% of V_{OUT}). When output voltage is higher than $V_{PG,TH}$, the PG pin turns to low output impedance, and PG is pulled down to low voltage level to indicate the output voltage is ready.

Figure 12 shows the power good indicator status after device starts up.

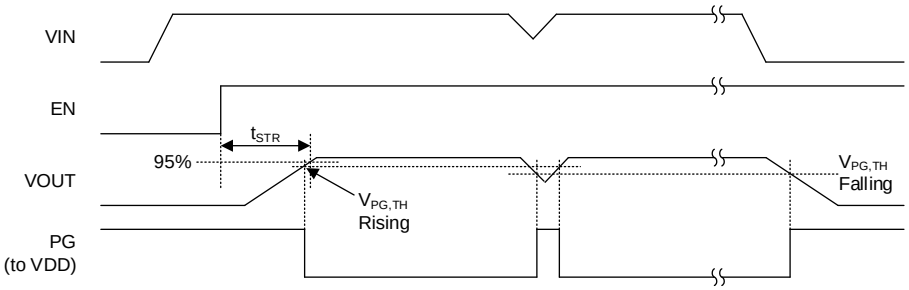


Figure 12 Power Good Indication

Reverse-Current Protection

The TPL9053 series provide the RCP protection to prevent output reverse current. If large capacitors been used at the output, there would be large reverse current when the input voltage is lower than output voltage. The TPL9053 series can shut off the regulator and body diode path to prevent the device damaged from reverse current fault.

Over-Current Protection and Short-to-Ground Protection

The TPL9053 series integrate an internal current limit that helps to protect the regulator during fault conditions.

- When the output is pulled down below the regulated voltage, over-current protection starts to work and limit the output current to 720 mA (typ).
- When the output is shorted to ground directly or pulled down below 50 mV, short-to-ground protection starts to work and limit the output current to 100 mA (typ).

Under the over-current conditions, the internal junction temperature ramps up quickly. When the junction temperature is high enough, it will cause the over temperature protection.

Over-Temperature Protection

The recommended operating junction temperature range is –40°C to 125°C. When the junction temperature is between 125°C and the thermal shutdown (TSD) threshold, the regulator can still work well, but will reduce the device lifetime for long-term using.

The over-temperature protection works when the junction temperature exceeds the thermal shutdown (TSD) threshold, which turns off the regulator immediately. Until when the device cools down and the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the regulator turns on again.

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL9053 devices are a series of 500-mA high PSRR, ultra-low noise, low-dropout linear regulator. The following application schematic shows a typical usage of the TPL9053 series.

Typical Application

Figure 13 shows the typical application schematic of the TPL9053 series.

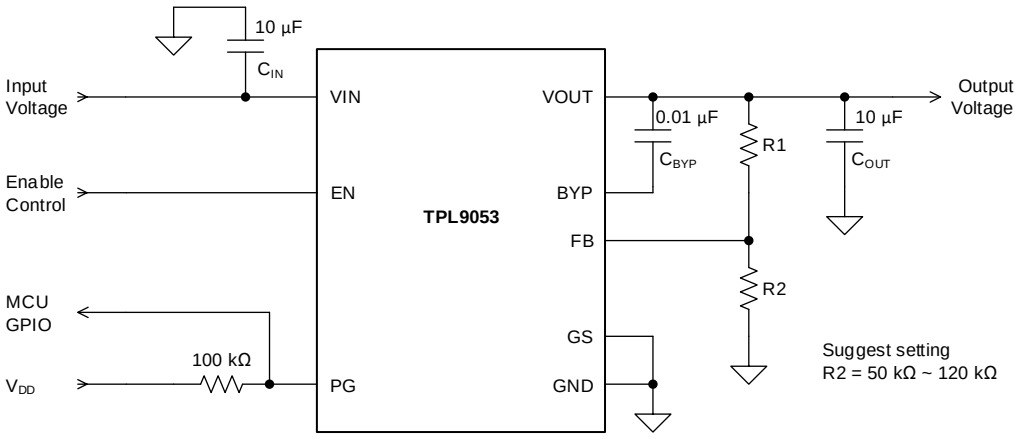


Figure 13 Typical Application Schematic

Input Capacitor and Output Capacitor

3PEAK recommends adding a 10 µF or greater capacitor with a 0.1 µF bypass capacitor in parallel at IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL9053 series requires an output capacitor of 4.7 µF or greater. 3PEAK recommends selecting a X5R- or X7R-type 10-µF ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (2)$$

The junction temperature can be estimated using Equation 3. θ_{JA} is the junction-to-ambient thermal resistance.

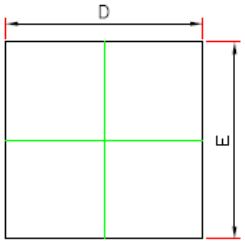
$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

Layout Requirements

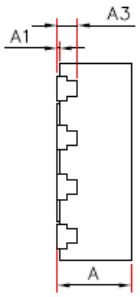
- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the input pin to ground with a 0.1 μF bypass capacitor. The loop area formed by the bypass capacitor connection, IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.

Package Outline Dimensions

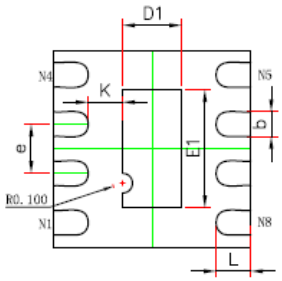
2×2 DFN-8



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.500	0.700	0.020	0.028
E1	1.100	1.300	0.043	0.051
k	0.350REF.		0.014REF.	
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.274	0.426	0.011	0.017

单击下面可查看定价，库存，交付和生命周期等信息

>>3PEAK(思瑞浦)