Micropower, Zero Drift, True Rail-to-Rail Instrumentation Amplifier

Data Sheet **AD8237**

FEATURES

- Gain set with 2 external resistors
  - Can achieve low gain drift at all gains
- Ideal for battery powered instruments
  - Supply current: 115 µA
  - Rail-to-rail input and output
  - Zero input crossover distortion
- Designed for excellent dc performance
  - Minimum CMRR: 106 dB
  - Maximum offset voltage drift: 0.3 µV/°C
  - Maximum gain error: 0.005% (all gains)
  - Maximum gain drift: 0.5 ppm/°C (all gains)
  - Input bias current: 1 nA guaranteed to 125°C
- Bandwidth mode pin (BW) to adjust compensation
- 8 kV HBM ESD rating
- RFI filter on-chip
- Single-supply operation: 1.8 V to 5.5 V
- 8-lead MSOP package

APPLICATIONS

- Bridge amplification
- Pressure measurement
- Medical instrumentation
- Thermocouple interface
- Portable systems
- Current measurement

GENERAL DESCRIPTION

The AD8237 is a micropower, zero drift, rail-to-rail input and output instrumentation amplifier. The relative match of two resistors sets any gain from 1 to 1000. The AD8237 has excellent gain accuracy performance that can be preserved at any gain with two ratio-matched resistors.

The AD8237 employs the indirect current feedback architecture to achieve a true rail-to-rail capability. Unlike conventional in-amps, the AD8237 can fully amplify signals with common-mode voltage at or even slightly beyond its supplies. This enables applications with high common-mode voltages to use smaller supplies and save power.

The AD8237 is an excellent choice for portable systems. With a minimum supply voltage of 1.8 V, a 115 µA typical supply current, and wide input range, the AD8237 makes full use of a limited power budget, yet offers bandwidth and drift performance suitable for bench-top systems.

PIN CONFIGURATION

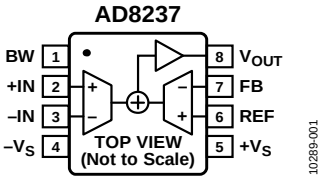

Figure 1.

Table 1. Instrumentation Amplifiers by Category[1]

General Purpose	Zero Drift	Military Grade	Micropower	Digital Gain
AD8421	AD8237	AD620	AD8237	AD8250
AD8221/AD8222	AD8231	AD621	AD8420	AD8251
AD8220/AD8224	AD8293	AD524	AD8235/AD8236	AD8253
AD8228	AD8553	AD526	AD627	AD8231
AD8295	AD8556	AD624		
AD8226	AD8557			

[1] See www.analog.com for the latest instrumentation amplifiers.

The AD8237 is available in an 8-lead MSOP package. Performance is specified over the full temperature range of −40°C to +125°C.

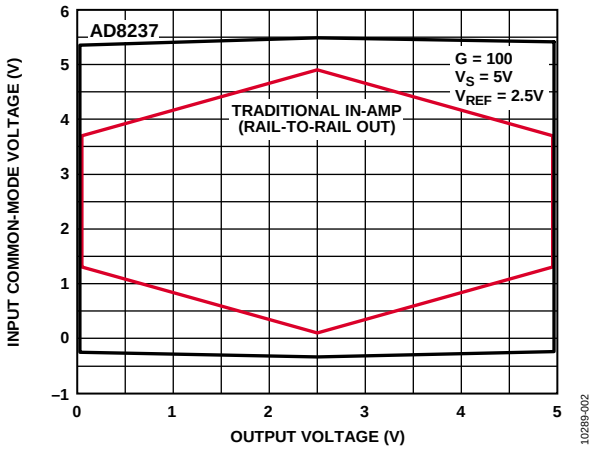

Figure 2. Input Common-Mode Voltage vs. Output Voltage, $+V_S$ = 5 V, G = 100

Rev. 0

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REVISION HISTORY

8/12—Revision 0: Initial Version

SPECIFICATIONS

$+V_S$ = +5 V, $-V_S$ = 0 V, V_{REF} = 2.5 V, V_{CM} = 2.5 V, T_A = 25°C, G = 1 to 1000, R_L = 10 kΩ to ground, specifications referred to input, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V_{CM} = 0.1 V to 4.9 V				
CMRR at DC					
G = 1, G = 10		106	120		dB
G = 100, G = 1000		114	140		dB
Over Temperature (G = 1)	T_A = −40°C to +125°C	104			dB
CMRR at 1 kHz			80		dB
NOISE					
Voltage Noise					
Spectral Density	f = 1 kHz		68		nV/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz		1.5		µV p-p
Current Noise					
Spectral Density	f = 1 kHz		70		fA/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz		3		pA p-p
VOLTAGE OFFSET					
Offset			30	75	µV
Average Temperature Coefficient	T_A = −40°C to +125°C			0.3	µV/°C
Offset RTI vs. Supply (PSR)		100			dB
INPUTS[1]	Valid for REF and FB pair, as well as +IN and −IN				
Input Bias Current	T_A = +25°C		250	650	pA
Over Temperature	T_A = −40°C to +125°C			1	nA
Average Temperature Coefficient			0.5		pA/°C
Input Offset Current	T_A = +25°C		250	650	pA
Over Temperature	T_A = −40°C to +125°C			1	nA
Average Temperature Coefficient			0.5		pA/°C
Input Impedance					
Differential			100‖5		MΩ‖pF
Common Mode			800‖10		MΩ‖pF
Differential Input Operating Voltage	T_A = −40°C to +125°C		±3.85		V
Input Operating Voltage (+IN, −IN, or REF)	T_A = +25°C	$-V_S$ − 0.3		$+V_S$ + 0.3	V
	T_A = −40°C to +125°C	$-V_S$ − 0.2		$+V_S$ + 0.2	V
DYNAMIC RESPONSE					
Small Signal Bandwidth	−3 dB				
Low Bandwidth Mode	Pin 1 connected to $-V_S$				
G = 1			200		kHz
G = 10			20		kHz
G = 100			2		kHz
G = 1000			0.2		kHz
High Bandwidth Mode	Pin 1 connected to $+V_S$				
G = 10			100		kHz
G = 100			10		kHz
G = 1000			1		kHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Settling Time 0.01%	4 V output step				
Low Bandwidth Mode	Pin 1 connected to $-V_S$				
G = 1			80		µs
G = 10			100		µs
G = 100			440		µs
G = 1000			4		ms
High Bandwidth Mode	Pin 1 connected to $+V_S$				
G = 10			80		µs
G = 100			100		µs
G = 1000			820		µs
Slew Rate					
Low Bandwidth Mode			0.05		V/µs
High Bandwidth Mode			0.15		V/µs
EMI Filter Frequency			6		MHz
GAIN[2]	G = 1 + (R2/R1)				
Gain Range[3]		1		1000	V/V
Gain Error	V_{OUT} = 0.1 V to 4.9 V, G = 1 to G = 1000			0.005	%
Gain Error vs. V_{CM}			15		ppm/V
Gain vs. Temperature	T_A = −40°C to +125°C			0.5	ppm/°C
Gain Nonlinearity	V_{OUT} = 0.2 V to 4.8 V, R_L = 10 kΩ to ground				
G = 1, G = 10			3		ppm
G = 100			6		ppm
G = 1000			10		ppm
OUTPUT					
Output Swing					
R_L = 10 kΩ to Midsupply	T_A = +25°C	$-V_S$ + 0.05		$+V_S$ − 0.05	V
	T_A = −40°C to 125°C	$-V_S$ + 0.07		$+V_S$ − 0.07	V
R_L = 100 kΩ to Midsupply	T_A = +25°C	$-V_S$ + 0.02		$+V_S$ − 0.02	V
	T_A = −40°C to 125°C	$-V_S$ + 0.03		$+V_S$ − 0.03	V
Short-Circuit Current			4		mA
POWER SUPPLY					
Operating Range		1.8		5.5	V
Quiescent Current	T_A = +25°C		115	130	µA
	T_A = −40°C to +125°C			150	µA
TEMPERATURE RANGE					
Specified		−40		+125	°C

[1] Specifications apply to input voltages between 0 V and 5 V. When measuring voltages beyond the supplies, there is additional offset error, bias currents increase, and input impedance decreases, especially at higher temperatures.
[2] For G > 1, errors from the external resistors, R1 and R2, must be added to these specifications, including error from the FB pin bias current.
[3] The AD8237 has only been characterized for gains of 1 to 1000; however, higher gains are possible.

$+V_S$ = 1.8 V, $-V_S$ = 0 V, V_{REF} = 0.9 V, V_{CM} = 0.9 V, T_A = 25°C, G = 1 to 1000, R_L = 10 kΩ to ground, specifications referred to input, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V_{CM} = 0.2 V to 1.6 V				
CMRR at DC					
G = 1, G = 10		100	120		dB
G = 100, G = 1000		114	140		dB
Over Temperature (G = 1)	T_A = −40°C to +125°C	94			dB
CMRR at 1 kHz			80		dB
NOISE					
Voltage Noise					
Spectral Density	f = 1 kHz, V_{DIFF} ≤ 100 mV		68		nV/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz, V_{DIFF} ≤ 100 mV		1.5		µV p-p
Current Noise					
Spectral Density	f = 1 kHz		70		fA/√Hz
Peak to Peak	f = 0.1 Hz to 10 Hz		3		pA p-p
VOLTAGE OFFSET					
Offset			25	75	µV
Average Temperature Coefficient	T_A = −40°C to +125°C			0.3	µV/°C
Offset RTI vs. Supply (PSR)		100			dB
INPUTS[1]	Valid for REF and FB pair, as well as +IN and −IN				
Input Bias Current	T_A = +25°C		250	650	pA
Over Temperature	T_A = −40°C to +125°C			1	nA
Average Temperature Coefficient			0.5		pA/°C
Input Offset Current	T_A = +25°C		250	650	pA
Over Temperature	T_A = −40°C to +125°C			1	nA
Average Temperature Coefficient			0.5		pA/°C
Input Impedance					
Differential			100‖5		MΩ‖pF
Common Mode			800‖10		MΩ‖pF
Differential Input Operating Voltage	T_A = −40°C to +125°C		± 0.75		V
Input Operating Voltage (+IN, −IN, REF, or FB)	T_A = +25°C	$-V_S$ − 0.3		$+V_S$ + 0.3	V
	T_A = −40°C to +125°C	$-V_S$ − 0.2		$+V_S$ + 0.2	V
DYNAMIC RESPONSE					
Small Signal Bandwidth	−3 dB				
Low Bandwidth Mode	Pin 1 connected to $-V_S$				
G = 1			200		kHz
G = 10			20		kHz
G = 100			2		kHz
G = 1000			0.2		kHz
High Bandwidth Mode	Pin 1 connected to $+V_S$				
G = 10			100		kHz
G = 100			10		kHz
G = 1000			1		kHz
Slew Rate					
Low Bandwidth Mode			0.05		V/µs
High Bandwidth Mode			0.15		V/µs
EMI Filter Frequency			6		MHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN[2]	G = 1 + (R2/R1)				
Gain Range[3]		1		1000	V/V
Gain Error	V_{OUT} = 0.2 V to 1.6 V, G = 1 to G = 1000			0.005	%
Gain Error vs. V_{CM}			15		ppm/V
Gain vs. Temperature	T_A = −40°C to +125°C			0.5	ppm/°C
Gain Nonlinearity	V_{OUT} = 0.2 V to 1.6 V				
G = 1, G = 10			3		ppm
G = 100			6		ppm
G = 1000			10		ppm
OUTPUT					
Output Swing					
R_L = 10 kΩ to Midsupply	T_A = +25°C	$-V_S$ + 0.05		$+V_S$ − 0.05	V
	T_A = −40°C to 125°C	$-V_S$ + 0.07		$+V_S$ − 0.07	V
R_L = 100 kΩ to Midsupply	T_A = +25°C	$-V_S$ + 0.02		$+V_S$ − 0.02	V
	T_A = −40°C to 125°C	$-V_S$ + 0.03		$+V_S$ − 0.03	V
Short-Circuit Current			4		mA
POWER SUPPLY					
Operating Range		1.8		5.5	V
Quiescent Current	T_A = +25°C		115	130	µA
	T_A = −40°C to +125°C			150	µA
TEMPERATURE RANGE					
Specified		−40		+125	°C

[1] Specifications apply to input voltages between 0 V and 1.8 V. When measuring voltages beyond the supplies, there is additional offset error, bias currents increase, and input impedance decreases, especially at higher temperatures.
[2] For G > 1, errors from the external resistors, R1 and R2, must be added to these specifications, including error from the FB pin bias current.
[3] The AD8237 has only been characterized for gains of 1 to 1000; however, higher gains are possible.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at −IN, +IN, FB, or REF[1]	$+V_S$ + 0.5 V
Minimum Voltage at −IN, +IN, FB, or REF[1]	$-V_S$ − 0.5 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature Range	−65°C to +150°C
ESD	
Human Body Model	8 kV
Charge Device Model	1.25 kV
Machine Model	0.2 kV

[1] If input voltages beyond the specified minimum or maximum voltages are expected, place resistors in series with the inputs to limit the current to 5 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device in free air.

Table 5.

Package	θ_{JA}	Unit
8-Lead MSOP, 4-Layer JEDEC Board	145.7	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

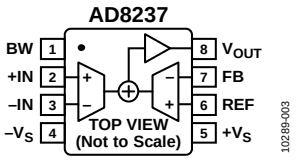


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BW	For high bandwidth mode, connect this pin to $+V_S$, or for low bandwidth mode, connect this pin to $-V_S$. Do not leave this pin floating.
2	+IN	Positive Input.
3	−IN	Negative Input.
4	$-V_S$	Negative Supply.
5	$+V_S$	Positive Supply.
6	REF	Reference Input.
7	FB	Feedback Input.
8	V_{OUT}	Output.

TYPICAL PERFORMANCE CHARACTERISTICS

$+V_S$ = +5 V, $-V_S$ = 0 V, V_{REF} = 2.5 V, T_A = 25°C, R_L = 10 kΩ to ground, unless otherwise noted.

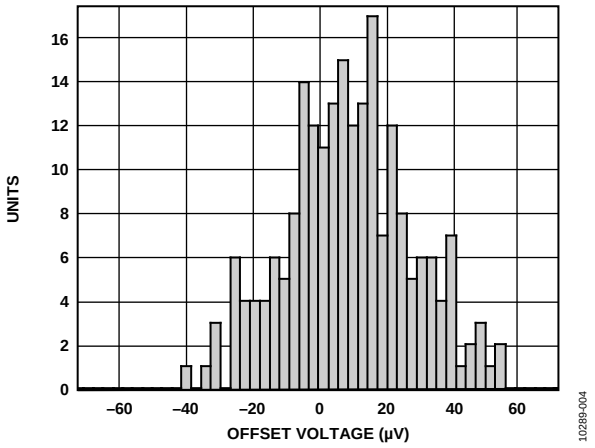


Figure 4. Typical Distribution of Offset Voltage

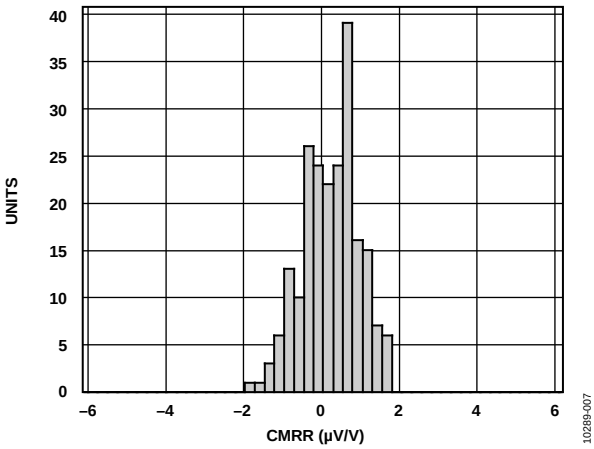


Figure 7. Typical Distribution of CMRR

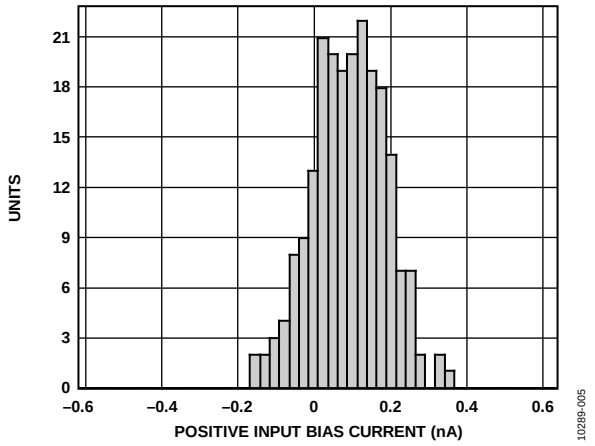


Figure 5. Typical Distribution of Input Bias Current

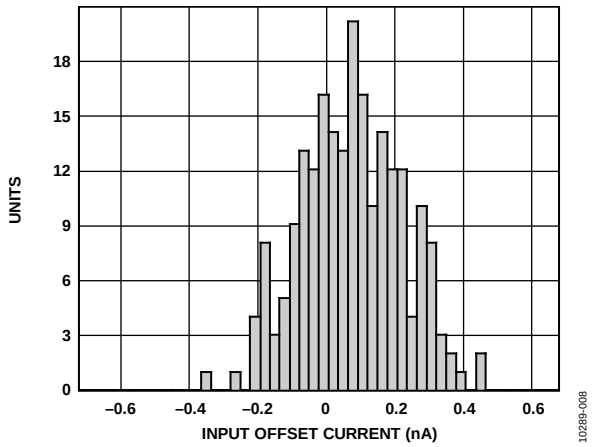


Figure 8. Typical Distribution of Input Offset Current

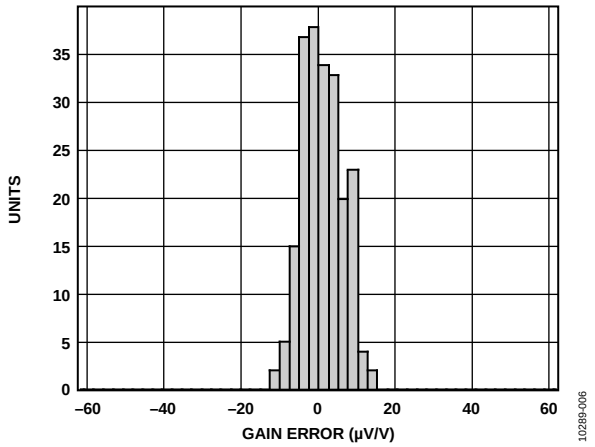


Figure 6. Typical Distribution of Gain Error (G = 1)

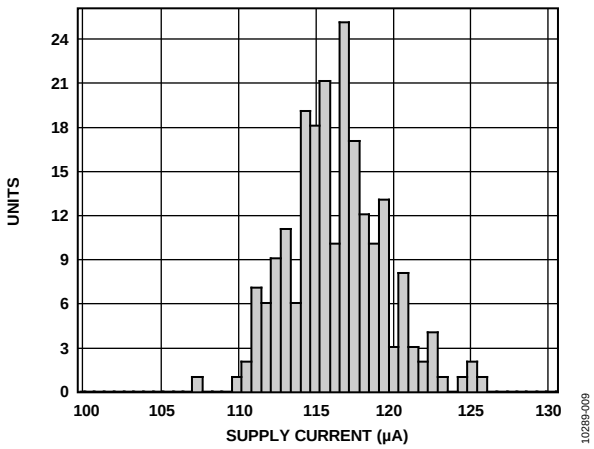


Figure 9. Typical Distribution of Supply Current

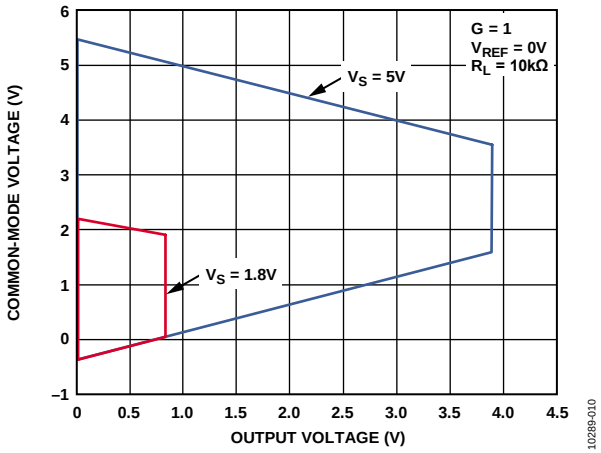


Figure 10. Input Common-Mode Voltage vs. Output Voltage, $G = 1$, $V_{REF} = 0$ V, $V_S = 5$ V and $V_S = 1.8$ V, $R_L = 10$ kΩ to Ground

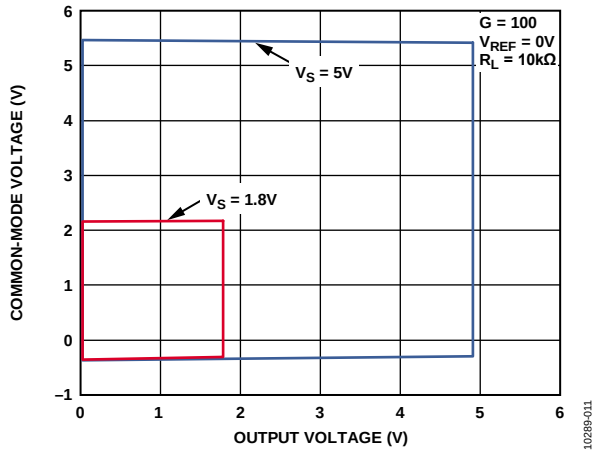


Figure 11. Input Common-Mode Voltage vs. Output Voltage, $G = 100$, $V_{REF} = 0$ V, $V_S = 5$ V and $V_S = 1.8$ V, $R_L = 10$ kΩ to Ground

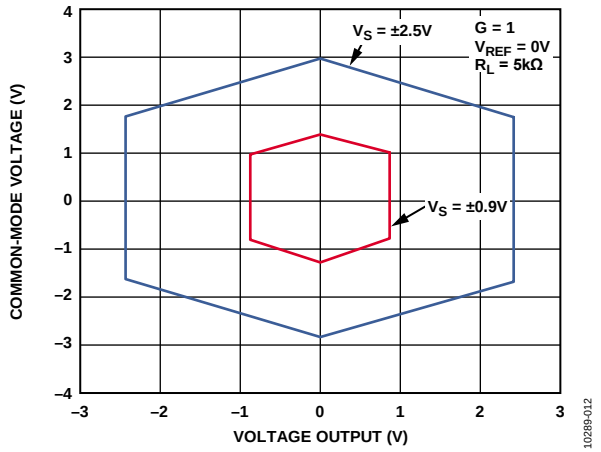


Figure 12. Input Common-Mode Voltage vs. Output Voltage, $G = 1$, $V_{REF} = 0$ V, $V_S = \pm 2.5$ V and $V_S = \pm 0.9$ V, $R_L = 5$ kΩ to Ground

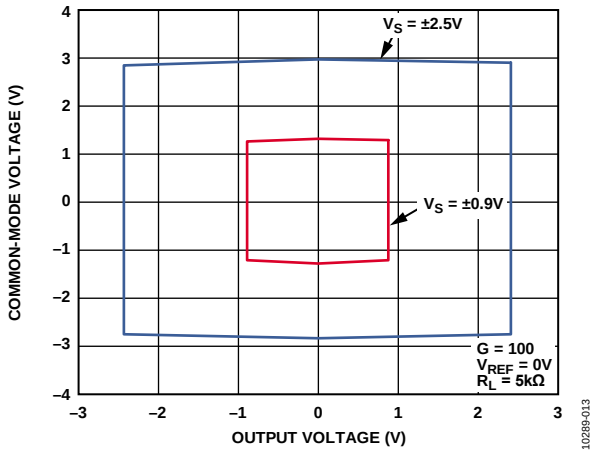


Figure 13. Input Common-Mode Voltage vs. Output Voltage, $G = 100$, $V_{REF} = 0$ V, $V_S = \pm 2.5$ V and $V_S = \pm 0.9$ V, $R_L = 5$ kΩ to Ground

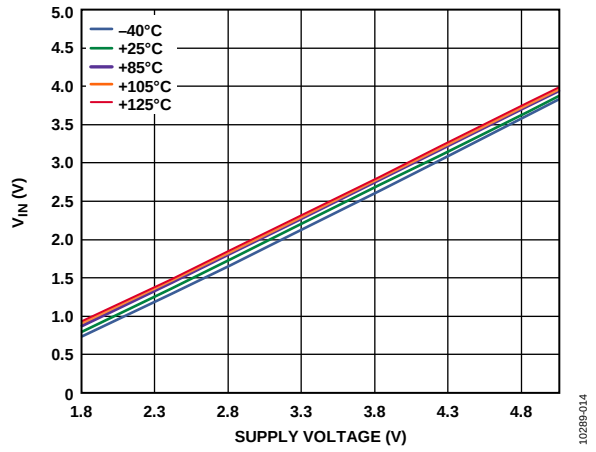


Figure 14. Maximum Differential Input vs. Supply Voltage

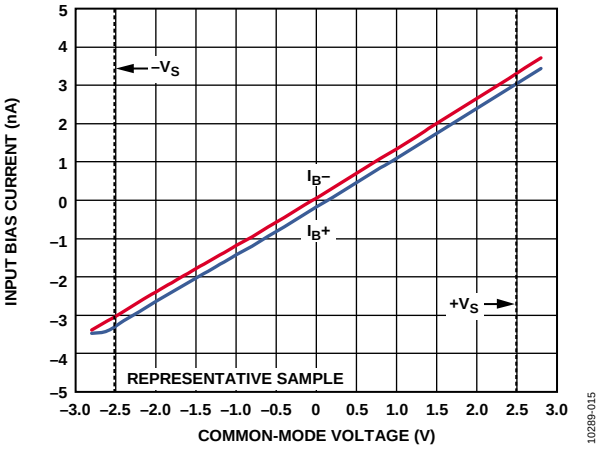


Figure 15. Input Bias Current vs. Common-Mode Voltage

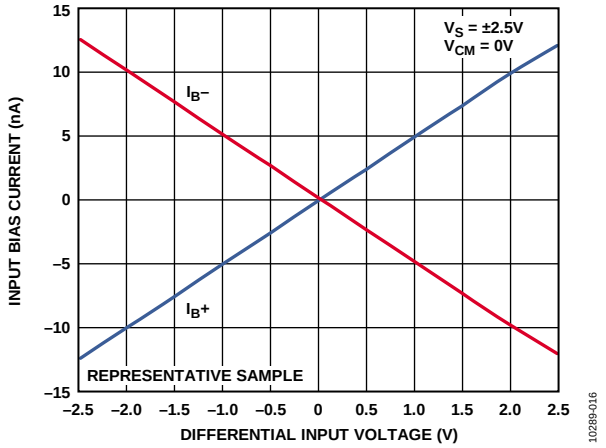


Figure 16. Input Bias Current vs. Differential Input Voltage

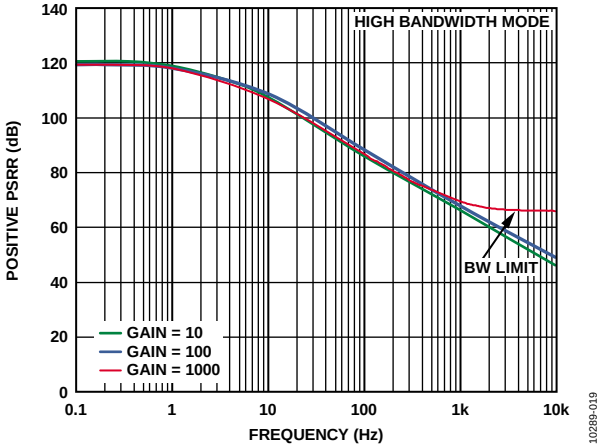


Figure 19. Positive PSRR vs. Frequency, RTI, High Bandwidth Mode

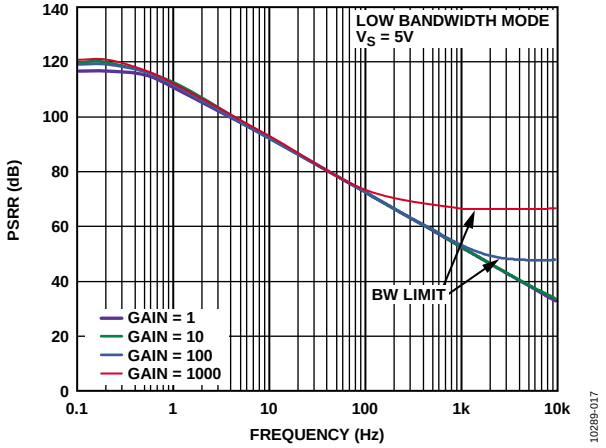


Figure 17. Positive PSRR vs. Frequency, RTI, Low Bandwidth Mode, V_S = 5 V

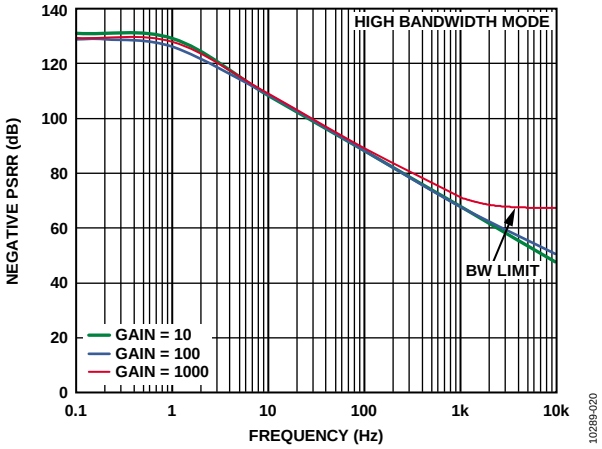


Figure 20. Negative PSRR vs. Frequency, RTI, High Bandwidth Mode

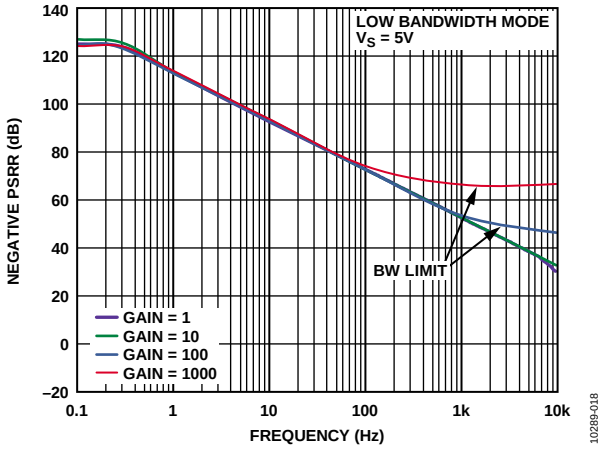


Figure 18. Negative PSRR vs. Frequency, RTI, Low Bandwidth Mode, V_S = 5 V

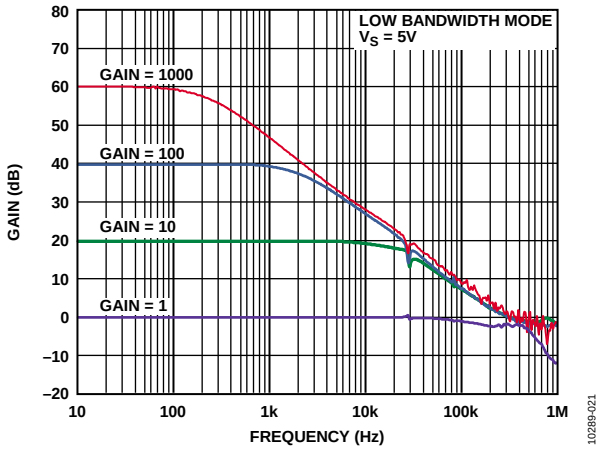


Figure 21. Gain vs. Frequency, Low Bandwidth Mode, V_S = 5 V

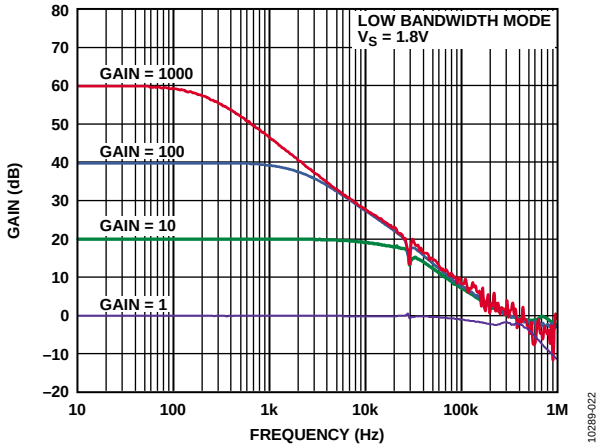


Figure 22. Gain vs. Frequency, Low Bandwidth Mode, V_S = 1.8 V

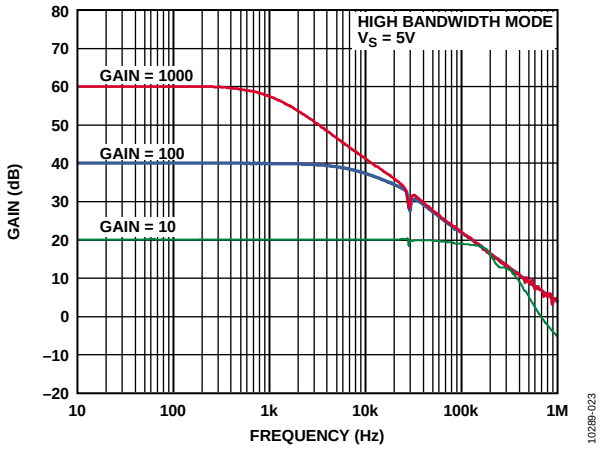


Figure 23. Gain vs. Frequency, High Bandwidth Mode, V_S = 5 V

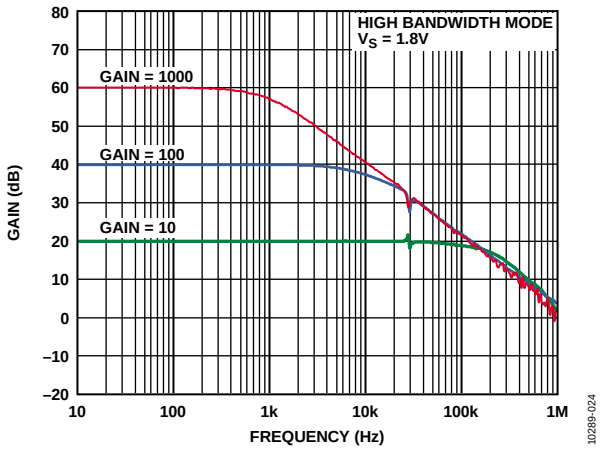


Figure 24. Gain vs. Frequency, High Bandwidth Mode, V_S = 1.8 V

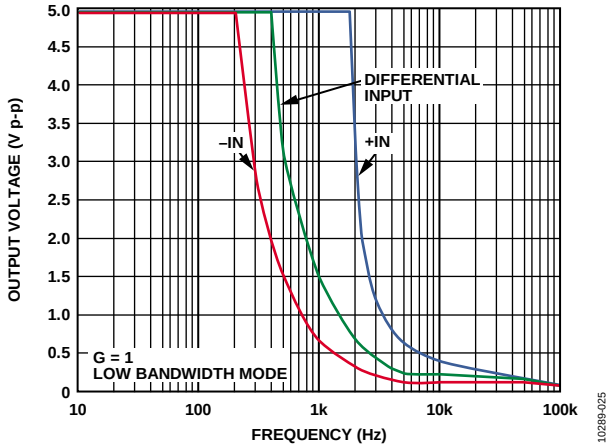


Figure 25. Large Signal Frequency Response, Low Bandwidth Mode, G = 1

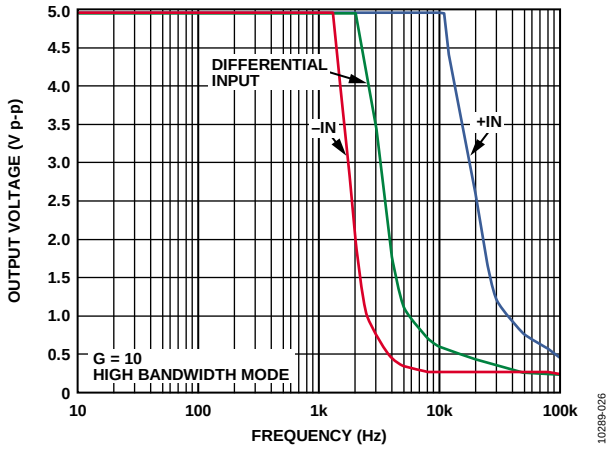


Figure 26. Large Signal Frequency Response, High Bandwidth Mode, G = 10

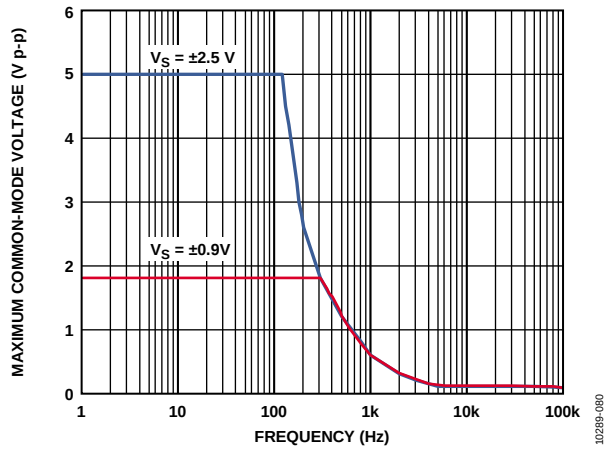


Figure 27. Maximum Common-Mode Voltage vs. Frequency

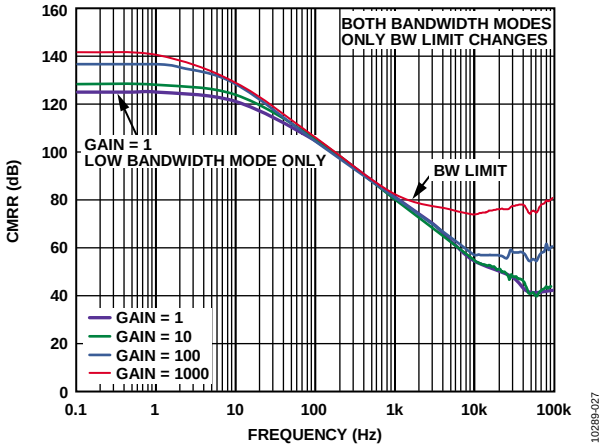


Figure 28. CMRR vs. Frequency

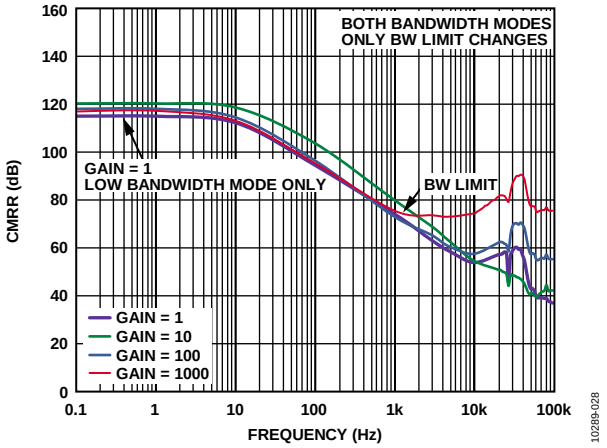


Figure 29. CMRR vs. Frequency, 1 kΩ Source Imbalance

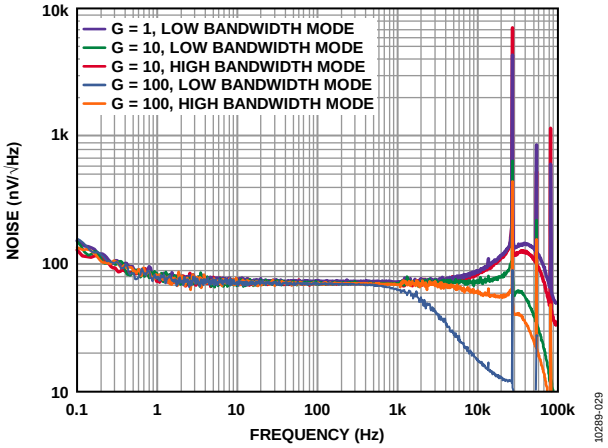


Figure 30. Voltage Noise Spectral Density vs. Frequency

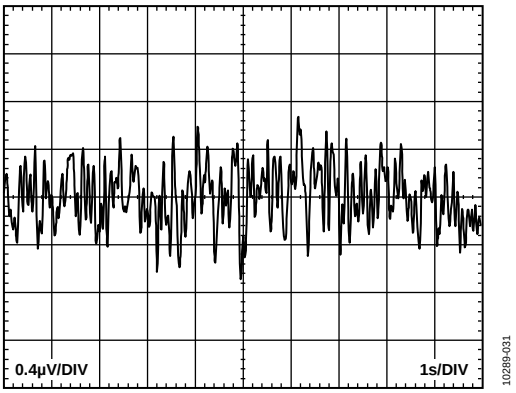


Figure 31. 0.1 Hz to 10 Hz RTI Voltage Noise

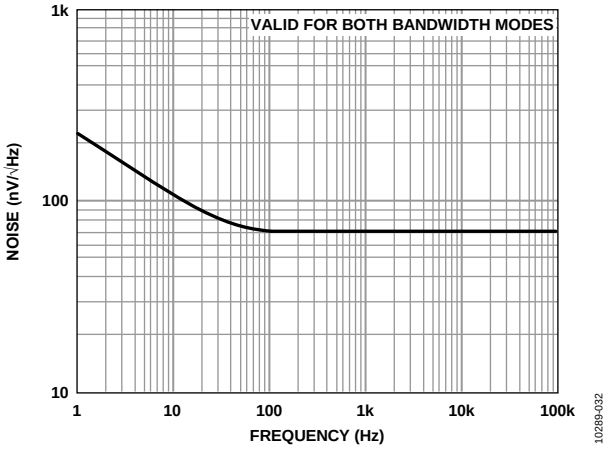


Figure 32. Current Noise Spectral Density vs. Frequency

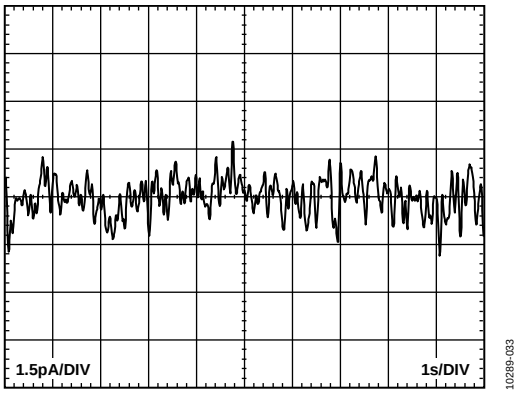


Figure 33. 0.1 Hz to 10 Hz RTI Current Noise

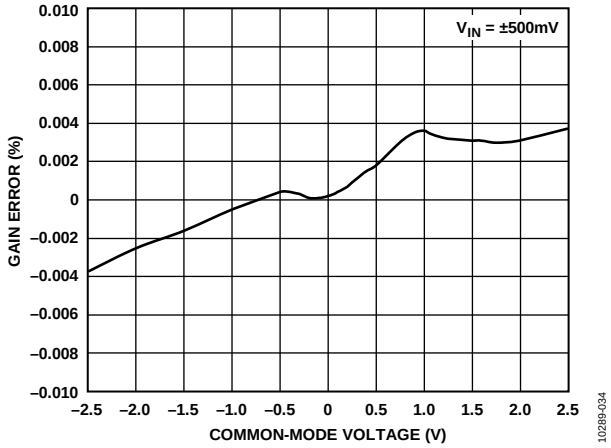


Figure 34. Gain Error vs. Common-Mode Voltage, G = 1

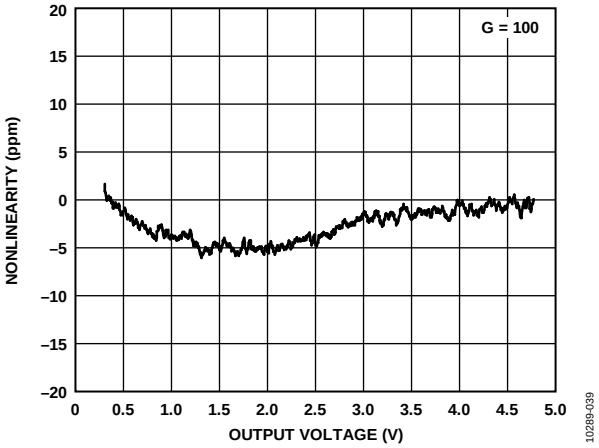


Figure 37. Gain Nonlinearity, G = 100, V_S = 5 V, R_L = 10 kΩ to Ground

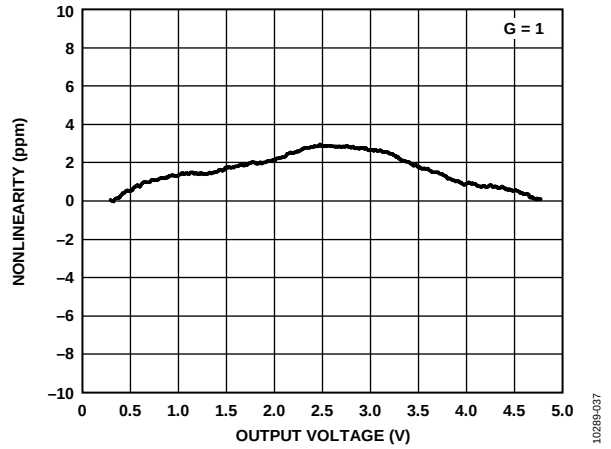


Figure 35. Gain Nonlinearity, G = 1, V_S = 5 V, R_L = 10 kΩ to Ground, Low Bandwidth Mode

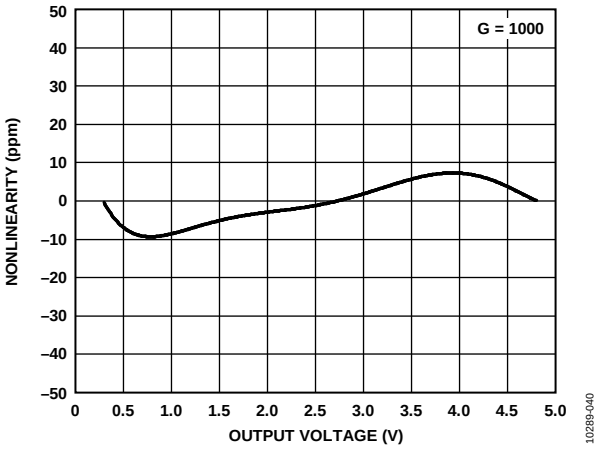


Figure 38. Gain Nonlinearity, G = 1000, V_S = 5 V, R_L = 10 kΩ to Ground

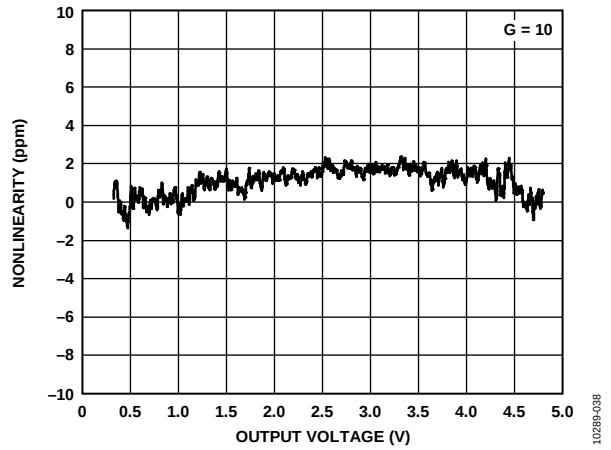


Figure 36. Gain Nonlinearity, G = 10, V_S = 5 V, R_L = 10 kΩ to Ground

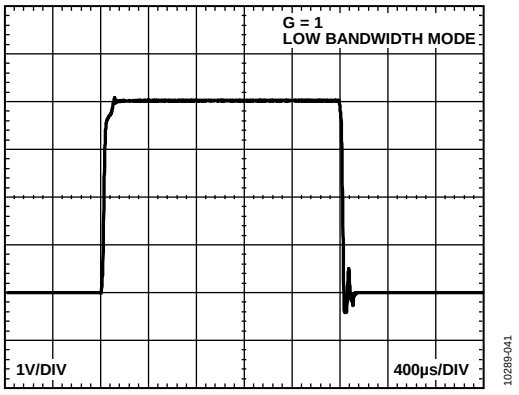


Figure 39. Large Signal Pulse Response, Low Bandwidth Mode, G = 1, R_L = 10 kΩ, C_L = 10 pF

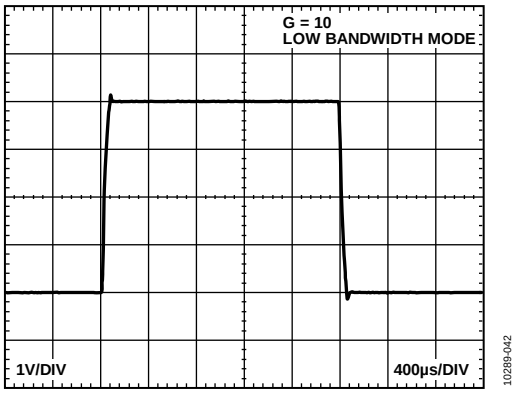


Figure 40. Large Signal Pulse Response, Low Bandwidth Mode, $G = 10$, $R_L = 10\ k\Omega$, $C_L = 10\ pF$

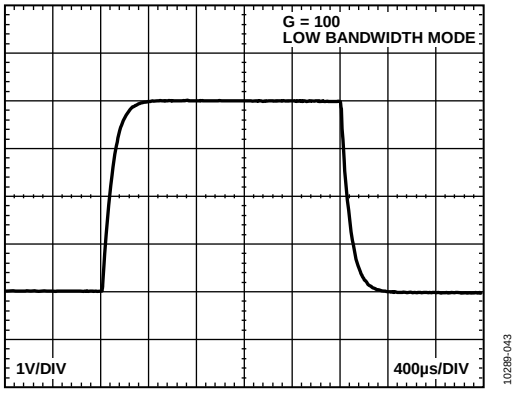


Figure 41. Large Signal Pulse Response, Low Bandwidth Mode, $G = 100$, $R_L = 10\ k\Omega$, $C_L = 10\ pF$

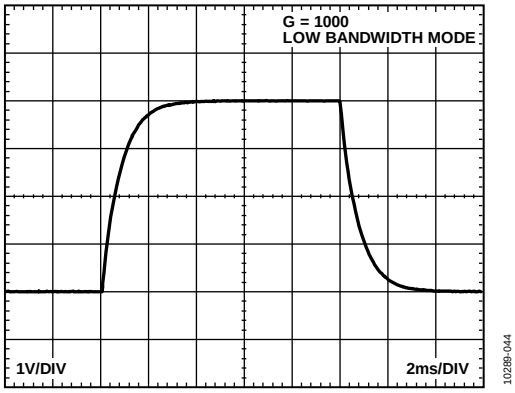


Figure 42. Large Signal Pulse Response, Low Bandwidth Mode, $G = 1000$, $R_L = 10\ k\Omega$, $C_L = 10\ pF$

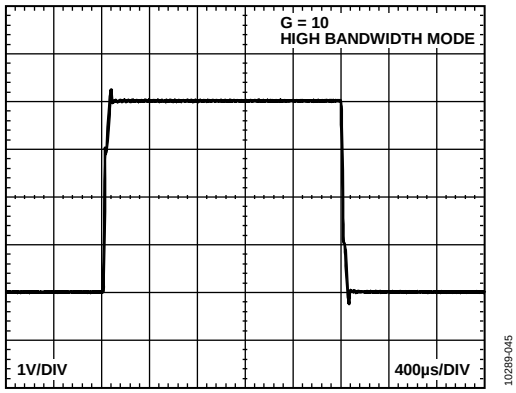


Figure 43. Large Signal Pulse Response, High Bandwidth Mode, $G = 10$, $R_L = 10\ k\Omega$, $C_L = 10\ pF$

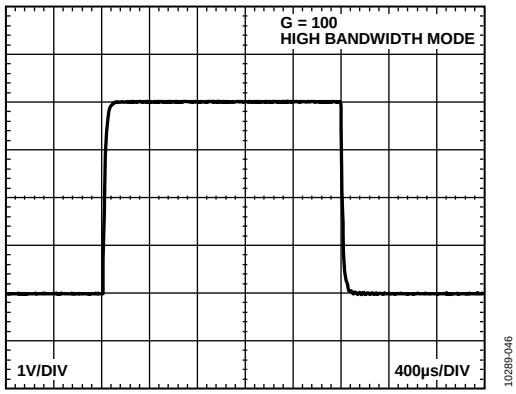


Figure 44. Large Signal Pulse Response, High Bandwidth Mode, $G = 100$, $R_L = 10\ k\Omega$, $C_L = 10\ pF$

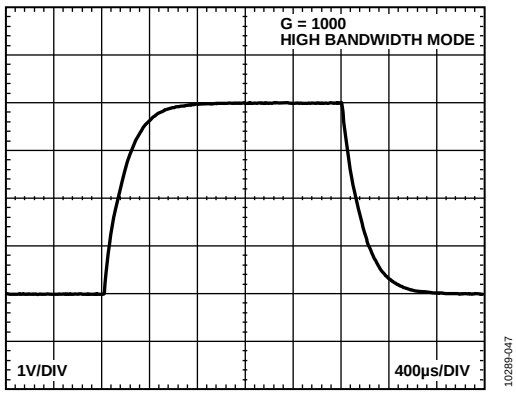


Figure 45. Large Signal Pulse Response, High Bandwidth Mode, $G = 1000$, $R_L = 10\ k\Omega$, $C_L = 10\ pF$

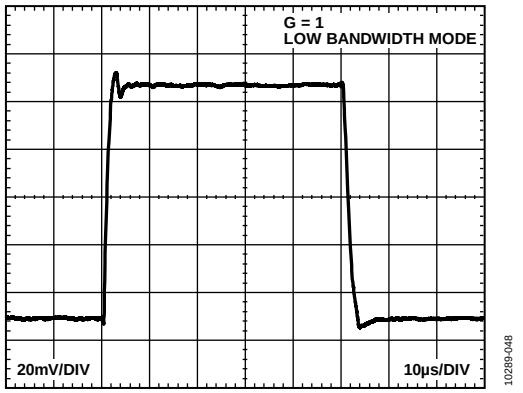


Figure 46. Small Signal Pulse Response, G = 1, R_L = 10 kΩ, C_L = 100 pF, Low Bandwidth Mode

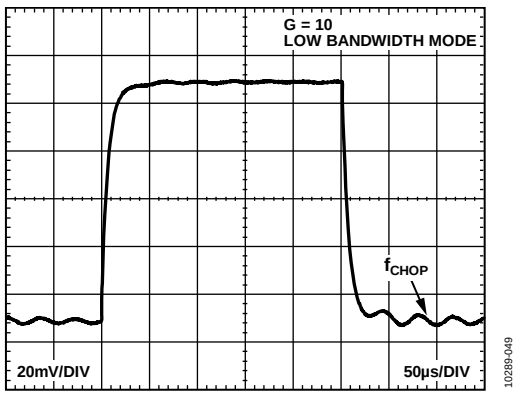


Figure 47. Small Signal Pulse Response, G = 10, R_L = 10 kΩ, C_L = 100 pF, Low Bandwidth Mode

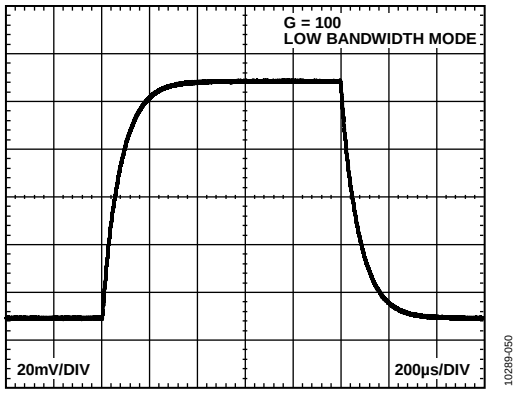


Figure 48. Small Signal Pulse Response, G = 100, R_L = 10 kΩ, C_L = 100 pF, Low Bandwidth Mode

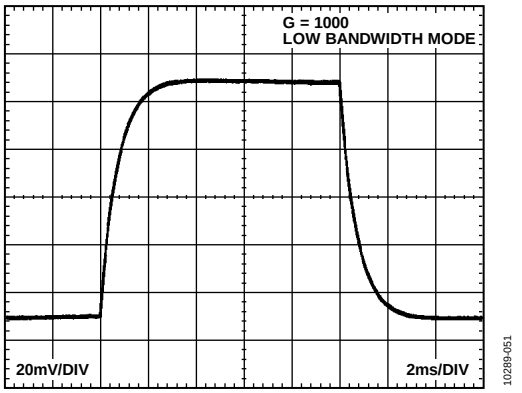


Figure 49. Small Signal Pulse Response, G = 1000, R_L = 10 kΩ, C_L = 100 pF, Low Bandwidth Mode

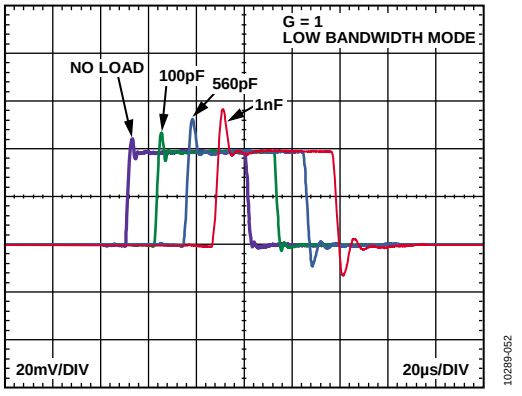


Figure 50. Small Signal Pulse Response with Various Capacitive Loads, G = 1, R_L = Infinity, Low Bandwidth Mode

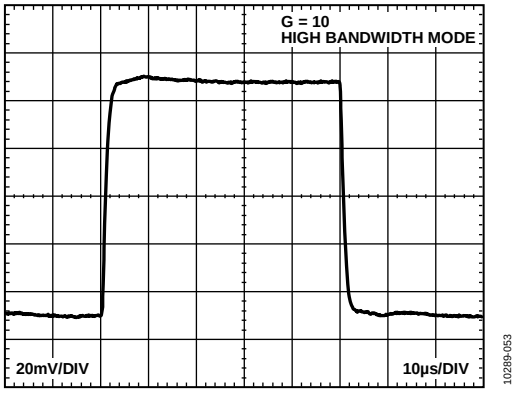


Figure 51. Small Signal Pulse Response, G = 10, R_L = 10 kΩ, C_L = 100 pF, High Bandwidth Mode

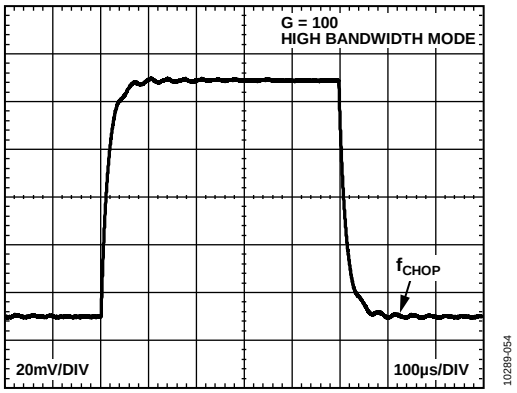


Figure 52. Small Signal Pulse Response, G = 100, R_L = 10 kΩ, C_L = 100 pF, High Bandwidth Mode

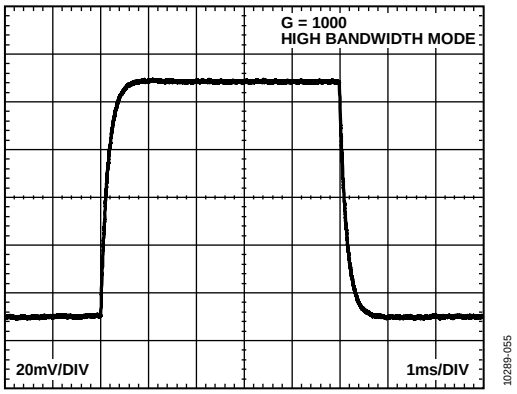


Figure 53. Small Signal Pulse Response, G = 1000, R_L = 10 kΩ, C_L = 100 pF, High Bandwidth Mode

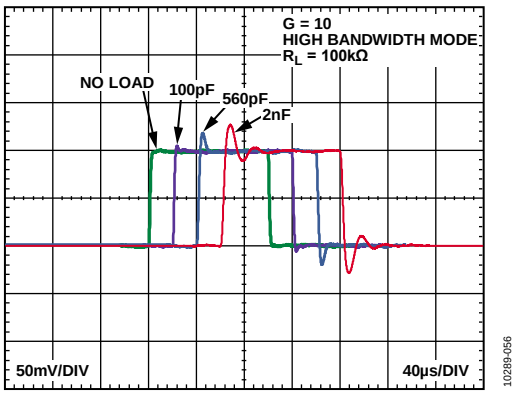


Figure 54. Small Signal Pulse Response with Various Capacitive Loads, G = 10, R_L = 100 kΩ, High Bandwidth Mode

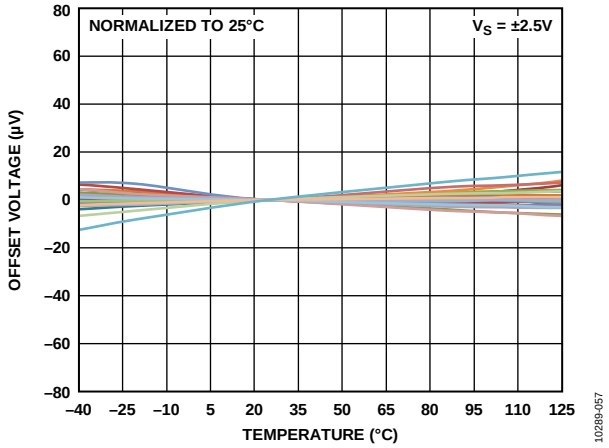


Figure 55. Offset Voltage vs. Temperature

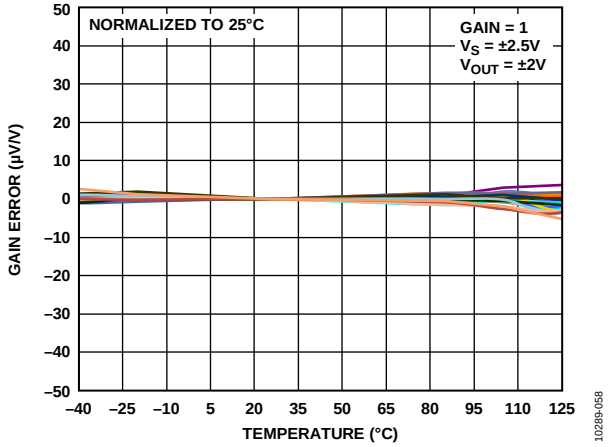


Figure 56. Gain vs. Temperature

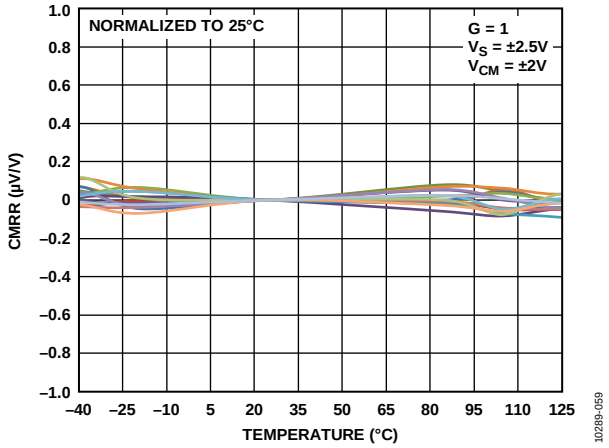


Figure 57. CMRR vs. Temperature

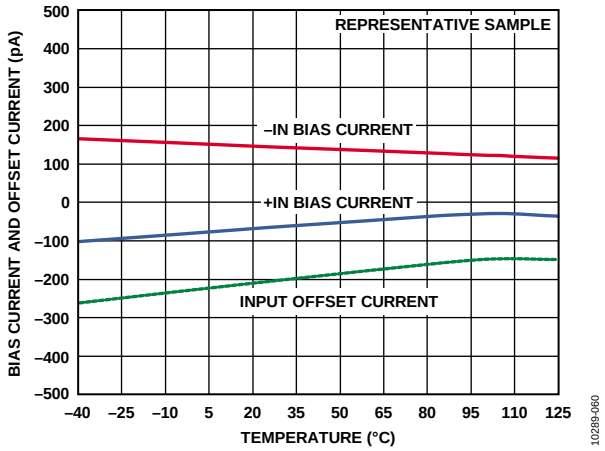


Figure 58. Input Bias Current and Input Offset Current vs. Temperature

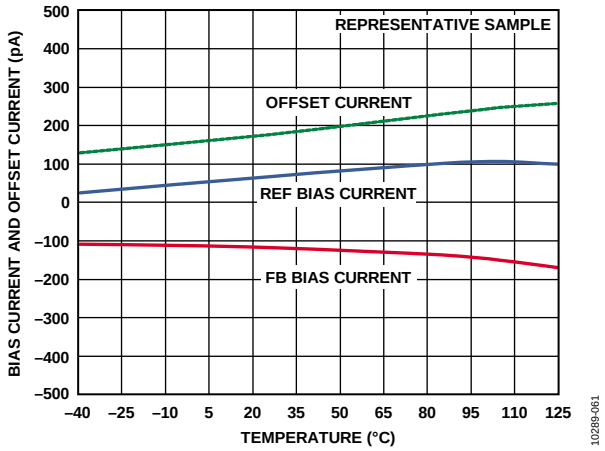


Figure 59. REF Input Bias Current, FB Input Bias Current, and Offset Current vs. Temperature

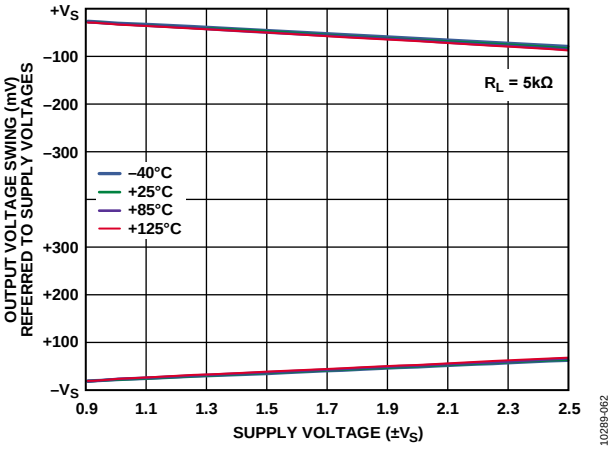


Figure 60. Output Voltage Swing vs. Supply Voltage

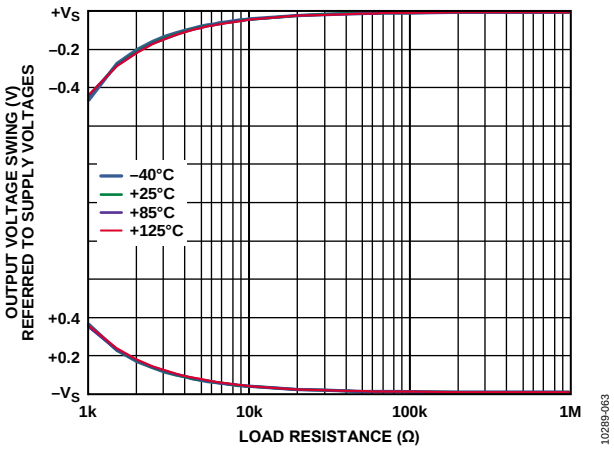


Figure 61. Output Voltage Swing vs. Load Resistance, V_S = ±2.5 V

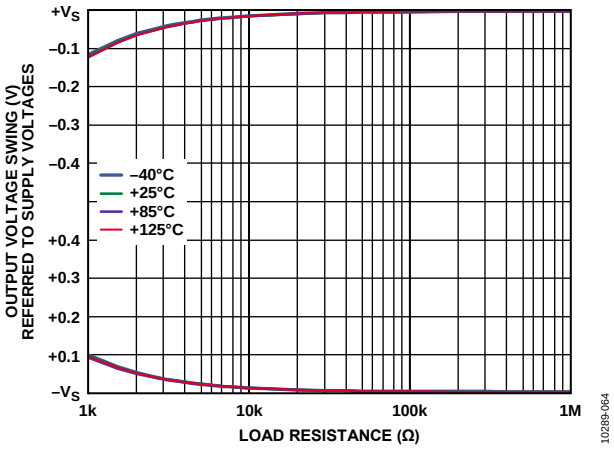


Figure 62. Output Voltage Swing vs. Load Resistance, V_S = ±0.9 V

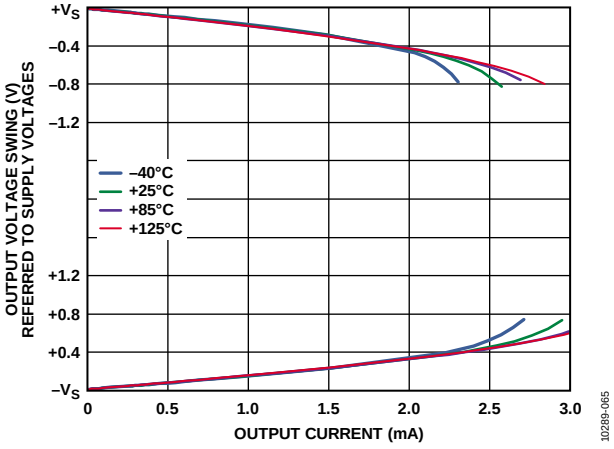


Figure 63. Output Voltage Swing vs. Output Current

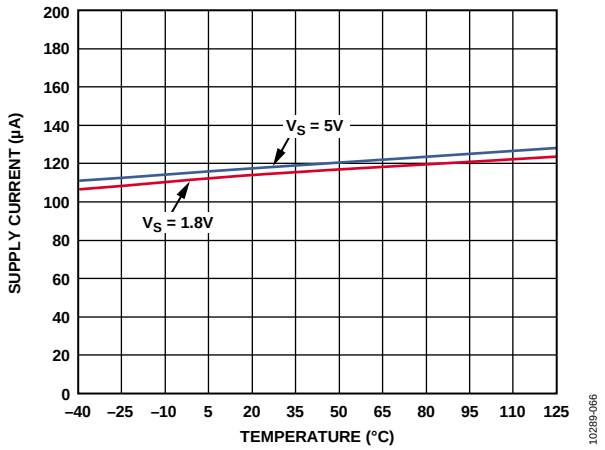


Figure 64. Supply Current vs. Temperature, V_S = 5 V, V_S = 1.8 V

THEORY OF OPERATION

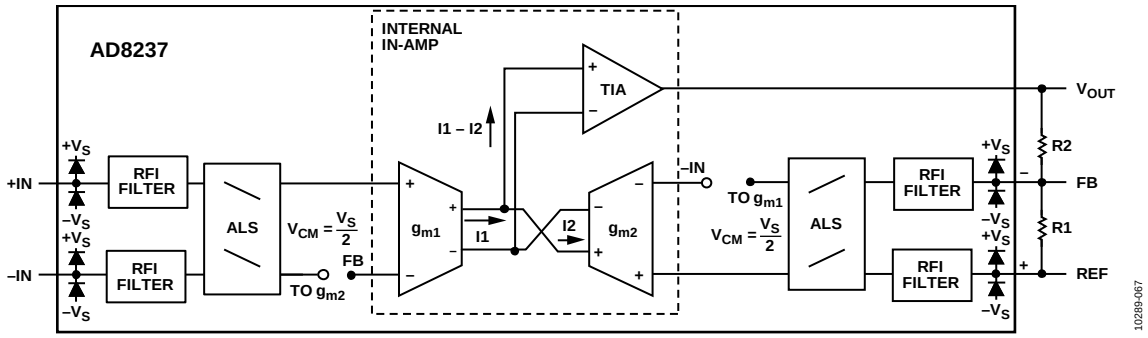


Figure 65. Simplified Schematic

ARCHITECTURE

The AD8237 is based on an indirect current feedback topology consisting of three amplifiers: two matched transconductance amplifiers that convert voltage to current, and one transimpedance amplifier, TIA, that converts current to voltage.

To understand how the AD8237 works, first consider only the internal in-amp. Assume a positive differential voltage is applied across the inputs of the transconductance amplifier, g_{m1}. This input voltage is converted into a differential current, I1, by the g_m. Initially, I2 is zero; therefore, I1 is fed into the TIA, causing the output to increase. If there is feedback from the output of the TIA to the negative terminal of g_{m2}, and the positive terminal is held constant, the increasing output of the TIA causes I2, as shown, to increase. When it is assumed that the TIA has infinite gain, the loop is satisfied when I2 equals I1. Because the gain of g_{m1} and g_{m2} are matched, this means that the differential input voltage across g_m1 appears across the inputs of g_{m2}. This behavioral model is all that is needed for proper operation of the AD8237, and the rest of the circuit is for performance optimization.

The AD8237 employs a novel adaptive level shift (ALS) technique. This switched capacitor method shifts the common-mode level of the input signal to the optimal level for the in-amp while preserving the differential signal. Once this is accomplished, additional performance benefits can be achieved by using the internal in-amp to compare +IN to FB and −IN to REF. This is only practical because the signals emitting from the ALS blocks are all referred to the same common-mode potential.

In traditional instrumentation amplifiers, the input common-mode voltage can limit the available output swing, typically depicted in a hexagon plot of the input common-mode vs. the output voltage. Because of this limit, very few instrumentation amplifiers can measure small signals near either supply rail. Using the indirect current feedback topology and ALS, the AD8237 achieves a truly rail-to-rail characteristic. This increases power efficiency in many applications by allowing for power supply reduction.

The AD8237 includes an RFI filter to remove high frequency out-of-band signals without affecting input impedance and CMRR over frequency. Additionally, there is a bandwidth mode pin to adjust the compensation. For gains greater than or equal to 10, the bandwidth mode pin (BW) can be tied to $+V_S$ to change the compensation and increase the gain bandwidth product of the amplifier to 1 MHz. Otherwise, connect BW to $-V_S$ for a 200 kHz gain bandwidth product.

SETTING THE GAIN

There are several ways to configure the AD8237. The transfer function of the AD8237 in the configuration in Figure 65 is

$$V_{OUT} = G(V_{+IN} - V_{-IN}) + V_{REF}$$

where:

$$G = 1 + \frac{R2}{R1}$$

Table 7. Suggested Resistors for Various Gains (1% Resistors)

R1 (kΩ)	R2 (kΩ)	Gain
None	Short	1.00
49.9	49.9	2.00
20	80.6	5.03
10	90.9	10.09
5	95.3	20.06
2	97.6	49.8
1	100	101
1	200	201
1	499	500
1	1000	1001

Whereas the ratio of R2 to R1 sets the gain, the designer determines the absolute value of the resistors. Larger values reduce power consumption and output loading; smaller values limit the FB input bias current and input impedance errors. If the parallel combination of R1 and R2 is greater than about 30 kΩ, the resistors start to contribute to the noise. For best output swing and linearity, keep $(R1 + R2) \parallel R_L \geq 10\ k\Omega$.

The bias current at the FB pin is dependent on the common-mode and differential input impedance. FB bias current errors from the common-mode input impedance can be reduced by placing a resistor value of R1||R2 in series with the REF terminal, as shown in Figure 66. At higher gains, this resistor can simply be the same value as R1.

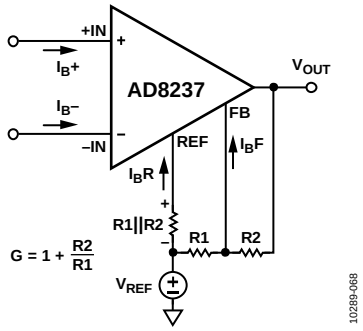


Figure 66. Canceling Error from FB Input Bias Current

Some applications may be able to take advantage of the symmetry of the input transconductance amplifiers by canceling the differential input impedance errors, as shown in Figure 67. If the source resistance is well known, setting the parallel combination of R1 and R2 equal to R_S accomplishes this. If practical resistor values force the parallel combination of R1 and R2 to be less than R_S, add a series resistor to the FB input to make up for the difference.

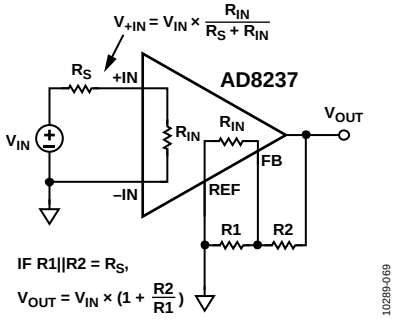


Figure 67. Canceling Input Impedance Errors

GAIN ACCURACY

Unlike most instrumentation amplifiers, the relative match of the two gain setting resistors determines the gain accuracy of the AD8237 rather than a single external resistor. For example, if two resistors have exactly the same absolute error, there is no error in gain. Conversely, two 1% resistors can cause approximately 2% maximum gain error at high gains. Temperature coefficient mismatch of the gain setting resistors increases the gain drift of the instrumentation amplifier circuit according to the gain equation. Because these external resistors do not have to match any on-chip resistors, resistors with good TCR tracking can achieve excellent gain drift without the need for a low absolute TCR.

For the best performance, keep the two input pairs (+IN and –IN, and FB and REF) at similar dc and ac common-mode potentials. This has two benefits. For dc common-mode, this minimizes the gain error of the AD8237. For ac common-mode, this yields improved frequency response. There is a maximum rate at which the ALS circuit can shift the common-mode voltage, which is shown in Figure 27. Because of this limit, the best large signal frequency response is achieved when the ac common-mode voltage of the two input pairs are matched. For example, if the negative input is at a fixed voltage and the positive input is driven with a signal, the feedback input moves with the positive input; therefore, the ac common-mode voltage of the two input pairs is the same. The effect of this is shown in Figure 25 and Figure 26.

CLOCK FEEDTHROUGH

The AD8237 uses nonoverlapping clocks to perform the chopping and ALS functions. The input voltage-to-current amplifiers are chopped at approximately 27 kHz.

Although there is internal ripple-suppression circuitry, trace amounts of these clock frequencies and their harmonics can be observed at the output in some configurations. These ripples are typically 100 µV RTI when the bandwidth is greater than the clock frequency. They can be larger after a transient pulse but settle back to nominal, which is included in the settling time specifications. The amount of feedthrough at the output is dependent upon the gain and bandwidth mode. The worst case is in high bandwidth mode when the gain can be almost 40 before the clock ripple is outside the bandwidth of the amplifier. For some applications, it may be necessary to use additional filtering after the AD8237 to remove this ripple.

INPUT VOLTAGE RANGE

The allowable input range of the AD8237 is much simpler than traditional architectures. For the transfer function of the AD8237 to be valid, the input voltage must follow two rules

- Keep the differential input voltage within the limits shown in Figure 14; approximately ±(Total Supply Voltage – 1.2) V.
- Keep the voltage of the inputs (including the REF and FB pins) and the output within the specified voltage range, which are approximately the supply rails.

Because the output swing is completely independent of the input common-mode voltage, there are no hexagonal figures or complicated formulas to follow, and no limitation for the output swing the amplifier has for input signals with changing common mode.

INPUT PROTECTION

If no external protection is used, keep the inputs of the AD8237 within the voltages specified in the absolute maximum ratings. If the application requires voltages beyond these ratings, input protection resistors can be placed in series with the inputs of the AD8237 to limit the current to 5 mA. For example, if $+V_S$ is 3 V and a 10 V overload voltage can occur at the inputs, place a protection resistor of at least (10 V − 3 V)/5 mA = 1.4 kΩ in series with the inputs.

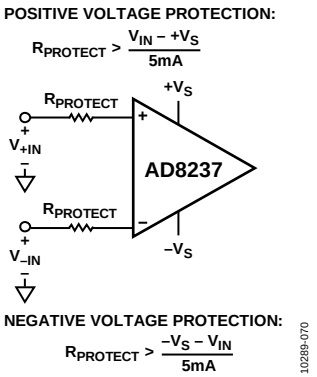


Figure 68. Protection Resistors for Large Input Voltages

FILTERING RADIO FREQUENCY INTERFERENCE

The AD8237 contains an on-chip RFI filter that is sufficient for a majority of applications. For applications where additional radio frequency immunity is needed, an external RFI filter can also be applied as shown in Figure 69.

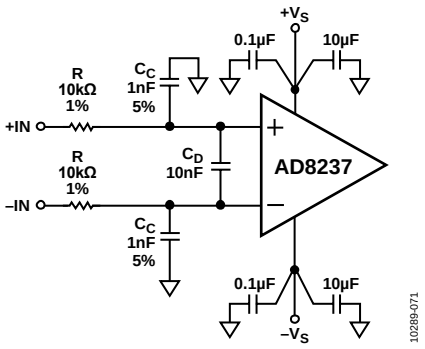


Figure 69. Adding Extra RFI Filtering

USING THE REFERENCE PIN

In general, instrumentation amplifier reference pins can be useful for a few reasons. They provide a means of physically separating the input and output grounds to reject ground bounce common to the inputs. They can also be used to precisely level shift the output signal. In the configuration shown in Figure 65 through Figure 67, the gain of the reference pin to the output is unity, as is common in a typical in-amp. Because the reference pin is functionally no different from the positive input, it can be used with gain, as shown in Figure 70.

This configuration can be very useful in certain cases, such as dc removal servo loops, which typically use an inverting integrator to drive REF and compensate for a dc offset. This requires special attention to the input range (especially at REF) and the output range. All three input voltages are referred to the one ground shown, which may need to be a low impedance midsupply.

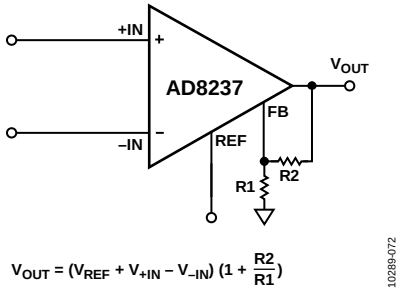


Figure 70. Applying Gain to the Reference Voltage

Traditional instrumentation amplifier architectures require the reference pin to be driven with a low impedance source. In these traditional architectures, impedance at the reference pin degrades both CMRR and gain accuracy. With the AD8237 architecture, resistance at the reference pin has no effect on CMRR.

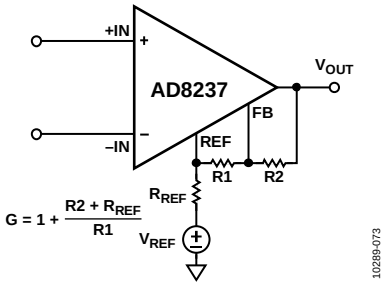


Figure 71. Calculating Gain with Reference Resistance

Resistance at the reference pin does affect the gain of the AD8237; however, if this resistance is constant, the gain setting resistors can be adjusted to compensate. For example, the AD8237 can be driven with a voltage divider, as shown in Figure 72.

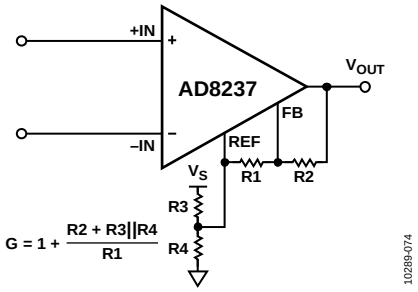


Figure 72. Using Voltage Divider to Set Reference Voltage

LAYOUT

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signal to be converted to a differential signal before reaching the in-amp. This conversion can occur when the path to the positive input pin has a different frequency response than the path to the negative input pin. For best CMRR vs. frequency performance, closely match the impedance of each path. Place additional source resistance in the input path (for example, for input protection) close to the in-amp inputs to minimize interaction between the resistors and the parasitic capacitance from the printed circuit board (PCB) traces.

Power Supplies

Use a stable dc voltage to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. For more information, see the PSRR performance curves in Figure 17 through Figure 20.

Place a 0.1 µF capacitor as close as possible to each supply pin. As shown in Figure 73, a 10 µF tantalum capacitor can be used farther away from the part. This capacitor, which is intended to be effective at low frequencies, can usually be shared by other precision integrated circuits. Keep the traces between these integrated circuits short to minimize interaction of the trace parasitic inductance with the shared capacitor. If a single supply is used, decoupling capacitors at $-V_S$ can be omitted.

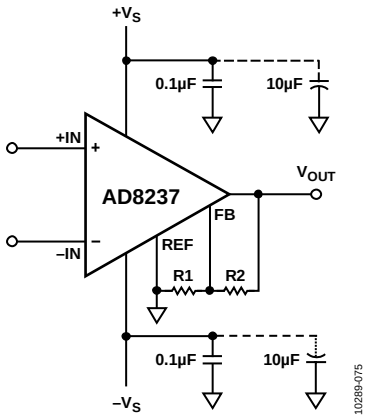


Figure 73. Supply Decoupling, REF, and Output Referred to Local Ground

Reference

The output voltage of the AD8237 is developed with respect to the potential on the reference terminal. Take care to tie REF to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8237 must have a return path to ground. When the source, such as a thermocouple, cannot provide a return current path, create one, as shown in Figure 74.

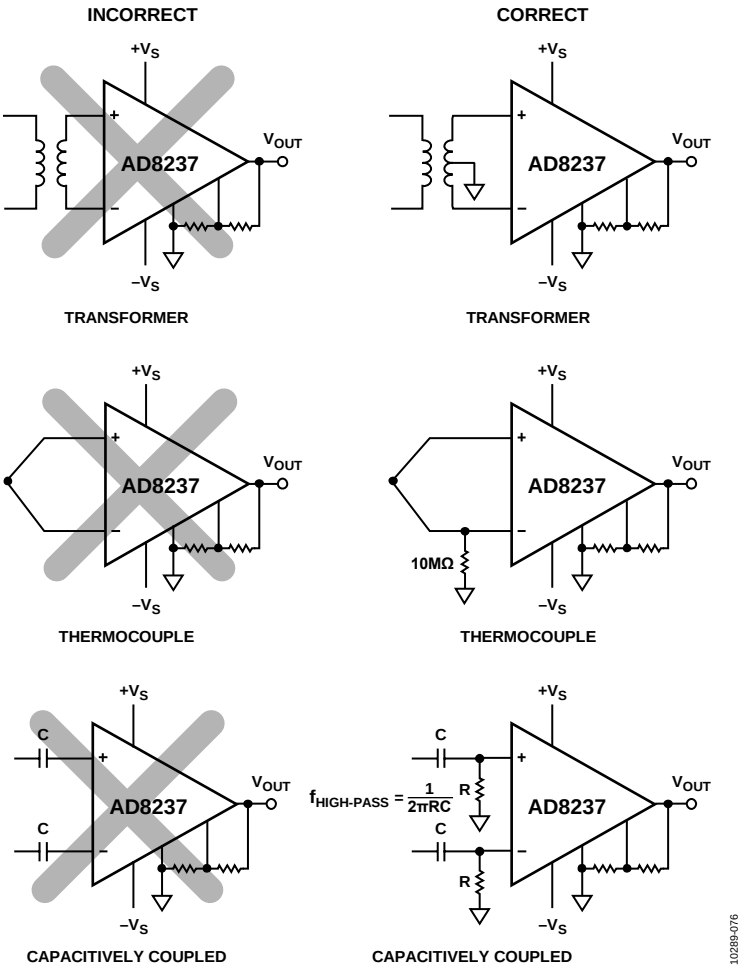


Figure 74. Creating an I_{BIAS} Path

APPLICATIONS INFORMATION

BATTERY CURRENT MONITOR

The micropower current consumption, unique topology, and rail-to-rail input of the AD8237 make it ideal for battery-powered current sensing applications. When configured as shown in Figure 75, the AD8237 is able to obtain an accurate high-side current measurement for both charging and discharging. Depending on the nature of the load, $+V_S$ may require RC decoupling. Use Kelvin sensing methods to achieve the most accurate results.

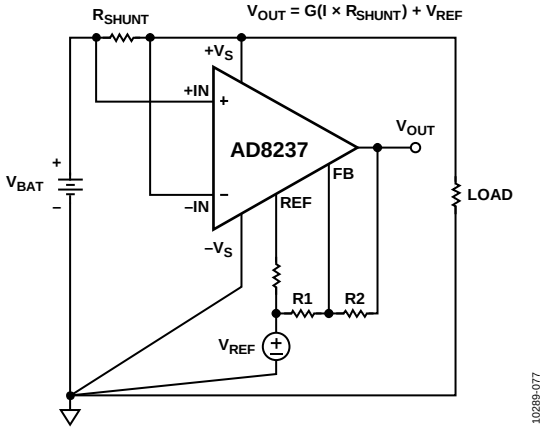


Figure 75. Battery-Powered Current Sense

PROGRAMMABLE GAIN IN-AMP

Most integrated circuit instrumentation amplifiers use a single resistor to set the gain, which is in a low impedance path. Any component placed between the gain setting pins has current flowing through it, which adds to the gain resistance. Typical CMOS switches have on resistance, R_{ON}. R_{ON} is not well controlled, is nonlinear with input voltage, and has high drift. This creates large gain errors and distortion at the output of the in-amp. This R_{ON} problem has made it difficult to build a precision programmable gain in-amp in the past. With the AD8237 topology, the switches can be placed in a high impedance sense path, eliminating the parasitic resistance effects. Figure 76 shows one way to accomplish programmable gain. Some applications may benefit from using a digital potentiometer instead of a multiplexer.

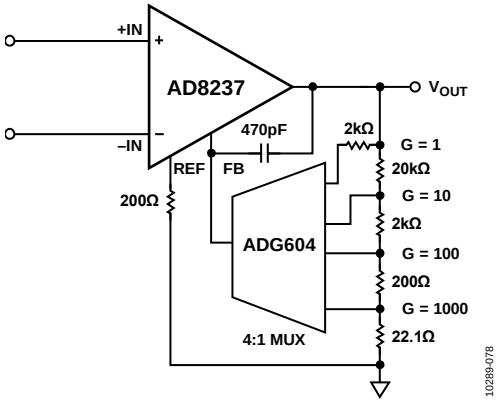


Figure 76. Programmable Gain with a Multiplexer

AD8237 IN AN ECG FRONT END

Electrocardiogram (ECG) circuits must operate with a differential dc offset due to the half-cell potential of the electrodes. The tolerance for this over potential is typically ±300 mV; however, it can be a volt or more in some situations. As ECG circuits move to lower supply voltages, the half-cell potential problem becomes more difficult, strictly limiting the gain that can be applied in the first stage. The AD8237 architecture provides a unique solution to this problem. If the REF pin is left unconnected to the gain setting network, a low frequency inverting integrator can be connected from the output to the REF pin. Because the AD8237 applies gain to the integrator output, the integrator only has to swing as far as the dc offset to compensate for it, rather than the dc offset multiplied by the gain. With this system architecture, large gains can be applied at the in-amp stage, and the requirements of the rest of the system can be greatly reduced. This also reduces noise and offset error contributions from devices after the in-amp in the signal path. The circuit in Figure 77 illustrates the core concept. Additional op amps can be added for improved performance, such as input buffering, filtering, and driven lead, if it is required by the system. Proper decoupling is not shown.

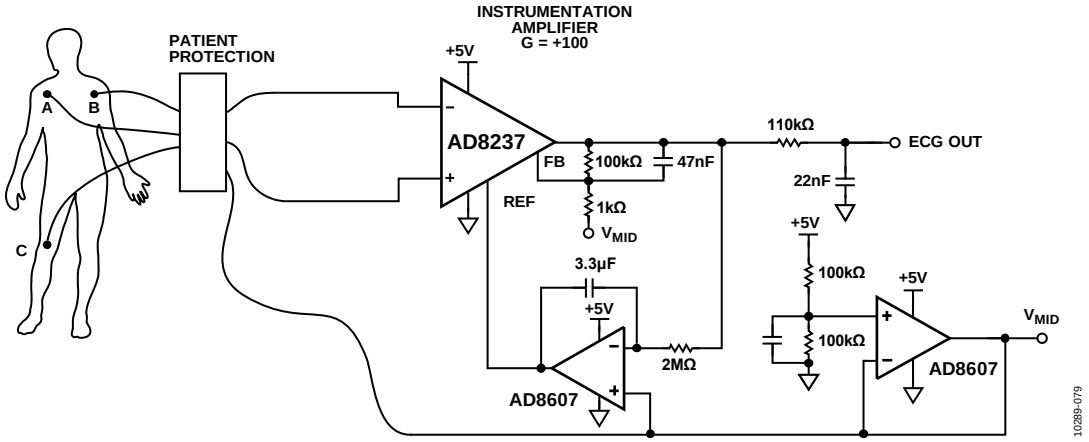
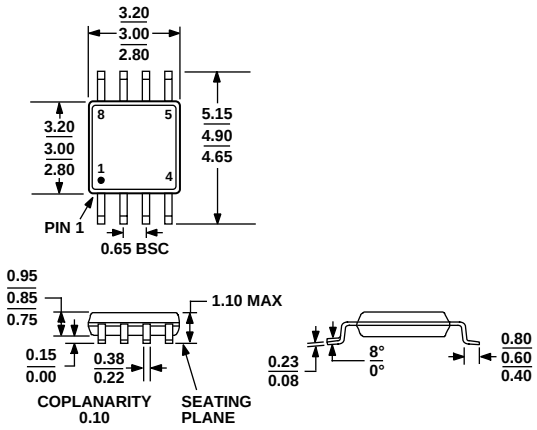


Figure 77. AD8237 in ECG

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 78. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package	Branding
AD8237ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP], Tube	RM-8	Y4H
AD8237ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP], 7-Inch Tape and Reel	RM-8	Y4H
AD8237ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP], 13-Inch Tape and Reel	RM-8	Y4H

[1] Z = RoHS Compliant Part.

NOTES

单击下面可查看定价，库存，交付和生命周期等信息

>>Analog Devices(亚德诺)