ANSILIC

ASP4644 Datasheet

Quad DCDC µModule Regulator with 16A Output Array

Table of Contents

1 Abstract

1.1 Features

Quad Output Step-Down Regulator with 4A per Output

Input voltage range : 4V to 14V

Output voltage range : 0.6V to 5.5V

Output Current : 4A DC,5A Peak Output Current Each Channel

Typical output ripple : 4.5mV

Current Mode Control, Fast Transient Response

Output Voltage Tracking

External Frequency Synchronization

AEC-Q100 Grade1 automotive certification (Automotive grade)

SEU ≥ 75Mev.cm^2/mg or 10^{-5} times/device.day (Commercial aerospace grade)

SEL ≥ 75Mev.cm^2/mg (Commercial aerospace grade)

Overvoltage, Current and Temperature Protection

Output current balance

Package: BGA77 (9mm*15mm*4.46mm)

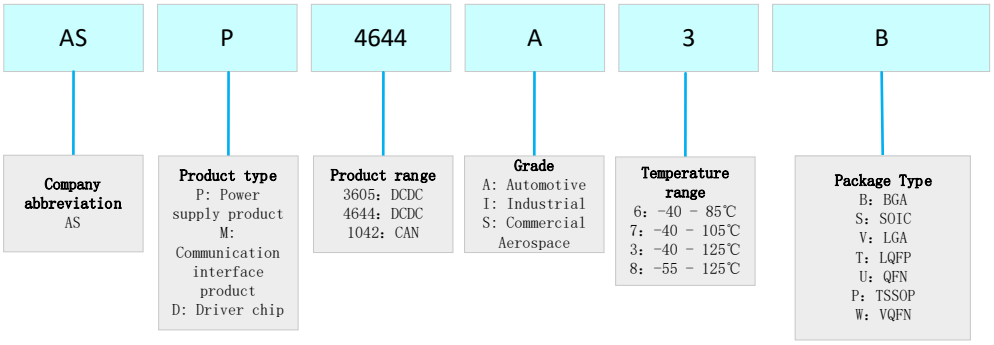
1.2 Description

The ASP4644 is a quad DCDC step-down µModule regulator with 4A per output. Outputs can be paralleled in an array for up to 16A capability. Included in the package are the switching controllers, power FETs, inductors and support components. Operating over an input voltage range of 4V to 14V with an external bias supply, the ASP4644 supports an output voltage range of 0.6V to 5.5V. Its high efficiency design delivers 4A continuous (5A peak) output current per channel. Only bulk input and output capacitors are needed.

1.3 Product Series

DEVICE	GRADE	TEMPERATURE RANGE	FEATURE
ASP4644I6B	Industrial	-40 to 85 °C	Industrial application
ASP4644A3B	Automotive	-40 to 125 °C	Automotive certification
ASP4644S8B	Commercial aerospace	-55 to 125 °C	Automotive certification Radiation-resistant design

芯片命名规则



1.4 Applications

Load-side power supplies

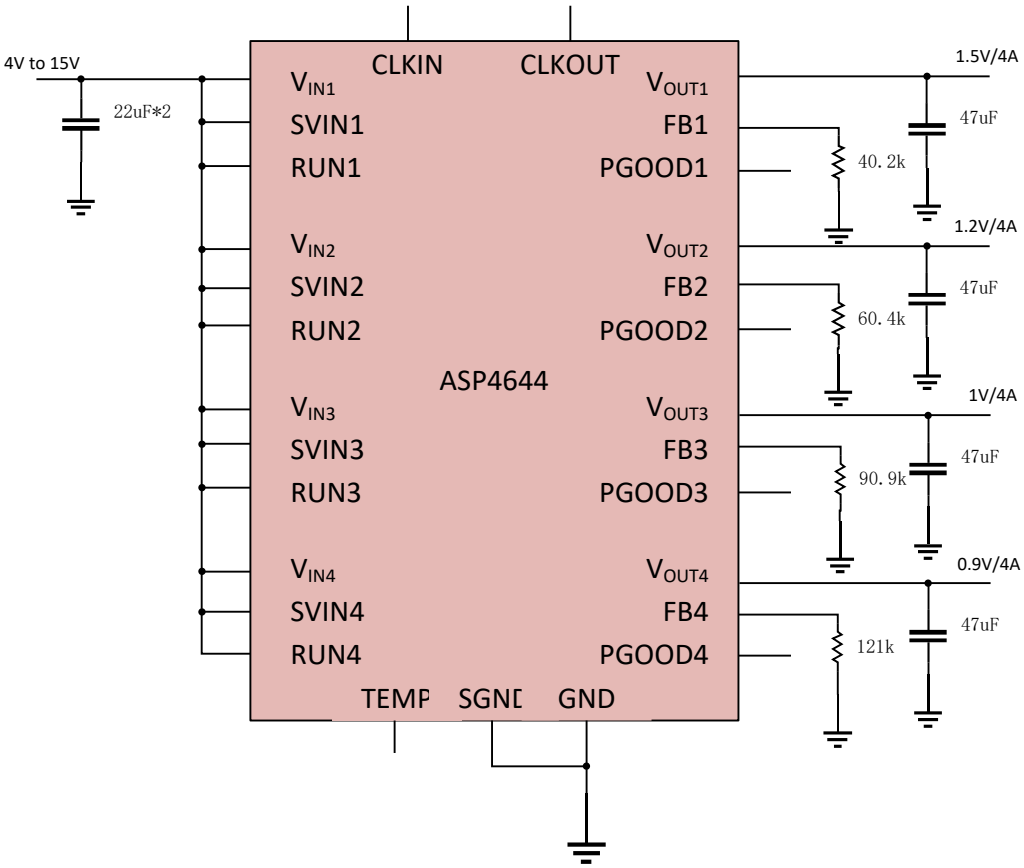
Portable instruments

Distributed power systems

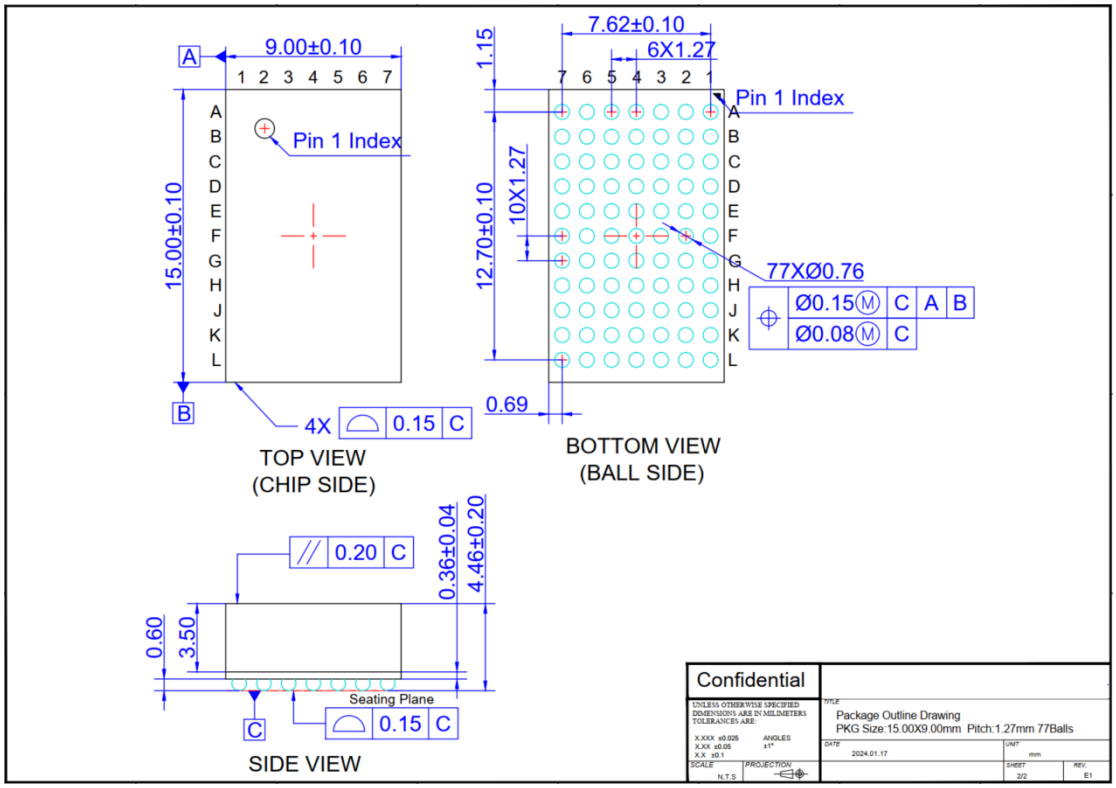
Battery-powered equipment

1.5 Typical Application

4V to 14V Input, Quad 0.9V, 1V, 1.2V and 1.5V Output DCDC/ Step-Down Regulator



1.6 Package Description



2 CHARACTERISTICS

2.1 Absolute Maximum Ratings

V_{IN}, SV_{IN} (Per Channel)：–0.3V ~ 15V

$INTV_{CC}$ (Per Channel)：–0.3V ~ 3.6V

RUN (Per Channel)：–0.3V ~ 15V

CLKOUT,CLKIN (Per Channel)：–0.3V ~ $INTV_{CC}$

PGOOD,MODE,TRACK/SS, FB (Per Channel)：–0.3V ~ $INTV_{CC}$

Internal Operating Temperature Range：–40°C ~ 125°C

Storage Temperature Range：–65°C ~ 125°C

NOTE1： ASP4644 operates reliably within an internal temperature range of 0°C to 125°C. It's crucial to consider that the maximum ambient temperature meeting these specifications varies based on specific operating conditions, PCB layout, rated package thermal resistance, and other environmental factors.

NOTE2： The circuit incorporates over-temperature protection to safeguard the equipment during momentary overload conditions. If the junction temperature exceeds 135°C, this protection activates to prevent potential reliability issues that may result from prolonged operation at high temperatures.

NOTE3： Running the chip beyond its absolute maximum ratings could permanently damage the equipment. Extended operation at or near these limits may affect the device's reliability and longevity.

2.2 Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}, SV_{IN}	Input DC Voltage	$SV_{IN}=V_{IN}$	4		14	V
$V_{OUT(RANGE)}$	Ouput Voltage		0.6		5.5	V
$V_{OUT(DC)}$	Output Voltage,Total Variation with Line and Load	C_{IN}=22uF&68uF, C_{OUT}=94uF Ceramic MODE= INTV_{CC},V_{IN} = 4V to 14V, I_{OUT} = 0A to 4A ,$R_{FB(BOT)}$ = 40.2k	1.47	1.5	1.53	V

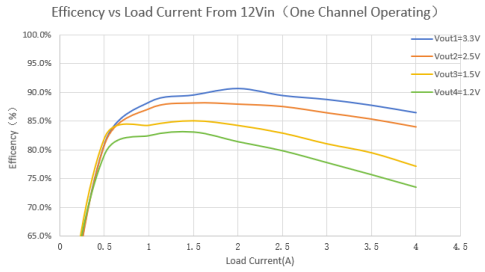
V_{RUN}	RUN Pin On Threshold			1.2		V
I_Q	Input Supply Bias Current	MODE=INTV$_{CC}$ MODE=GND Shutdown,Run=GND		5 14 220		mA mA uA
Is	Input Supply Current	V_{IN}=12V,V_{OUT}=1.5V,I_{OUT}=4A		0.64		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN}=12V,V_{OUT}=1.5V	0		4	A
△V_{OUT}/V_{OUT}	Line Regulation Accuracy	V_{OUT}=1.5V,V_{IN}=4V to 14V, No Load		0.03		%
△V_{OUT}/V_{OUT}	Load Regulation Accuracy	V_{IN}=12V，V_{OUT}=1.5V, I_{Load}=0 to 4A		0.4		%
$V_{OUT(AC)}$	Output Ripple Voltage	V_{IN}=5V，V_{OUT}=1.2V，I_{Load}=2A Cin=22uF&68uF, Cout=47uF x2 Ceramic		4.5		mV
△ V_{OUT}（START）	Turn-On Overshoot	V_{IN}=12V , V_{OUT}=1.5V , I_{Load}=0A Cout=47uF x2 Ceramic		30		mV
T_{START}	Turn-On Time	V_{IN}=12V , V_{OUT}=1.5V , I_{Load}=0A Cout=47uF x2 Ceramic,TRACK/SS=0.1uF		30.9		ms

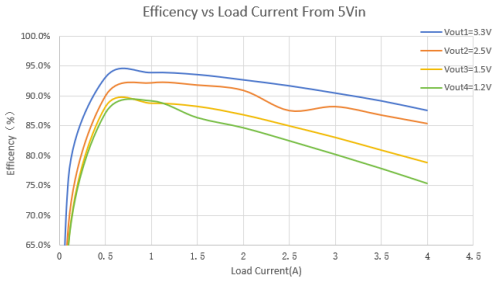
$\Delta V_{OUT\ (VPP)}$	Peak Deviation for Dynamic Load	负载:0A-2A-0A, Cout=47uF x2 V_{IN}=12V , V_{OUT}=1.5V		145		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	负载:0A-2A-0A, Cout=47uF x2 V_{IN}=12V , V_{OUT}=1.5V		5ms		ms
I_{OUTPK}	Settling Time for Dynamic Load Step	V_{IN}=12V , V_{OUT}=1.5V		8		A
V_{FB}	Voltage at FB Pin	V_{IN}=5V~14V V_{OUT}=1.2V/1.5V/2.5V/3.3V 空载		0.6		V
R_{FBHI}	Resistor Between V_{OUT} and FB Pins			60.4		kΩ
$I_{TRACK/SS}$	Resistor Between V_{OUT} and FB Pins	TRACK=0V		2.5		uA

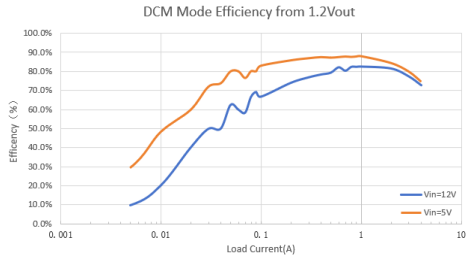
$T_{ON\ (MIN)}$	Minimum On-Time			40		ns
$T_{OFF\ (MIN)}$	Minimum On-Time			70		ns
OV	Output Overvoltage PGOOD Upper Threshold	V_{FB} Rising	5	8	11	%
UV	Output Overvoltage PGOOD Lower Threshold	V_{FB} Falling	-13	-10	-7	%
I_{PGOOD}	PGOOD Leakage			32		uA
V_{PGL}	PGOOD Voltage Low	I_{PGOOD}=1mA		0.02	0.1	V
V_{INTVCC}	Internal V_{CC} Voltage	SV_{IN}=4V to 14V	3.2	3.3	3.4	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulaion	Icc=0mA to 20mA		0.8		%
f_{OSC}	Oscillator	RT = 162k		0.84		MHz

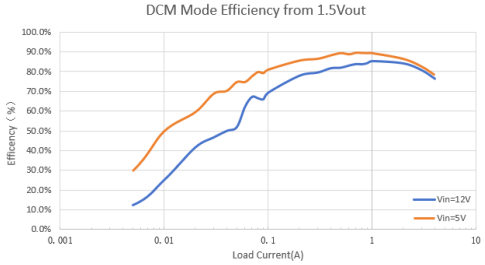
	Frequency					
CLKIN	CLKIN Threshold			0.7		V

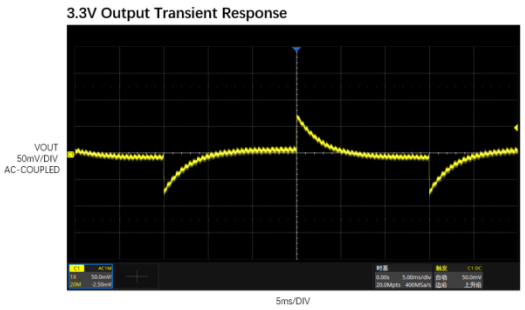
2.3 Typical Performance Characteristics



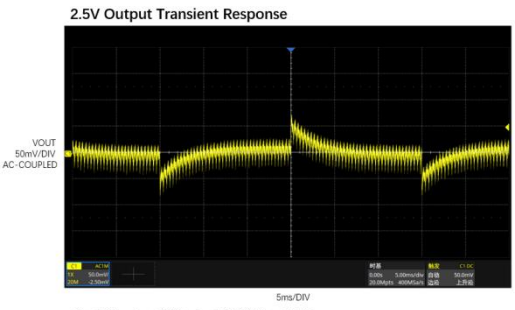




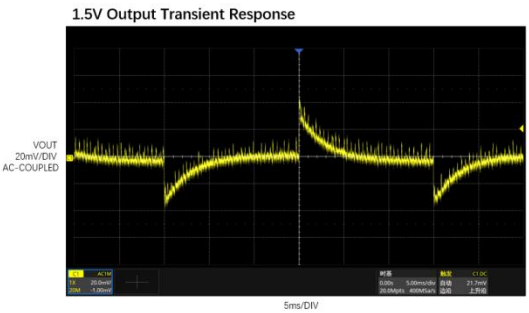




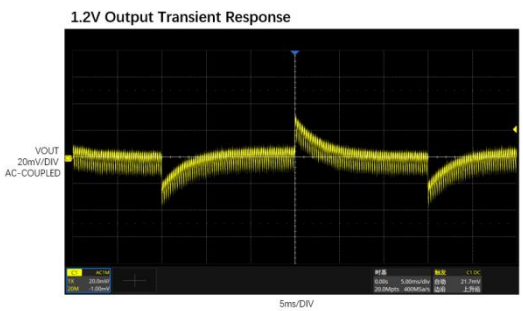
V_{IN}=12V V_{OUT}=3.3V I_{load}=3A TO 4A 1A/us
Output Capacitor=47uf X2



V_{IN}=12V V_{OUT}=2.5V I_{load}=3A TO 4A 1A/us
Output Capacitor=47uf X2

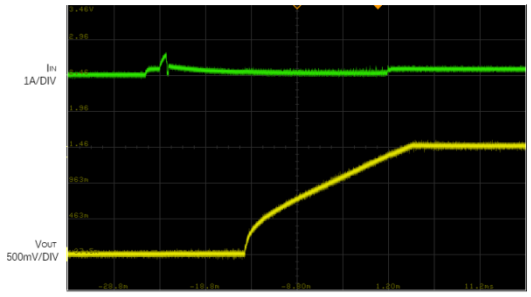


V_{IN}=12V V_{OUT}=1.5V I_{load}=3A TO 4A 1A/us
Output Capacitor=47uf X2



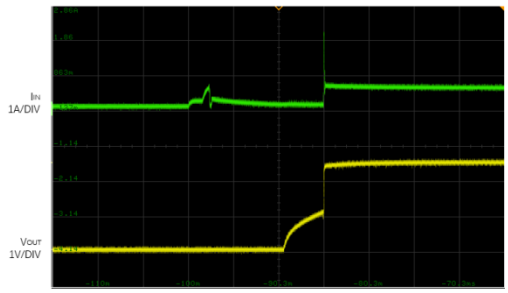
V_{IN}=12V V_{OUT}=1.2V I_{load}=3A TO 4A 1A/us
Output Capacitor=47uf X2

Start-UP with No Load



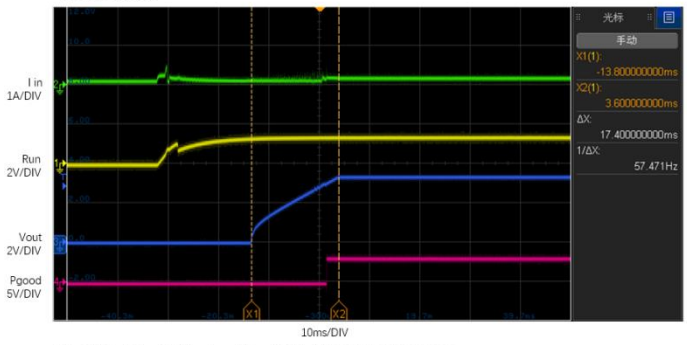
V_{IN}=12V V_{OUT}=1.5V SOFT-START Capacitor=0.1uF
Output Capacitor=47uf X2

Start-UP with 2A Load



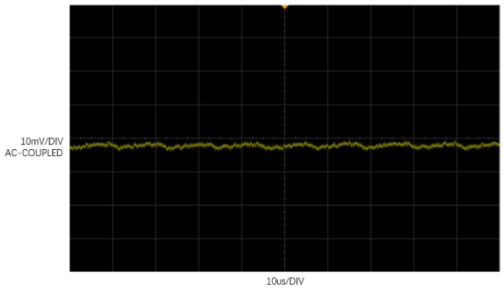
V_{IN}=12V V_{OUT}=2.5V SOFT-START Capacitor=0.1uF
Output Capacitor=47uf X2

Start Status



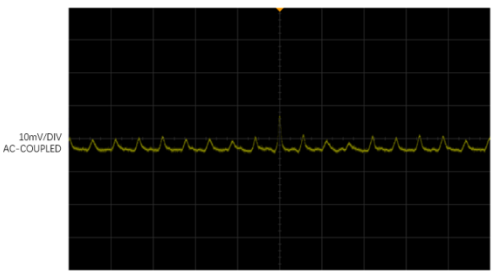
V_{IN}=12V V_{OUT}=3.3V I_{load}=0A SOFT-START Capacitor=0.1uF
Output Capacitor=47uf X2

Output Ripple



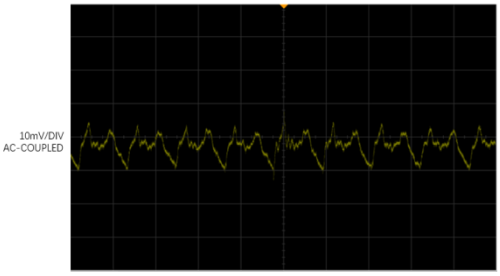
V_{IN}=5V V_{OUT}=2.5V I_{load}=4A SOFT-START Capacitor=0.1uF
Output Capacitor=47uf X2

Output Ripple



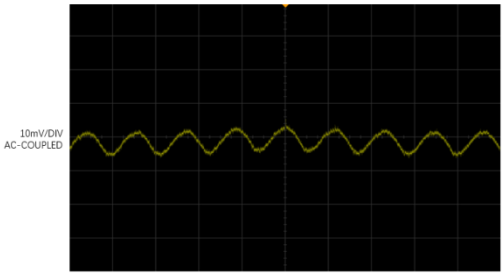
V_{IN}=5V V_{OUT}=1.5V I_{load}=0A SOFT-START Capacitor=0.1uF
Output Capacitor=47uf X2

Output Ripple



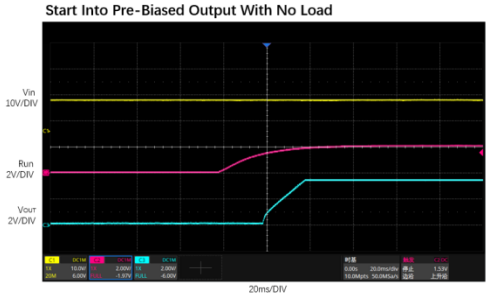
V_{IN}=12V V_{OUT}=1.5V I_{load}=4A SOFT-START Capacitor=0.1uF
Output Capacitor=47uf X2

Output Ripple



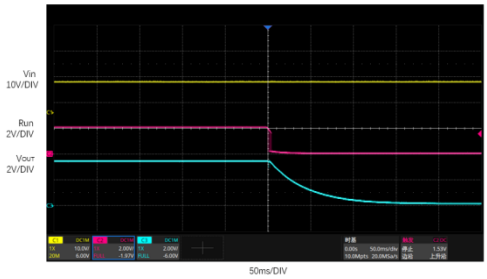
V_{IN}=12V V_{OUT}=3.3V I_{load}=0A SOFT-START Capacitor=0.1uF
Output Capacitor=47uf X2

Start Into Pre-Biased Output With No Load



V_{IN}=12V V_{OUT}=3.3V SOFT-START Capacitor=0.1uF
Output Capacitor=47uf X2

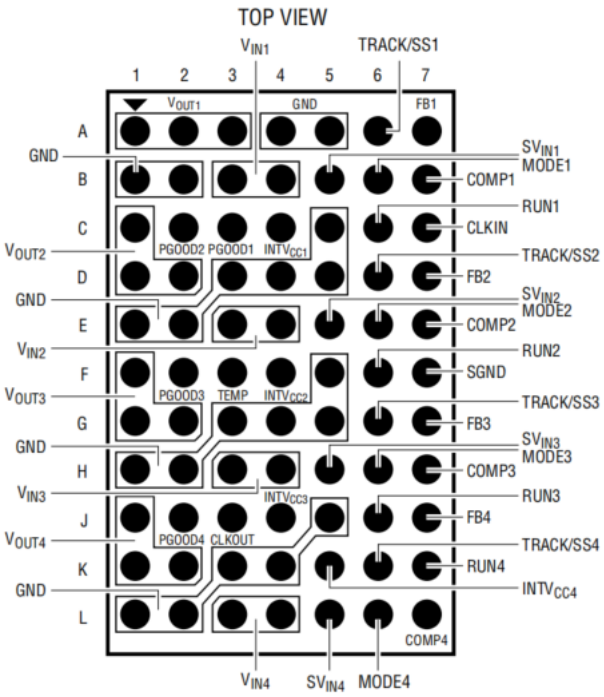
Enable To Close Output （No Load）



V_{IN}=12V V_{OUT}=3.3V SOFT-START Capacitor=0.1uF
Output Capacitor=47uf X2

3 PIN

3.1 PIN Configuration



3.2 PIN Functions

MODE1,MODE2,MODE3,MODE4: Operation Mode Select for Each Switching Mode Regulator Channel. Tie this pin to $INTV_{CC}$ to force continuous synchronous operation at all output loads. Tying it to SGND enables discontinuous current mode operation at light loads. Do not leave floating.

FB1,FB2,FB3,FB4: The Negative Input of the Error Amplifier for Each Switching Mode Regulator Channel. Internally, in ASP4644, this pin is connected to V_{OUT} of each channel with a 60.4kΩ precision resistor. Different output voltages can be programmed with an additional resistor between the FB and GND pins for the ASP4644.

TRACK/SS1,TRACK/SS2,TRACK/SS3,TRACK/SS4: Output Tracking and Soft-

Start Pin of Each Switching Mode Regulator Channel. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to match the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 2.5μA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function

COMP1, COMP2,COMP3,COMP4: Current Control Threshold and Error Amplifier Compensation Point of Each Switching Mode Regulator Channel. The internal current comparator threshold is proportional to this voltage. Tie the COMP pins together for parallel operation. The device is internally compensated.

RUN1, RUN2, RUN3, RUN4: Run Control Input of Each Switching Mode Regulator Channel. Enable regulator operation by tying the specific RUN pin above 1.2V. Pulling it below 1.1V shuts down the respective regulator channel. Do not leave floating.

PGOOD1 ,PGOOD2,PGOOD3 ,PGOOD4: Output Power Good with Open-Drain Logic of Each Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within ±10% of the internal 0.6V reference.

GND : Power Ground Pins for Both Input and Output Returns. Use large PCB copper areas to connect all GND together.

SGND : Signal Ground Connection. SGND is connected to GND internally through single point. Use a separated SGND ground copper area for the ground of the feedback resistor and other components connected to signal pins. A second connection between the PGND plane and SGND plane is recommended on the backside of the PCB underneath the module.

SV_{IN1}，SV_{IN2}，SV_{IN3}，SV_{IN4}: Signal V_{IN} Filtered input voltage to the internal 3.3V regulator for the control circuitry of each Switching mode Regulator Channel. Tie this pin to the V_{IN} pin respectively in most applications. Connect SV_{IN} to an external voltage supply of at least 4V which must also be greater than V_{OUT}.

$INTV_{CC1}$，$INTV_{CC2}$，$INTV_{CC3}$，$INTV_{CC4}$: Internal 3.3V Regulator Output of Each

Switching Mode Regulator Channel. The internal power drivers and control circuits are powered from this voltage. Each pin is internally decoupled to GND with 1μF low ESR ceramic capacitor already.

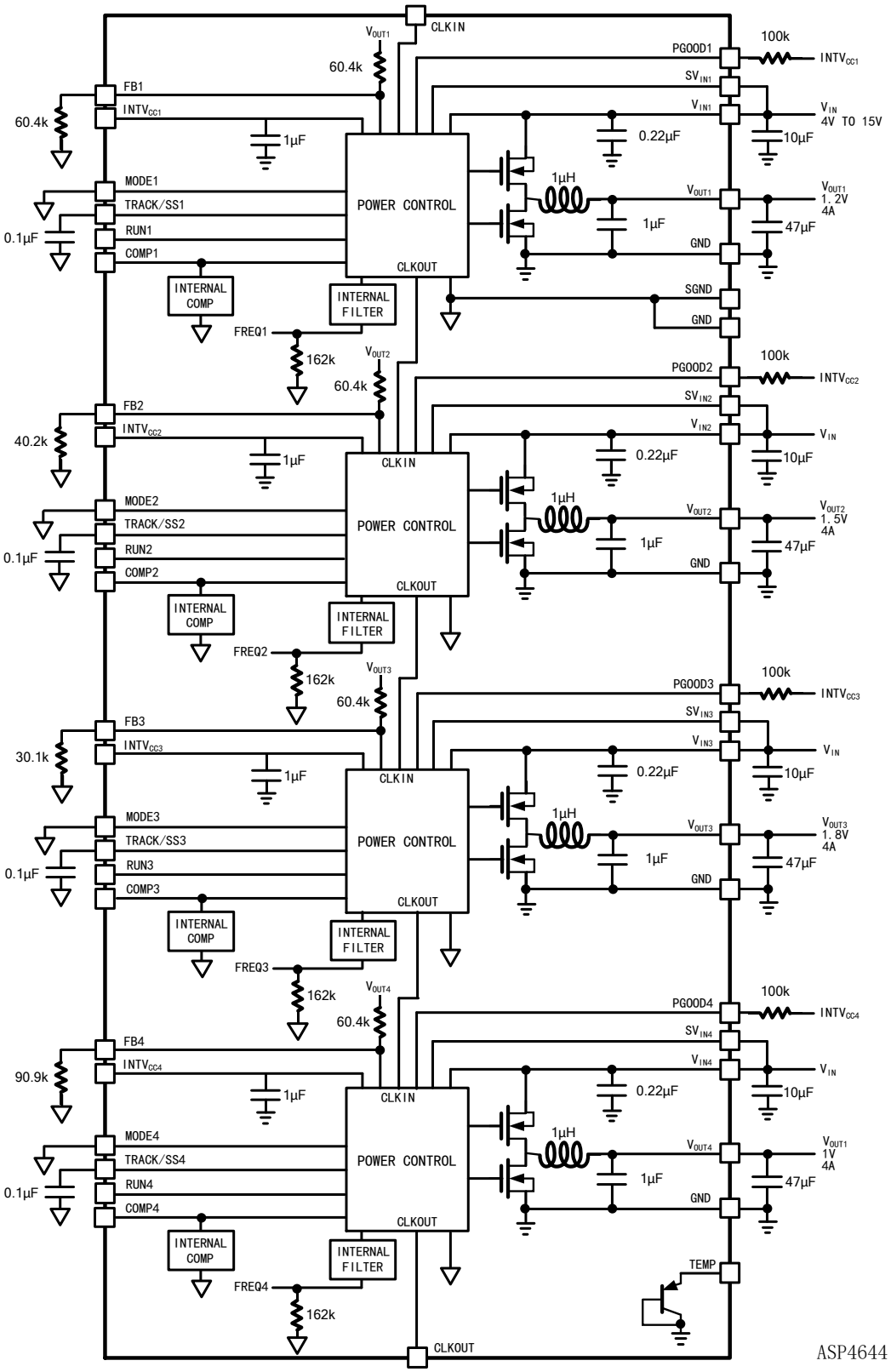
CLKOUT : Output Clock Signal for Phase Operation of the Module. The phase of CLKOUT with respect to CLKIN is set to 180°. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. See the Application Information section for details. Strictly output; do not drive this pin. CLKOUT is only active when RUN4 is enabled.

CLKIN : External Synchronization Input to Phase Detector of the Module. This pin is internally terminated to SGND with 20kΩ. The phase-locked loop will force the channel 1 turn-on signal to be synchronized with the rising edge of the CLKIN signal. Channel 2, channel 3 and channel 4 will also be synchronized with the rising edge of the CLKIN signal with a pre-determined phase shift.

V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}: Power Output Pins of Each Switching Mode Regulator Channel. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

V_{IN1},V_{IN2},V_{IN3},V_{IN4}: Power input pins connect to the drain of the internal top MOSFET for each switching mode regulator channel. Apply input voltages between these pins and GND pins. Recommend placing input decoupling capacitance directly between each of V_{IN} pins and GND pins.

4 BLOCK DIAGRAM



5 APPLICATION

5.1 Functional Description

The ASP4644 is a quad output standalone non-isolated switch mode DC/DC power supply. It has four separate regulator channels with each of them capable of delivering up to 4A continuous output current with few external input and output capacitors. Each regulator provides precisely regulated output voltage programmable from 0.6V to 5.5V via a single external resistor over 4V to 14V input voltage range.

The ASP4644 integrates four separate constant frequency controlled on-time valley current mode regulators, power MOSFETs, inductors, and other supporting discrete components. The typical switching frequency is set to 1MHz. For switching noise-sensitive applications, the µModule regulator can be externally synchronized to a clock from 700kHz to 1.3MHz.

Current mode control also provides cycle-by-cycle fast current monitoring. Foldback current limiting is provided in an overcurrent condition to reduce the inductor valley current to approximately 40% of the original value when V_{FB} drops. An internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Continuous conduction mode (CCM) operation is forced during OV and UV conditions except during start-up when the TRACK pin is ramping up to 0.6V.

Pulling the RUN pin below 1.1V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry.

5.2 Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects each regulator channel from V_{OUT}

pin to FB pin.

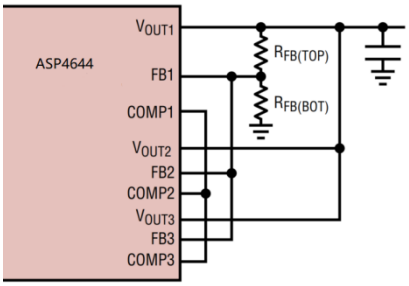


Figure 1 ASP4644 Feedback Resistor for Paralleling Application

Adding a resistor $R_{FB(BOT)}$ from FB pin to GND programs the output voltage:

$$R_{FB(BOT)} = \frac{60.4K}{\frac{V_{OUT}}{0.6} - 1}$$

Table 1: Relationship between VFB Pin Resistance and Output Voltage V_{OUT}

V_{OUT}(V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5
$R_{FB(BOT)}$(k)	Open	90.9	60.4	40.2	30.1	19.1	13.3	8.25

For parallel operation of N channels, use the following equation can be used to solve for $R_{FB(BOT)}$. Tie the V_{OUT} and the FB and COMP pins together for each paralleled output with a single resistor to GND as determined by:

$$R_{FB(BOT)} = \frac{\frac{60.4K}{N}}{\frac{V_{OUT}}{0.6} - 1}$$

For parallel operation of N Channels, only one set of $R_{FB(TOP)}$ and $R_{FB(BOT)}$ is needed while tying the V_{OUT}, FB and COMP pins from different channels together. See Figure 1 for example.

5.3 Input Decoupling Capacitors

The ASP4644 module should be connected to a low acimpedance DC source. For each regulator channel, a 10μF input ceramic capacitor is recommended for RMS ripple current decoupling. A bulk input capacitor is only needed when the input source

impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor or polymer capacitor.

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D(1-D)}$$

where η% is the estimated efficiency of the power module.

5.4 Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only single piece of low ESR output ceramic capacitor is required for each regulator channel to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 2 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 2A load step transient.

V_{OUT} (V)	C_{IN} (CERAMIC) (µF)	C_{IN} (BULK)	C_{OUT1} (CERAMIC) (µF)	C_{OUT2} (BULK) (µF)	C_{FF} (pF)	V_{IN} (V)	DROOP (mv)	P-P DERIVATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	R_{FB} (kΩ)
1	10		47			5,12	5	72	40	1	1	90.9
1	10			100µF	10	5,12	5	60	40	1	1	90.9
1	10		47			5,12	5	127	40	2	1	90.9
1	10			100µF	10	5,12	5	90	40	2	1	90.9
1.2	10		47			5,12	5	76	40	1	1	60.4
1.2	10			100µF	10	5,12	5	65	40	1	1	60.4
1.2	10		47			5,12	5	145	40	2	1	60.4
1.2	10			100µF	10	5,12	5	103	40	2	1	60.4
1.5	10		47			5,12	5	80	40	1	1	40.2
1.5	10			100µF	10	5,12	5	70	40	1	1	40.2
1.5	10		47			5,12	5	161	40	2	1	40.2
1.5	10			100µF	10	5,12	5	115	40	2	1	40.2
1.8	10		47			5,12	5	95	40	1	1	30.1
1.8	10			100µF	10	5,12	5	80	40	1	1	30.1
1.8	10		47			5,12	5	177	40	2	1	30.1
1.8	10			100µF	10	5,12	5	128	40	2	1	30.1
2.5	10		47			5,12	5	125	40	1	1	19.1
2.5	10			100µF	10	5,12	5	100	50	1	1	19.1
2.5	10		47			5,12	5	225	40	2	1	19.1
2.5	10			100µF	10	5,12	5	161	50	2	1	19.1
3.3	10		47			5,12	5	155	40	1	1	13.3
3.3	10			100µF	10	5,12	5	122	60	1	1	13.3
3.3	10		47			5,12	5	285	40	2	1	13.3
3.3	10			100µF	10	5,12	5	198	60	2	1	13.3
5	10		47		10	5,12	5	220	40	1	1	8.25
5	10			100µF	10	5,12	5	420	40	2	1	8.25

Table 2 The pairing of output voltage and capacitance

5.5 Discontinuous Conduction Mode (DCM)

In applications where low output ripple and high efficiency at intermediate current are desired, discontinuous conduction mode (DCM) should be used by connecting the MODE pin to SGND. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode.

5.6 Force Continuous Conduction Mode (CCM)

In applications where fixed frequency operation is more critical than low current

efficiency, and where the lowest output ripple is desired, forced continuous conduction mode operation should be used. Forced continuous operation can be enabled by tying the MODE pin to $INTV_{CC}$. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the ASP4644's output voltage is in regulation.

5.7 Operating Frequency

The operating frequency of the ASP4644 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 1MHz. In most applications, no additional frequency adjusting is required.

If any operating frequency other than 1MHz is required by application, the µModule regulator can be externally synchronized to a clock from 700kHz to 1.3MHz.

5.8 Frequency Synchronization and Clock In

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows all internal top MOSFET turn-on to be locked to the rising edge of the same external clock. The external clock frequency range must be within ±30% around the 1MHz set frequency. A pulse detection circuit is used to detect a clock on the CLKIN pin to turn on the phase-locked loop. The pulse width of the clock has to be at least 400ns. The clock high level must be above 2V and clock low level below 0.3V. During the start-up of the regulator, the phase-locked loop function is disabled.

5.9 Multichannel Parallel Operation

For loads that demand more than 4A of output current, the ASP4644 multiple regulator channels can be easily paralleled to provide more output current without increasing input and output voltage ripples. The ASP4644 has preset built-in phase shift between each two of the four regulator channels which is suitable to employ a 2+2, 3+1 or 4 channels parallel operation. Table 3 gives the phase difference between regulator channels.

Table 3 Phase Difference Between Regulator Channels

CHANNEL	CH1	CH2	CH3	CH4
Phase Difference	180°	90°	180°	

The figure shows a 2+2 and a 4-channels parallel concept schematic for clock phasing.

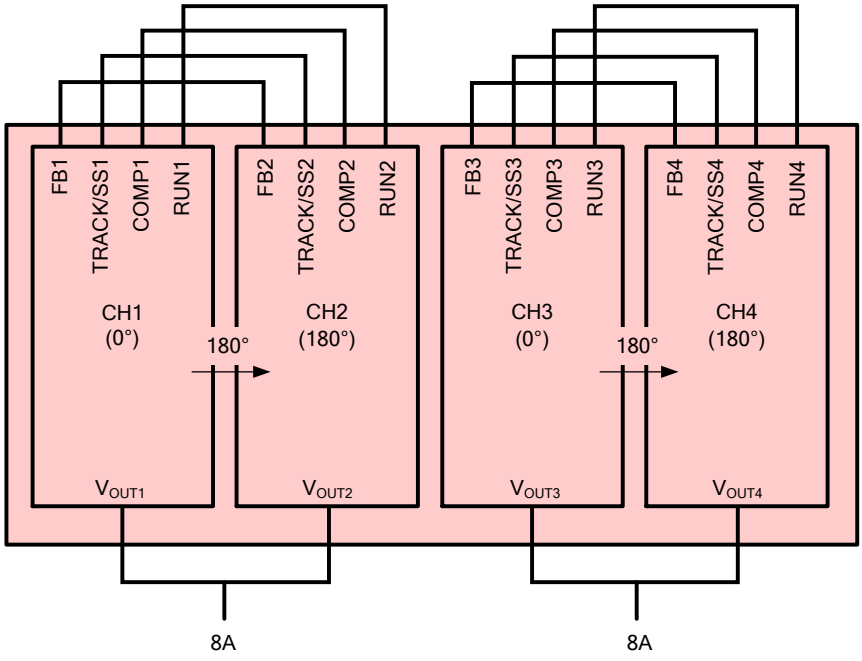


Figure 2 2+2 Channels Parallel Concept Schematic

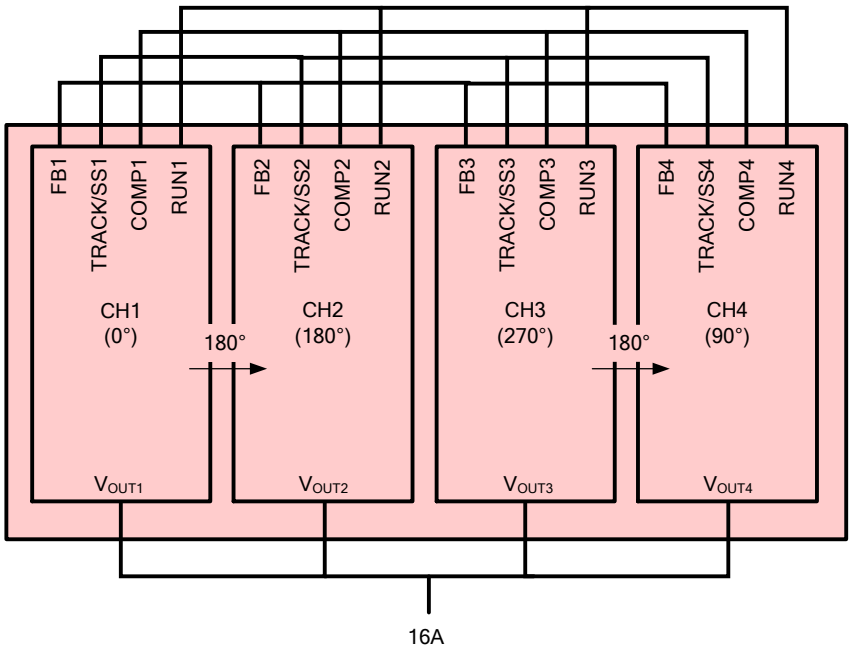


Figure 3 shows 2+2 and a 4 Channels Parallel Concept Schematic

The ASP4644 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Please tie the RUN, TRACK/SS, FB and COMP pins of each paralleling channel together.

5.10 Soft-Start and Output Voltage Tracking

The TRACK/SS pin provides a means to either soft-start of each regulator channel or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal 2.5μA current source will charge up the external soft-start capacitor towards the $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{SS} = 0.6 \cdot \frac{C_{SS}}{2.5\mu A}$$

where CSS is the capacitance on the TRACK/SS pin. Current foldback and forced continuous mode are disabled during the soft-start process.

Output voltage tracking can also be programmed externally using the TRACK/SS pin

of each regulator channel. The output can be tracked up and down with another regulator. Figure 4 and Figure 5 show an example waveform and schematic of a ratiometric tracking where the slave regulator's (V_{OUT2}, V_{OUT3} and V_{OUT4}) output slew rate is proportional to the master's (V_{OUT1}).

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave output voltage and the master output voltage should satisfy the following equation during the start-up.

$$V_{OUT(SL)} \cdot \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \cdot \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

Where the 60.4k is the integrated top feedback resistor and the $R_{FB(SL)}$ is the external bottom feedback resistor of the ASP4644. The $R_{TR(TOP)}/R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 5.

Following the upper equation, the master's output slew rate (MR) and the slave's output slew rate (SR) in volts/time is determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

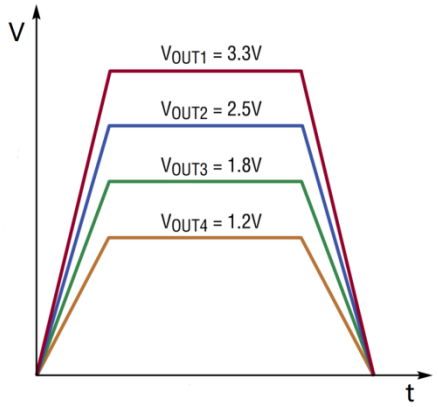


Figure 4 Output Ratiometric Tracking Waveform

For example, $V_{OUT(MA)}$=3.3V, MR=3.3V/24ms and $V_{OUT(SL)}$=1.2V, SR= 1.2V/24ms as V_{OUT1} and V_{OUT4} shown in Figure 5. From the equation, we could solve out that $R_{TR4(TOP)}$ = 60.4k and $R_{TR4(BOT)}$= 13.3k is a good combination. Follow the same equation, we can

get the same $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider value for V_{OUT2} and V_{OUT3}.

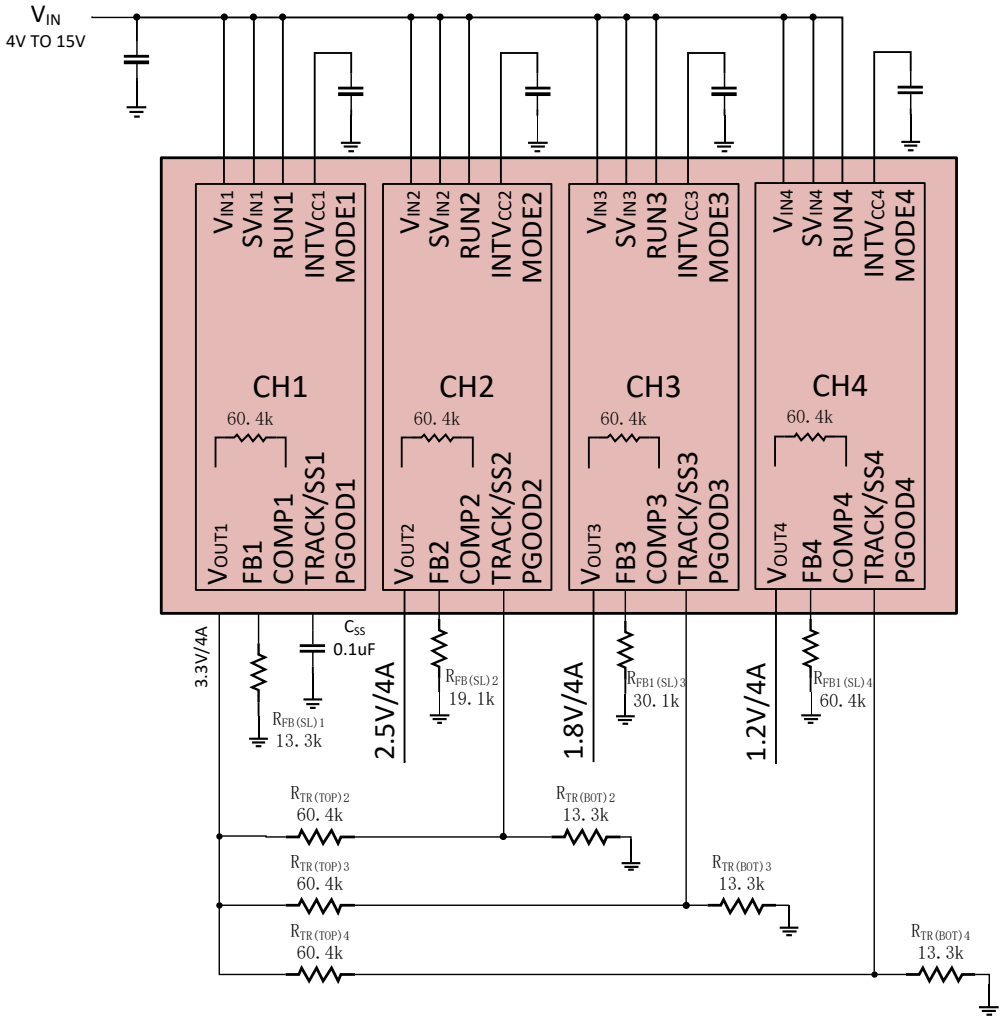


Figure 5 Output Ratiometric Tracking Schematic

The coincident output tracking can be recognized as a special ratiometric output tracking which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), as waveform shown in Figure 6.

From the equation we could easily find out that, in the coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its output voltage divider.

$$\frac{R_{FB(SL)}}{R_{FB(SL)}+60.4k} = \frac{R_{TR(BOT)}}{R_{TR(TOP)}+R_{TR(BOT)}}$$

For example, $R_{TR4(TOP)}$ = 60.4k and $R_{TR4(BOT)}$ = 60.4k is a good combination for coincident tracking for $V_{OUT(MA)}$ = 3.3V and $V_{OUT(SL)}$ = 1.2V application.

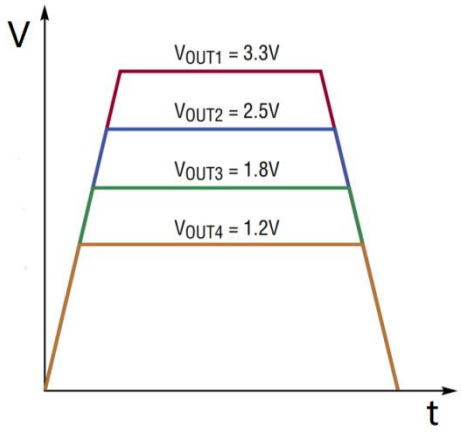


Figure 6 Output Coincident Tracking Waveform

5.11 Power Good

The PGOOD pins are open drain pins that can be used to monitor each valid output voltage regulation. This pin monitors a ±10% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the ASP4644's PGOOD falling edge includes a blanking delay of approximately 52 switching cycles.

5.12 RUN Enable

Pulling the RUN pin of each regulator channel to ground forces the regulator into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.7V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the RUN pin voltage above 1.2V will turn on the entire regulator channel.

5.13 Overtemperature Protection

The internal overtemperature protection monitors the junction temperature of the module. If the junction temperature reaches approximately 160°C, both power switches

will be turned off until the temperature drops about 20°C cooler.

5.14 Layout Checklist/Example

The high integration of ASP4644 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

• Use large PCB copper areas for high current paths, including V_{IN1} to V_{IN4}, GND, V_{OUT1} to V_{OUT4}. It helps to minimize the PCB conduction loss and thermal stress.

• Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.

• Place a dedicated power ground layer underneath the unit.

• To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.

• Do not put via directly on the pad, unless they are capped or plated over.

• Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.

• For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK/SS pin can be tied a common capacitor for regulator soft-start.

• Bring out test points on the signal pins for monitoring.

Figure 7 gives a good example of the recommended layout.

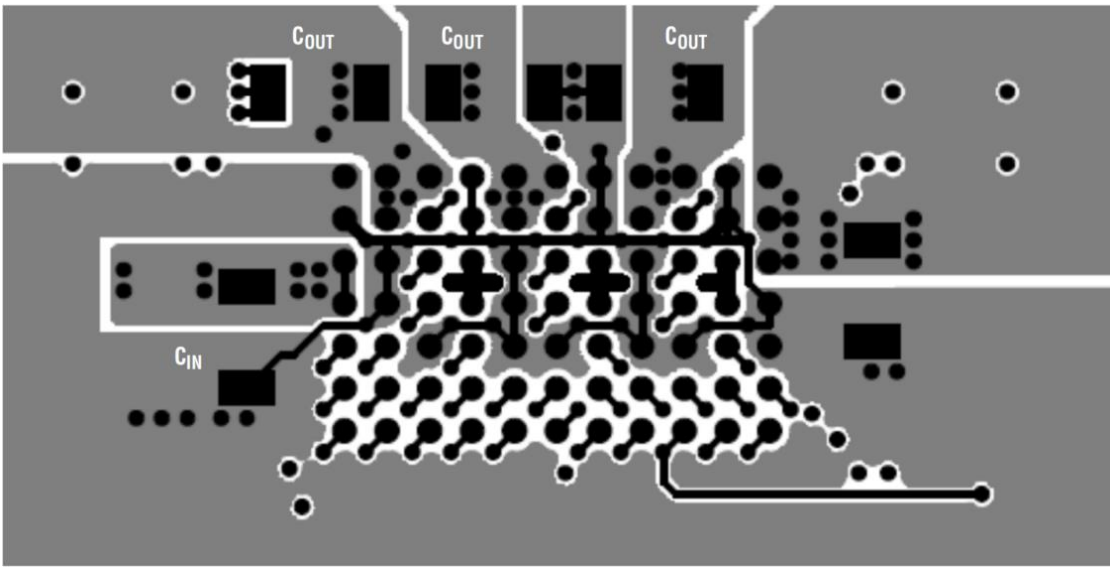


Figure 7 Recommended PCB Layout

5.15 Safety Considerations

The ASP4644 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

5.16 Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD 51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board: defined by JESD 51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients in found in JESD 51-12

("Guidelines for Reporting and Using Electronic Package Thermal Information"). Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application. The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the page. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's

application.

θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 848; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

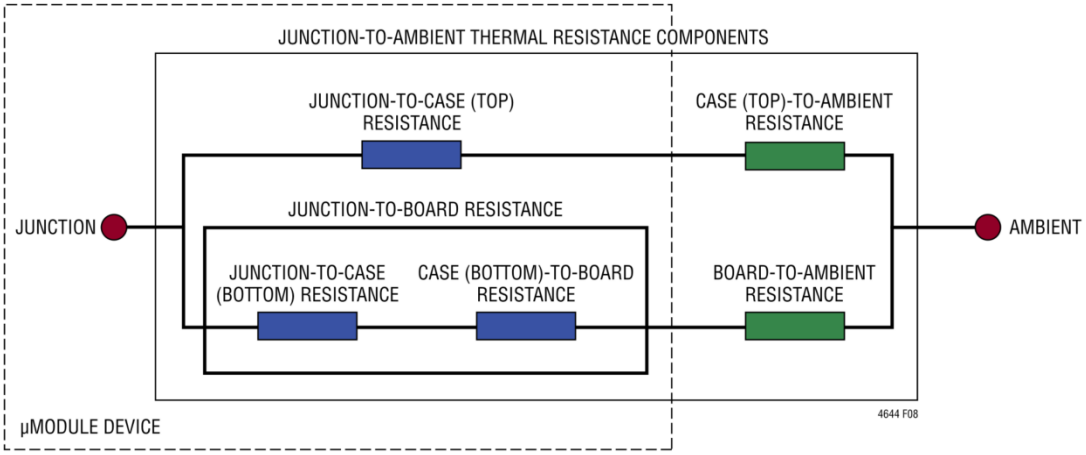


Figure 84 Graphical Representation of JESD 51-12 Thermal Coefficients

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

The thermal characteristic parameter Ψ_{JC} is defined as follows:

To address practical application issues, the table also includes Ψ_{JC}, which estimates the internal junction temperature during testing. Ψ_{JC} represents the ratio of the temperature difference between the junction and the top of the product's outer casing to the total power dissipation of the chip; it is a parameter constructed for this purpose. Despite its formula and unit (°C/W) being similar to θ, Ψ_{JC} is not strictly a 'thermal resistance' parameter. Its definition is as follows:

$$\Psi_{JC} = \frac{T_J - T_C}{P_D} = \frac{T_{JC}}{P_D}$$

Among these parameters, Ψ_{JC} represents the thermal characteristic from junction to case, T_{JC} denotes the junction-to-case temperature difference, and PD stands for the total power dissipation of the chip. Thus, to determine the junction temperature (T_J), first measure the case temperature T_C, calculate the total power dissipation P_D of the chip, and then apply the following formula:

$$T_J = T_C + \Psi_{JC} P_D$$

6 TYPICAL APPLICATIONS

6.1 Output Tracking Mode

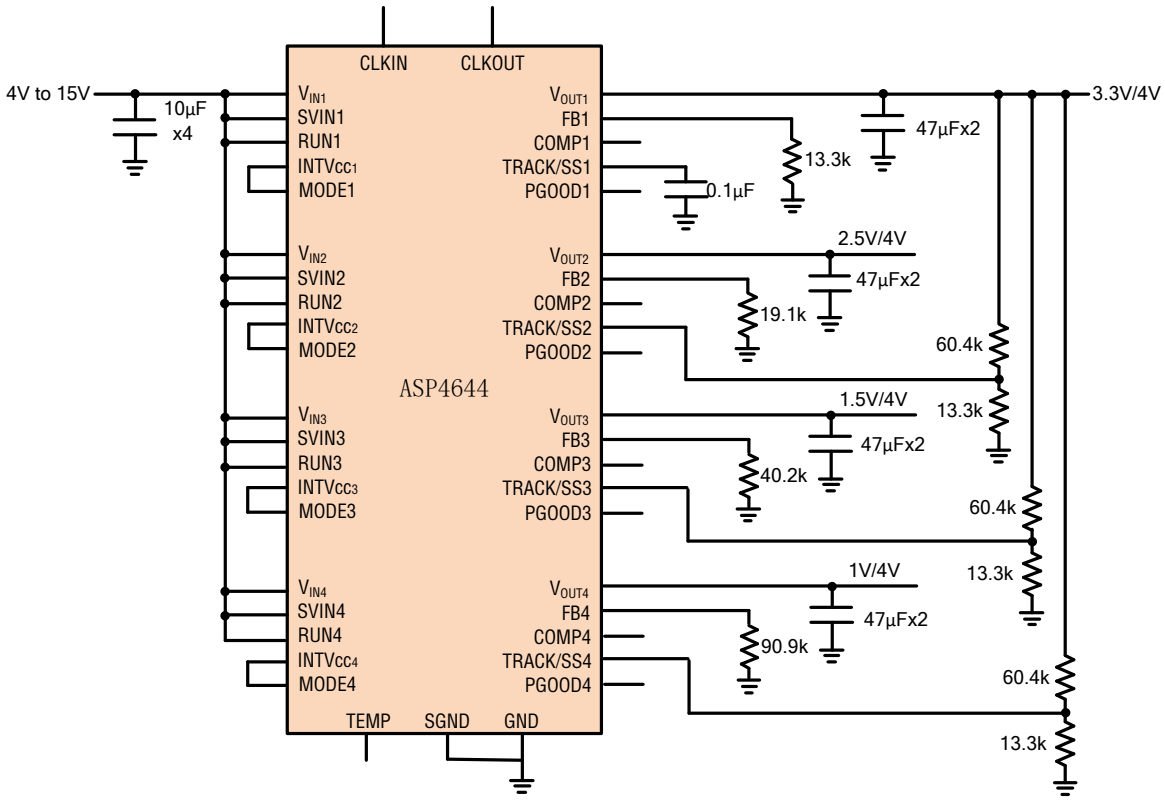


Figure 9 4V to 14V Input, Quad 1.2V, 1.5V, 2.5V and 3.3V Output with Tracking

6.2 Mode for Driving Large Loads in a 4-way Parallel Configuration

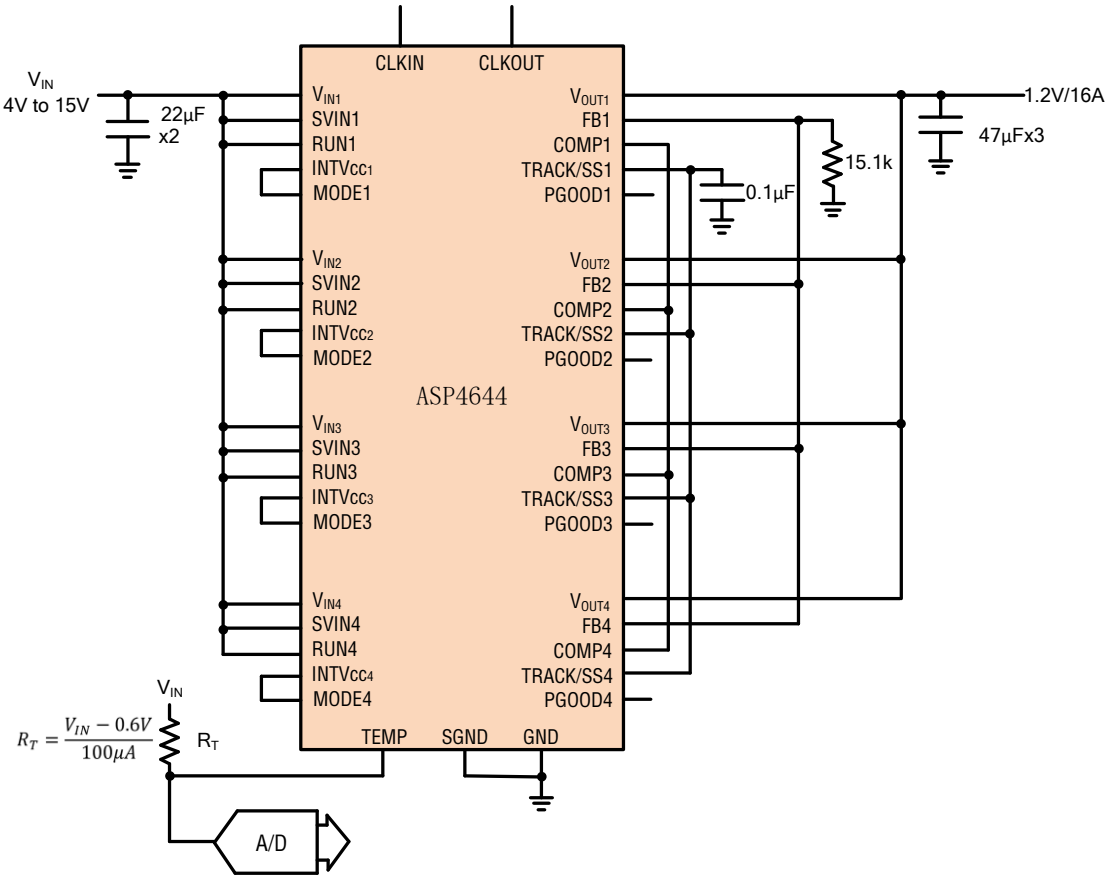


Figure 50 4V to 14V Input, 4-Phase, 1.2V at 16A Design with Temperature Monitoring

6.3 2+2 Drive Mode

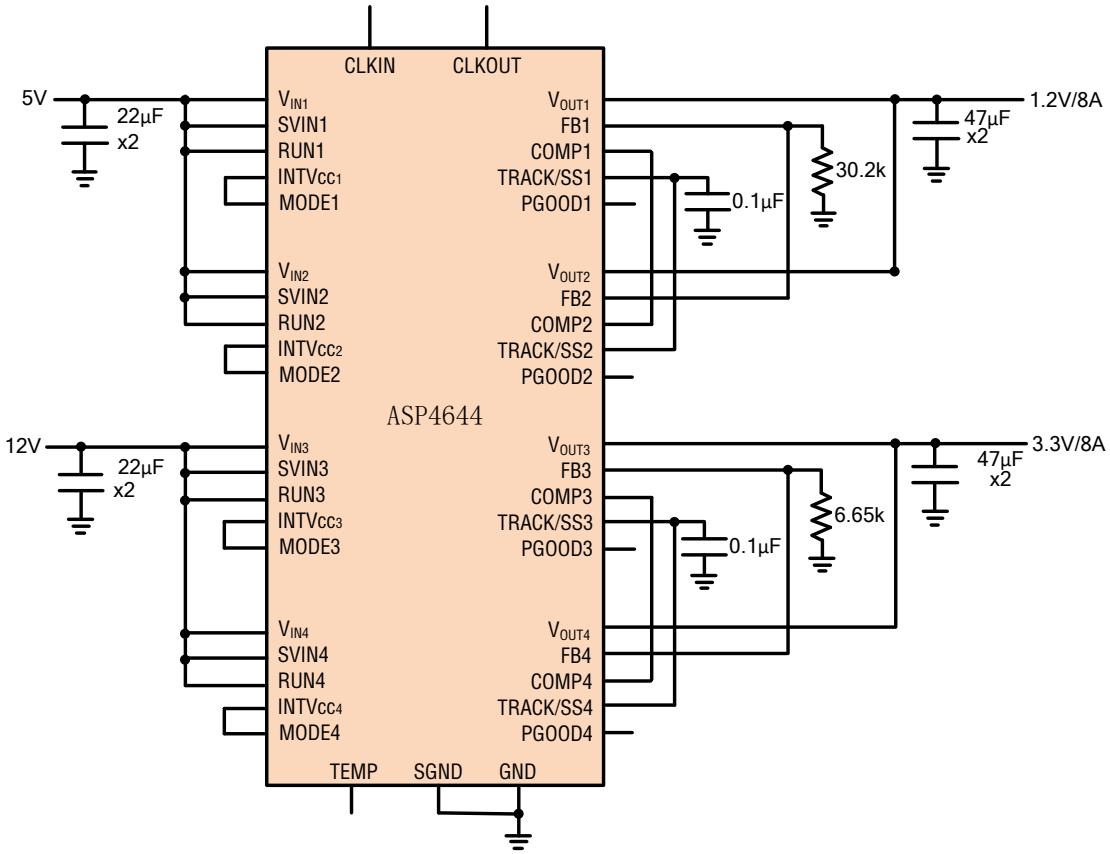


Figure 11 12V and 5V Two Separate Input Rails, 1.2V at 8A and 3.3V at 8A Output