ANSILIC

ASP3605 Datasheet

15V、5A Synchronous Step-Down Regulator

目录

1 Brief introduction

1.1 Description

The ASP3605 is a high efficiency, monolithic synchronous buck regulator using a phase lockable controlled on-time constant frequency, current mode architecture. PolyPhase operation allows multiple ASP3605 regulators to run out of phase while using minimal input and output capacitance. The operating supply voltage range is from 15V down to 4V, making it suitable for dual lithium-ion battery inputs as well as point of load power supply applications from a 12V or 5V rail.
The operating frequency is programmable from 800kHz to 4MHz with an external resistor. The high frequency capability allows the use of small surface mount inductors. For switching noise sensitive applications, it can be externally synchronized from 800kHz to 4MHz. The PHMODE pin allows user control of the phase of the outgoing clock signal. The unique constant frequency/controlled on-time architecture is ideal for high step-down ratio applications that are operating at high frequency while demanding fast transient response. Two internal phase-lock loops synchronize the internal oscillator to the external clock and also servos the regulator on-time to lock on to either the internal clock or the external clock if it's present.

1.2 Features

High Efficiency: Up to 94%
Output Current: 5A
V_{IN} Range: 4V to 15V
Integrated Power N-Channel MOSFETs
Adjustable Frequency：800kHz to 4MHz
PolyPhase Operation：Up to 12 Phases
Output Tracking
0.6V ±1% Reference Accuracy
Typical Ripple Value : 4.5mV
Current Mode Operation for Excellent Line and Load Transient Response
Vehicle certification: AEC-Q100 Grade1 (Automotive grade)
SEU: ≥75Mev.cm^2/mg or 10^{-5} times/device.day (Commercial aerospace grade)
SEL: ≥75Mev.cm^2/mg (Commercial aerospace grade)
Package: QFN24 (4mm × 4mm)

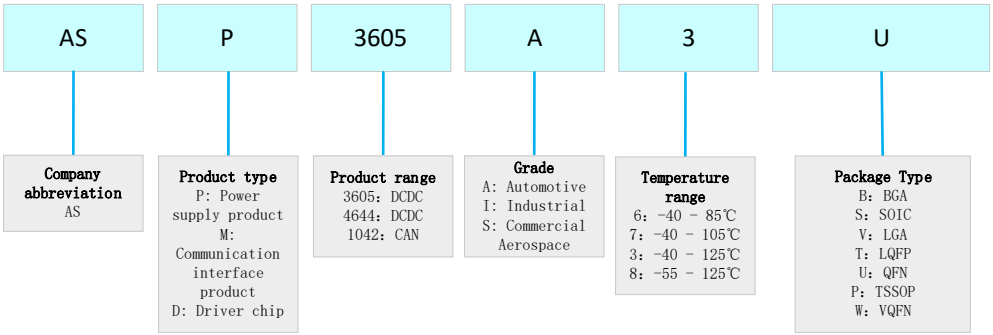
1.3 Series products

The chip model is as follows：

CHIP	CHIP MODEL	LEVEL	PACKAGE	REMARKS

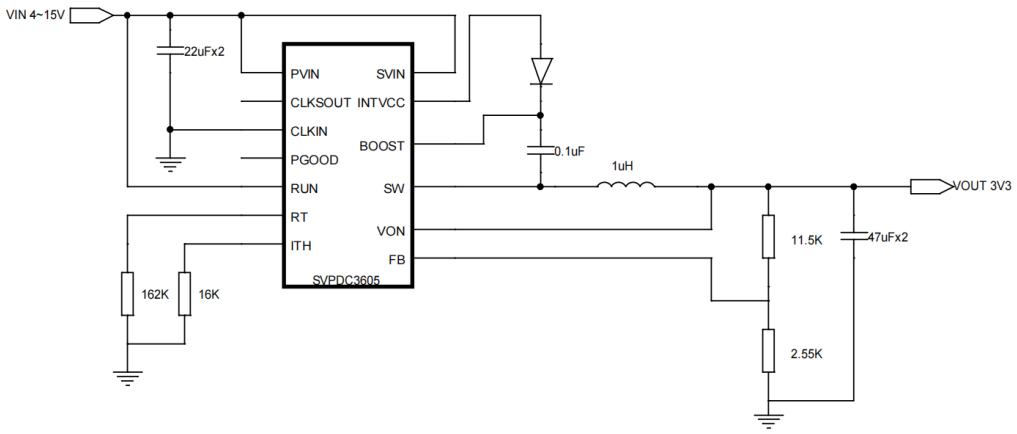
TYPE			DESCRIPTION	
Power chip	ASP3605I6U	Industrial grade	QFN24	
Power chip	ASP3605A3U	Automobile grade	QFN24	
Power chip	ASP3605S8U	Commercial aerospace grade	QFN24	

Chip naming convention



1.4 TYPICAL APPLICATION

Scheme diagram of high efficiency 1MHz, 5A buck regulator

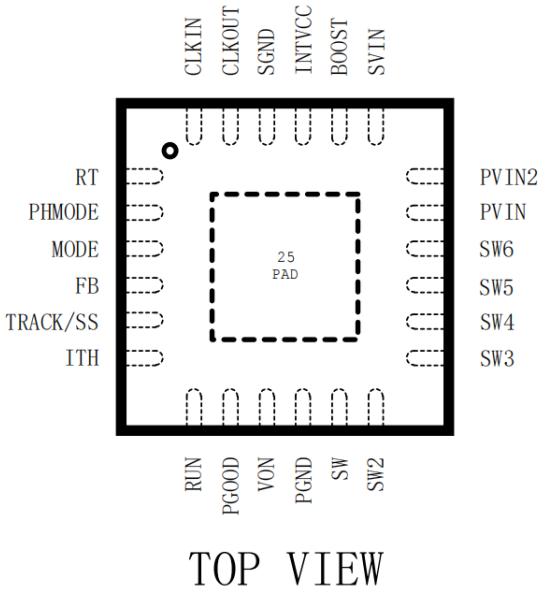


1.5 APPLICATION SCENARIO

Point of Load Power Supply
Portable Instruments
Distributed Power Systems
Battery-Powered Equipment

2 PIN DESCRIPTION

2.1 PIN ARRANGEMENT



TOP VIEW

2.2 PIN FUNCTIONS

RT (Pin 1): Oscillator Frequency Programming Pin. Connect an external resistor (between 200k to 40k) from RT to SGND to program the frequency from 800kHz to 4MHz. Since the synchronization range is ±30% of set frequency, be sure that the set frequency is within this percentage range of the external clock to ensure frequency lock.
PHMODE (Pin 2): Control Input to Phase Selector. Determines the phase relationship between internal oscillator and CLKOUT. Tie it to $INTV_{CC}$ for 2-phase operation, tie it to SGND for 3-phase operation, and tie it to $INTV_{CC}/2$ for 4-phase operation.
MODE (Pin 3): Operation Mode Select. Tie this pin to $INTV_{CC}$ to force continuous synchronous operation at all output loads. Tying it to SGND enables discontinuous mode operation at light loads. Do not float this pin.
FB (Pin 4): Output Feedback Voltage. Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. This pin is normally connected to a resistive divider from the output voltage.
TRACK/SS (Pin 5): Output Tracking and Soft-Start Pin. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 2μA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides soft-start function.

COMP (Pin 6): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.8V. Tying this pin to $INTV_{CC}$ activates internal compensation and output voltage positioning, raising V_{OUT} to 1.5% higher than the nominal value at I_{OUT} = 0 and 1.5% lower at I_{OUT} = 5A.

RUN (Pin 7): Run Control Input. Enables chip operation by tying RUN above 1.2V. Tying it below 1.1V shuts down the part.

PGOOD (Pin 8): Output Power Good with Open-Drain Logic. PGOOD is pulled to ground when the voltage on the FB pin is not within ±10% of the internal 0.6V reference.

V_{ON} (Pin 9): On-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to V_{OUT} and keeps the switching frequency constant at different V_{OUT}. However, when V_{ON} is <0.6V or >6V, then switching frequency will no longer remain constant.

PGND (Pin 10, Pin 25): Power Ground. Return path of internal power MOSFETs. Connect this pin to the negative terminals of the input capacitor and output capacitor. The exposed pad must be soldered to the PCB ground for electrical contact and rated thermal performance.

SW (Pins 11 to 16): Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to PV_{IN}.

PV_{IN} (Pins 17, 18): Power V_{IN}. Input voltage to the onchip power MOSFETs.

SV_{IN} (Pin 19): Signal V_{IN}. Filtered input voltage to the on-chip 3.3V regulator. Connect a (1Ω to 10Ω) resistor between SV_{IN} and PVIN and bypass to GND with a 0.1µF capacitor.

BOOST (Pin 20): Boosted Floating Driver Supply for Internal Top Power MOSFET. The (+) terminal of the bootstrap capacitor connects here. This pin swings from a diode voltage drop below $INTV_{CC}$ up to PV_{IN} + $INTV_{CC}$.

INTVCC (Pin 21): Internal 3.3V Regulator Output. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 1µF low ESR ceramic capacitor.

SGND (Pin 22): Signal Ground Connection.

CLKOUT (Pin 23): Output Clock Signal for PolyPhase Operation. The phase of CLKOUT with respect to CLKIN is determined by the state of the PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND.

CLKIN (Pin 24): External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 20k.The phase-locked loop will force the top power NMOS's turn on signal to be synchronized with the rising edge of the CLKIN signal.

3 EIGENVALUE

3.1 ABSOLUTE MAXIMUM RATINGS

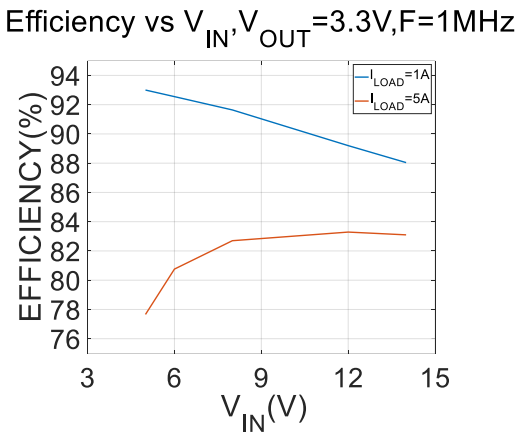
PV_{IN}, SV_{IN}, SW Voltage：–0.3V ~ 15V
SW Transient Voltage：–2V ~ 17.5V
$INTV_{CC}$ Voltage：–0.3V ~ 3.6V
BOOST Voltage：–0.3V ~ PV_{IN} + $INTV_{CC}$
V_{ON} Voltage：–0.3V ~ SV_{IN}
RUN Voltage：–0.3V ~ 15V
COMP, RT, CLKOUT, PGOOD Voltage：–0.3V ~ INTVCC
CLKIN, PHMODE, MODE Voltage：–0.3V ~ INTVCC
TRACK/SS, FB Voltage：–0.3V ~ INTVCC
Operating Temperature Range：–40°C ~ 125°C
Storage Temperature Range：–65°C ~ 125°C

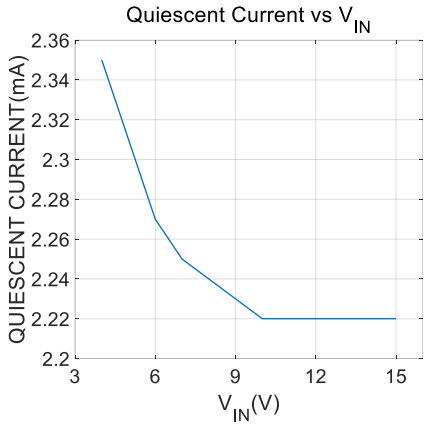
3.2 ELECTRICAL CHARACTERISTICS

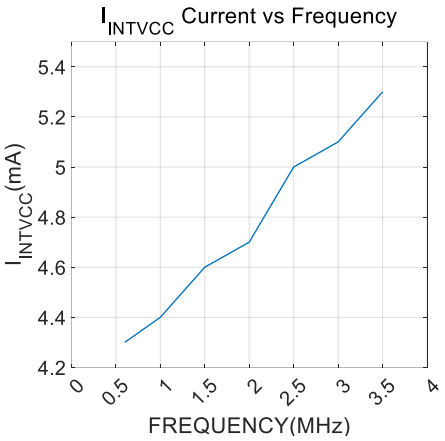
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
P_{VIN}	V_{IN} Supply Range		4		15	V
I_Q	Input DC Supply Current Active Shutdown	Mode = 0, RT = 162k		2 220	10	mA μA
V_{FB}	Feedback Reference Voltage	COMP =1.2V – 40°C to 85°C COMP =1.2V – 40°C to 125°C	0.596 0.596	0.6 0.6	0.614 0.611	V V
$\Delta V_{FB(LINE)}$	Feedback Voltage Line Regulation	V_{IN} = 4V to 15V, COMP = 1.2V,– 40°C to 125°C	0.01	0.08	0.3	%
$\Delta V_{FB(LOAD)}$	Feedback Voltage Load Regulation	COMP = 0.8V to 1.6V, –40°C to 125°C	0.059	0.17	3.2	%
I_{LIM}	Positive Inductor Valley	V_{FB} = 0.57V	5	6	7.5	A

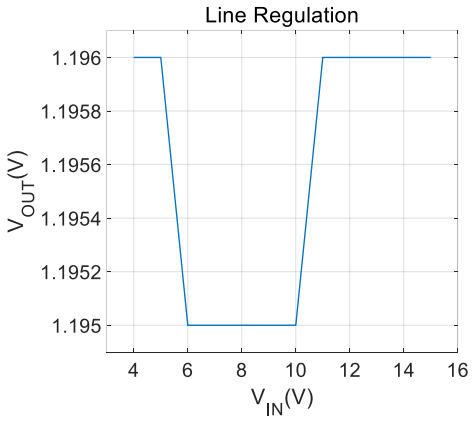
	Current Limit Negative Inductor Valley Current Limit			-5		A
V_{RUN}	I_Q = 2mA I_Q = 400μA	RUN Rising RUN Rising	 0.5	1.2 0.6	 0.9	V
ΔV_{RUN}	Hysteresis voltage			100		mV
V_{INTVCC}	Internal V_{CC} Voltage	4V < V_{IN} < 15V	3.2	3.3	3.5	V
OV	Output Overvoltage PGOOD Upper Threshold	V_{FB} Rising	5	8	11	%
UV	Output Undervoltage PGOOD Lower Threshold	V_{FB} Falling	-13	-10	-7	%
R_{PGOOD}	PGOOD Pull-Down Resistance	1mA Load		25		Ω
I_{PGOOD}	PGOOD Leakage	0.54V<VFB<0.66V		31.6		μA
f_{OSC}	Oscillator Frequency	RT = 162k		1		MHz
CLKIN	CLKIN Threshold			0.7		V
$I_{TRACK/SS}$	TRACK Pull-Up Current			2.2	4	μA
Full-load input current at low voltage	V_{IN} =5V，V_{OUT} =1.2V，I_{OUT}=4A		1.22	1.3		A
Output Ripple Voltage	V_{IN}=5V ，V_{OUT}=1.2V ，I_{Load}=2A Cin=22uF&68uF, Cout=47uF x2 Ceramic			4.5		mV

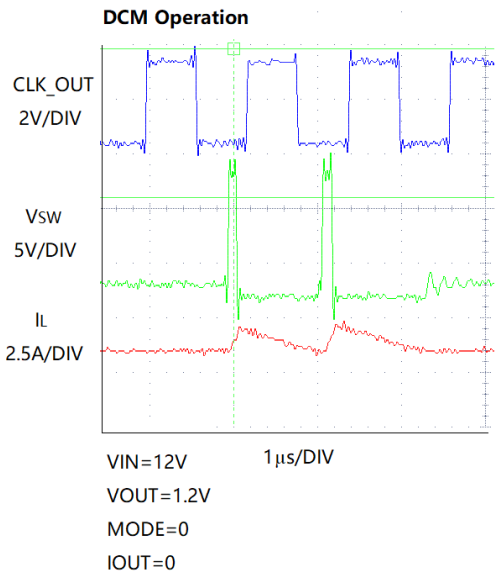
3.3 TYPICAL PERFORMANCE CHARACTERISTICS

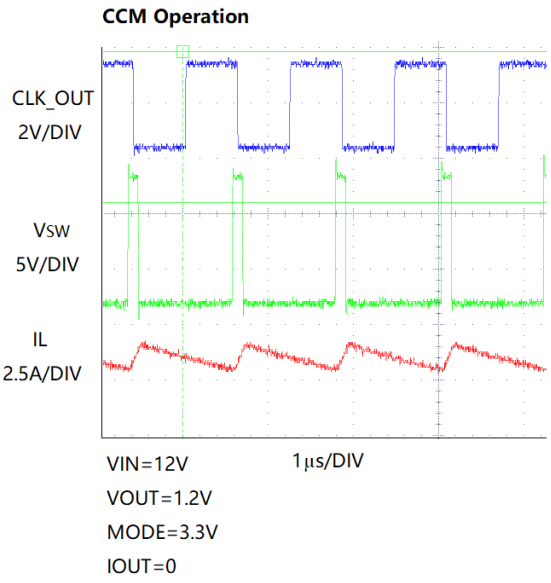


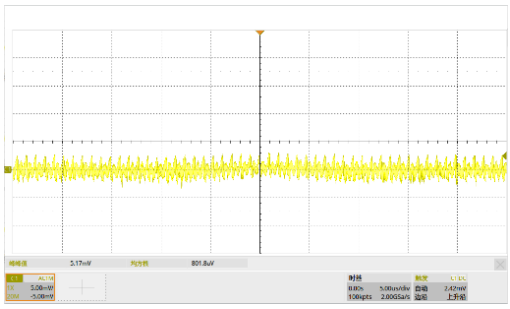




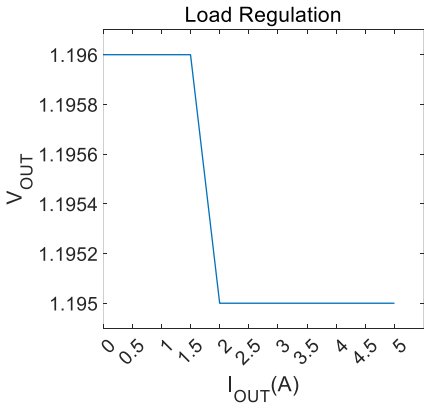








Power ripple



4 OPERATION

4.1 Main Control Loop

The ASP3605 is a current mode monolithic step-down regulator. In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a one-shot timer, OST. When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator, ICMP, trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage drop across the bottom power MOSFET's VDS. The voltage on the COMP pin sets the comparator threshold corresponding to the inductor valley current. The error amplifier, EA, adjusts this COMP voltage by comparing the feedback signal, V_{FB}, from the output voltage with that of an internal 0.6V reference. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference. The COMP voltage then rises until the average inductor current matches that of the load current.

At low load current, the inductor current can drop to zero and become negative. This is detected by current reversal comparator, IREV, which then shuts off the bottom power MOSFET, resulting in discontinuous operation. Both power MOSFETs will remain off with the output capacitor supplying the load current until the COMP voltage rises above the zero current level (0.6V) to initiate another cycle. Discontinuous mode operation is disabled by tying the MODE pin to $INTV_{CC}$, which forces continuous synchronous operation regardless of output load.

The operating frequency is determined by the value of the RT resistor, which programs the current for the internal oscillator. An internal phase-lock loop servos the oscillator frequency to an external clock signal if one is present on the CLKIN pin. Another internal phase-lock loop servos the switching regulator on-time to track the internal oscillator to force constant switching frequency.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage, V_{FB}, exits a ±10% window around the regulation point. Continuous operation is forced during OV and UV condition except during start-up when the TRACK pin is ramping up to 0.6V.

Foldback current limiting is provided if the output is shorted to ground. As V_{FB} drops to zero, the maximum sense voltage allowed across the bottom power MOSFET is lowered to approximately 40% of the original value to reduce the inductor valley current.

Pulling the RUN pin to ground forces the ASP3605 into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.7V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the RUN voltage above 1.2V turns on the entire chip.

4.2 $INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.3V supply that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply up to 100mA RMS and must be bypassed to ground with a minimum of 1μF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Connecting a load to the $INTV_{CC}$ pin is not recommended since it will further push the LDO into its RMS current rating while increasing power dissipation and die temperature.

4.3 V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the ASP3605 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 17V, the regulator suspends operation by shutting off both power MOSFETs. Once V_{IN} drops below 15V, the regulator immediately resumes normal operation. The regulator does not execute its soft-start function when exiting an overvoltage condition.

4.4 PV_{IN}/SV_{IN} Voltage Differential

SV_{IN} should be tied to PV_{IN} with a low pass filter of 1Ω to 10Ω and 0.1μF. For applications where PV_{IN} and SV_{IN} are tied to vastly different voltage potentials, though the output voltage will remain in regulation, there will be an offset in the internal on-time generator such that if SV_{IN} is different than PV_{IN} by more than 50% of the PV_{IN} voltage, the resulting switching frequency will deviate from the frequency programmed by the RT resistor and/or the external clock synchronization frequency. In such applications, in order to return the switching frequency back to the original desired frequency, RT resistor value can be adjusted accordingly. However, the better alternative is to tie the V_{ON} pin to a voltage different than that of V_{OUT} in order to negate the offset of the V_{IN} differential. For instance, if SV_{IN} is 6V and PV_{IN} is 12V, the resulting switching frequency may be slower than what's programmed by the RT resistor. Tying the V_{ON} pin to a voltage half of V_{OUT} will negate the V_{IN} offset and return the switching frequency back to normal.

4.5 Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.6V \bullet (1 + R_2/R_1)$$

The resistive divider allows the VFB pin to sense a fraction of the output voltage as shown in Figure 1.

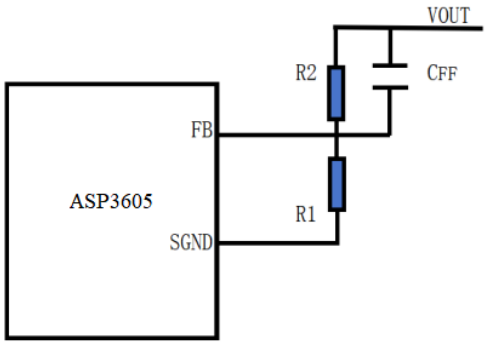


Figure 1. Setting the Output Voltage

4.6 Programming Switching Frequency

Connecting a resistor from the RT pin to SGND programs the switching frequency from 800kHz to 4MHz according to the following formula:.

$$\text{Frequency (Hz)} = \frac{1.6e11}{RT(\Omega)}$$

The internal PLL has a synchronization range of ±30% around its programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this ±30% range of the RT programmed frequency.

4.7 Output Voltage Tracking and Soft-Start

The ASP3605 allows the user to program its output voltage ramp rate by means of the TRACK/SS pin. An internal 2μA pulls up the TRACK/SS pin to $INTV_{CC}$. Putting an external capacitor on TRACK/SS enables soft starting the output to prevent current surge on the input supply. For output tracking applications, TRACK/SS can be externally driven by another voltage source. From 0V to 0.6V, the TRACK/SS voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the feedback voltage to that of TRACK/SS pins. During this start-up time, the ASP3605 will operate in discontinuous mode. When TRACK/SS is above 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.
The soft start time can be calculated using the following formula:

$$T_{SS} = \frac{C_{SS} * 0.6}{I_{SS(2.5\mu A)}}$$

For output tracking applications, the TRACK/SS pin can be externally driven by another voltage source.

4.8 Output Power Good

When the ASP3605's output voltage is within the ±10% window of the regulation point, which is reflected back as a V_{FB} voltage in the range of 0.54V to 0.66V, the output

voltage is good and the PGOOD pin is pulled high with an external resistor. Otherwise, an internal open-drain pulldown device (12Ω) will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the ASP3605's PGOOD falling edge includes a blanking delay of approximately 52 switching cycles.

4.9 Multiphase Operation

For output loads that demand more than 5A of current, multiple ASP3605s can be cascaded to run out of phase to provide more output current. The CLKIN pin allows the ASP3605 to synchronize to an external clock (±50% of frequency programmed by RT) and the internal phase-locked-loop allows the ASP3605 to lock onto CLKIN's phase as well. The CLKOUT signal can be connected to the CLKIN pin of the following ASP3605 stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to $INTV_{CC}$, SGND or $INTV_{CC}/2$ generates a phase difference (between CLKIN and CLKOUT) of 180 degrees, 120 degrees, or 90 degrees respectively, which corresponds to 2-phase, 3-phase or 4-phase operation. A total of 12 phases can be cascaded to run simultaneously out of phase with respect to each other by programming the PHMODE pin of each ASP3605 to different levels.

4.10 Internal/External COMP Compensation

During single phase operation, the user can simplify the loop compensation by tying the COMP pin to $INTV_{CC}$ to enable internal compensation. This connects an internal 30k resistor in series with a 40pF capacitor to the output of the error amplifier (internal COMP compensation point) while also activating output voltage positioning such that the output voltage will be 1.5% above regulation at no load and 1.5% below regulation at full load. This is a trade-off for simplicity instead of OPTI-LOOP optimization, where COMP components are external and are selected to optimize the loop transient response with minimum output capacitance.

4.11 Minimum Off-Time and Minimum On-Time Considerations

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time that the ASP3605 is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the power MOSFET back off. This time is generally about 70ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is::

$$V_{IN(MIN)} = V_{OUT}\frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 40ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{MIN} = f \cdot t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of severe consequences. As the sections on inductor and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application circuit.

4.12 C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} \cong I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 f C_{OUT}} + ESR \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum

electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints. Their relatively low value of bulk capacitance may require multiples in parallel.

4.13 Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 2 to 3 times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} = 2.5\frac{\Delta I_{OUT}}{f_o V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 22μF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the PV_{IN} pins as possible.

4.14 Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \times L}(1 - \frac{V_{OUT}}{V_{IN(MAX)}})$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 2.5A. This is especially important at low V_{OUT} operation where V_{OUT} is 1.8V or below. Care must be given to choose an inductance value that will generate a big enough current ripple (1.5A to 2.5A) so that the chip's valley current comparator has enough signal-to-noise ratio to force constant switching frequency. Meanwhile, also note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f\Delta I_{L(MAX)}}(1 - \frac{V_{OUT}}{V_{IN(MAX)}})$$

However, the inductor ripple current must not be so large that its valley current level ($-\Delta I_L/2$) can exceed the negative current limit, which can be as low as –3.5A. If the negative current limit is exceeded in forced continuous mode of operation, V_{OUT} can get charged to above the regulation level until the inductor current no longer exceeds the negative current limit. In such instances, choose a larger inductor value to reduce the inductor ripple current. The alternative is to reduce the RT resistor value to increase the switching frequency in order to reduce the inductor ripple current.

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements.

4.15 Checking Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the COMP pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test

point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The COMP external components shown in the circuit on the second page of this data sheet provides an adequate starting point for most applications. The series R-C filter sets the dominant pole zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1μs to 10μs will produce output voltage and COMP pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with the R and the bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feedforward capacitor, C_{FF}, can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R_2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. In some applications, a more severe transient can be caused by switching in loads with large (>10μF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft-starting.

4.16 Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement.

Percent efficiency can be expressed as::

$$\%Efficiency = 100\% - (L1 + L2 + L3 + \cdots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in ASP3605 circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses..

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = \left(R_{DS(ON)}TOP\right)(DC) + \left(R_{DS(ON)}BOT\right)(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

$$I^2R\ losses = I_{OUT}^2(R_{SW} + R_L)$$

2. The $INTV_{CC}$ current is the sum of the power MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. Since $INTV_{CC}$ is a low dropout regulator output powered by V_{IN}, its power loss equals:

$$P_{LDO} = V_{IN}I_{INTVCC}$$

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The ASP3605 internal power devices switch quickly enough that these losses are not significant compared to other sources. Other losses including diode conduction losses during dead-time and inductor core losses which generally account for less than 2% total additional loss.

4.17 Thermal Considerations

In a majority of applications, the ASP3605 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed-back QFN package. However, in applications where the ASP3605 is running at high ambient temperature, high V_{IN}, high switching frequency and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 15°C cooler.

To avoid the ASP3605 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \theta_{JA}$$

As an example, consider the case when the ASP3605 is used in applications where V_{IN} = 12V, I_{OUT}= 5A, f = 1MHz, and V_{OUT} = 1.8V. The equivalent power MOSFET resistance R_{SW} is:

$$R_{SW} = R_{DS(ON)}TOP \cdot \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)}Bot(1 - \frac{V_{OUT}}{V_{IN}})$$

The V_{IN} current during 1MHz force continuous operation with no load is about 11mA, which includes switching and internal biasing current loss, transition loss, inductor core loss and other losses in the application. Therefore, the total power dissipated by the part is:

$$P_D = I_{OUT}^2 R_{SW} + V_{IN} I_{VIN}(NO\ Load)$$

The QFN 4mm ×4mm package junction-to-ambient thermal resistance, θ_{JA}, is around 37°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = P_D \cdot 37℃/W + 25℃$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 15% at 67°C yields a new junction temperature of 72°C. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

4.18 Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the ASP3605. Check the following in your layout:

1. Do the capacitors C_{IN} connect to the power PV_{IN} and power PGND as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.
2. Are C_{OUT} and L1 closely connected? The (–) plate of C_{OUT} returns current to PGND and the (–) plate of C_{IN}.
3. The resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line terminated near SGND. The feedback signal V_{FB} should be routed away from noisy components and traces, such as the SW line, and its trace should be minimized. Keep R1 and R2 close to the IC.
4. Solder the Exposed Pad (Pin 25) on the bottom of the package to the PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the ASP3605.
5. Keep sensitive components away from the SW pin. The RT resistor, the compensation

capacitor C_C and C_{COMP} and all the resistors R1, R3 and RC, and the $INTV_{CC}$ bypass capacitor, should be placed away from the SW trace and the inductor L1. Also, the SW pin pad should be kept as small as possible.

6. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the SGND pin which is then connected to the PGND pin at the negative terminal of the output capacitor, C_{OUT}.

7. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to PGND..

4.19 Design Example

As a design example, consider using the ASP3605 in an application with the following specifications:

V_{IN} = 10.8V ~ 13.2V, V_{OUT} = 1.8V, $I_{OUT(MAX)}$ = 5A, $I_{OUT(MIN)}$ = 500mA, f = 2MHz。

Because efficiency is important at both high and low load current, discontinuous mode operation will be utilized. First select from the characteristic curves the correct RT resistor value for 2MHz switching frequency. Based on that RT should be 80.6k. Then calculate the inductor value for about 50% ripple current at maximum V_{IN}:

$$L = \left(\frac{V_{OUT}}{f \cdot I_{OUT}}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, two 47µF ceramic capacitors will be used.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{V_{IN}}{V_{OUT}}\right)^{1/2}$$

Decoupling the PV_{IN} pins with two 22µF ceramic capacitors is adequate for most applications.

4.20 DCM and FCCM

When the MODE pin is connected to GND and the circuit is under light load conditions, the chip operates in Discontinuous Conduction Mode (DCM).

Conversely, when the MODE pin is connected to $INTV_{CC}$, the circuit operates in Forced Continuous Conduction Mode (FCCM) regardless of the output load.

4.21 RUN Enable Pin

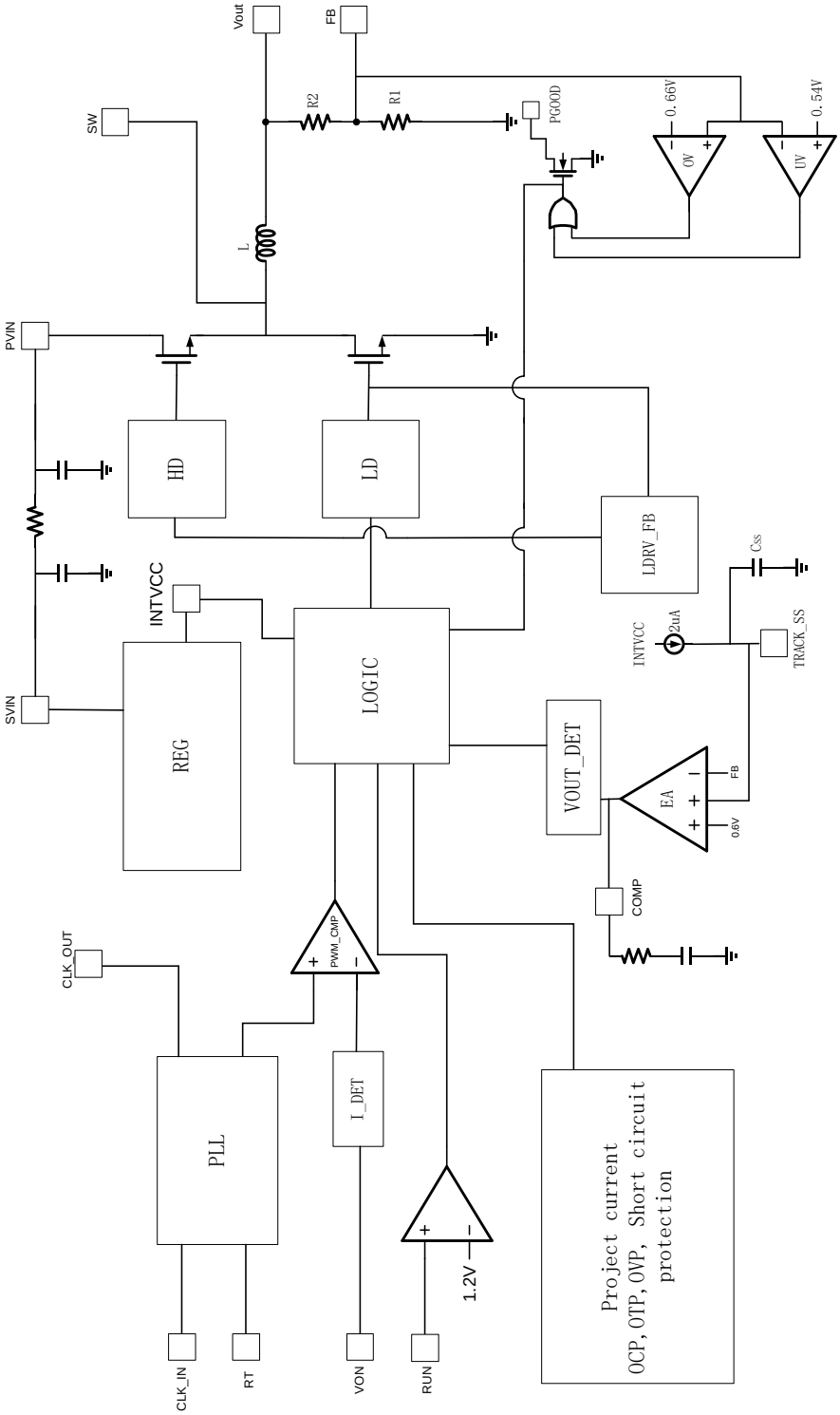
The RUN pin has a typical threshold voltage of approximately 1.2V. When the RUN pin is pulled to GND, the module enters a shutdown state, during which the power MOSFET and most internal control circuits are turned off.

When the RUN pin voltage is greater than or equal to 0.7V, only the internal reference

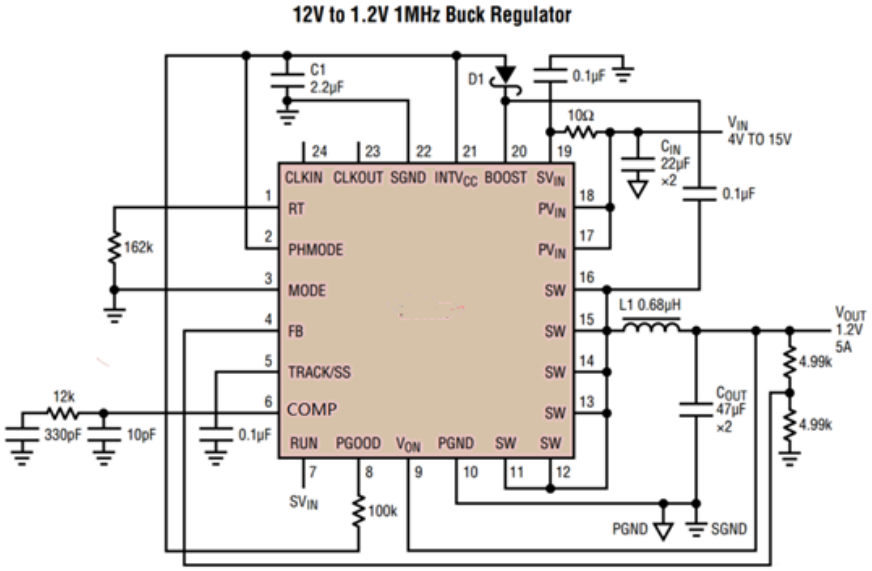
voltage is enabled, while the power MOSFET remains off.

The chip will only enter normal operation mode when the RUN pin voltage is greater than or equal to 1.2V.

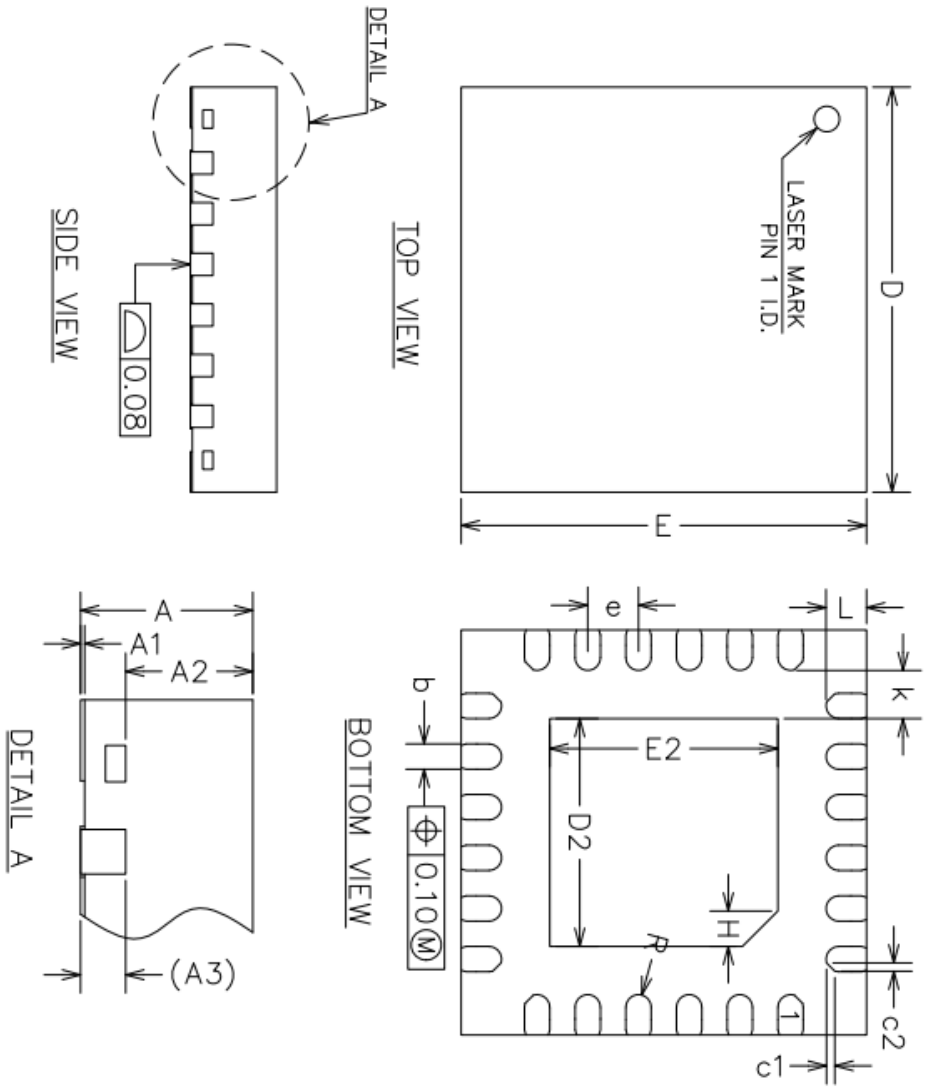
5 BLOCK DIAGRAM



6 TYPICAL APPLICATIONS



7 PACKAGE DESCRIPTION



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.15	2.25	2.35
E2	2.15	2.25	2.35
e	0.40	0.50	0.60
H		0.35REF	
K	0.30	–	–
L	0.35	0.40	0.45
R	0.09	–	–
c1	–	0.08	–
c2	–	0.08	–

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDRAD MO-220 VVGGD-8.DO NOT INCLUDE MOLD FLASH OR PROTRUSION.