ANSILIC

ASM1042 Datasheet

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1 Features

- AEC-Q100 (Level 1) support: Meets automotive application requirements
- Complies with ISO 11898-2:2016 and ISO 11898-5:2007 Physical layer standards, provides functional safety
  - Documentation to help with functional safety system design
- Support 5Mbps
  - With a short symmetric propagation delay time and a fast number of cycles, the timing margin can be increased
  - Faster data rates in loaded CAN networks
- EMC Performance: Support SAE J2962-2 and IEC 62228-3 (up to 500kbps) without a common mode choke
- The I/O voltage range supports 3.3V and 5V MCUS
- Ideal passive behavior when unpowered
  - Bus and logic pins in high resistance (no load)
  - Uninterrupted operation and protection on/off bus and RXD outputs
  - IEC ESD protection up to ±15kV
  - Bus fault protection: ±58V (non-H model) and ±70V (H model)
  - VCC and VIO (V models only) power terminals have undervoltage protection
  - Drive Explicit Timeout (TXD DTO) - Data rates as low as 10kbps
  - Thermal shutdown Protection (TSD)
- Receiver common-mode input voltage: ±30V
- Typical loop delay: 110ns
- The junction temperature ranges from -55℃ to 150℃

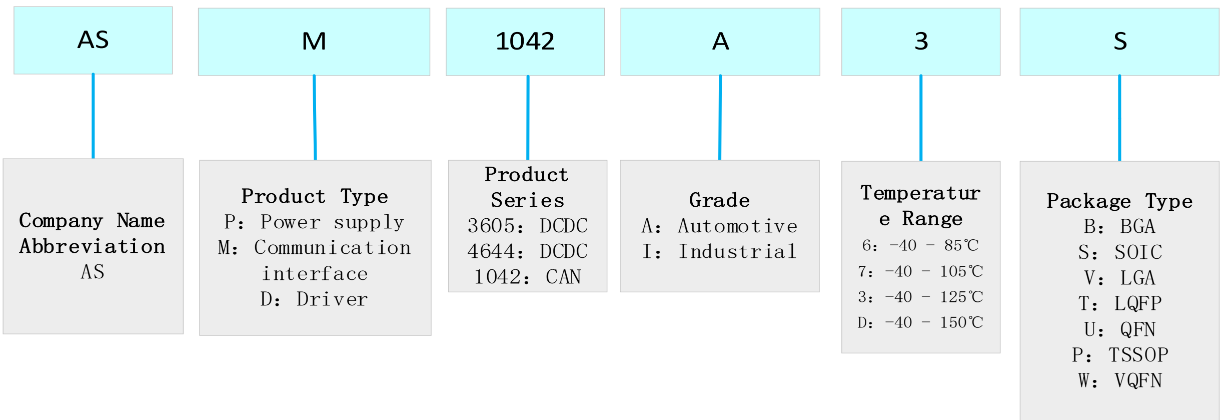
2 Product Description

This CAN transceiver family complies with the ISO1189-2 (2016) High Speed CAN (Controller Local Area Network) physical layer standard. All devices are designed for CAN FD networks with data rates up to 2Mbps (megabits per second). The transceiver supports a data rate of 5Mbps and provides an auxiliary power input for I/O levels to set input pin thresholds and RXD output levels. The series features low power standby mode and remote wake request. In addition, the device offers a variety of protection features to improve the durability of the device and network.

Chip models are as follows:

Chip type	Chip Model	Grade	Package
Communication interface chip	ASM1042A3S	Automotive	SOIC8
Communication interface chip	ASM1042I6S	Industrial	SOIC8

Chip Naming Rule



Parameters	Symbol	Min.	Max.	Unit
Bus supply voltage	VCC	-0.3	7	V
Supply voltage of the I/O port	VIO	-0.3	7	V
CAN bus I/O voltage range	VBUS	-70	70	V

Max. pressure difference between CANH and CANL	V(Diff)	-70	70	V
Voltage range of the logical port	VTXD、VSTB、VRXD	-0.3	7	V
RXD Output current	IO(RXD)	-8	8	mA
Junction temperature	TJ	-55	150	℃

3 Pin definition

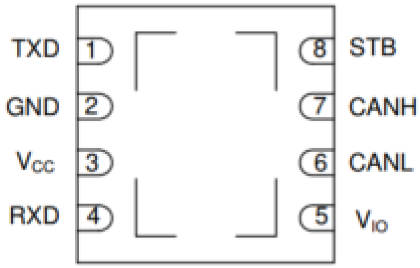


Figure 1 Pin distribution of FD CAN chip

Pin number	Pin name	Pin function
1	TXD	Transmitter data input side
2	GND	Ground
3	VCC	Receiver power supply
4	RXD	Receiver input
5	VIO	Receiver I/O power supply
6	CANL	Low potential CAN input and output
7	CANH	High potential CAN input and output
8	STB	Standby mode the control terminal, high level are in standby mode

4 Internal circuit structure diagram

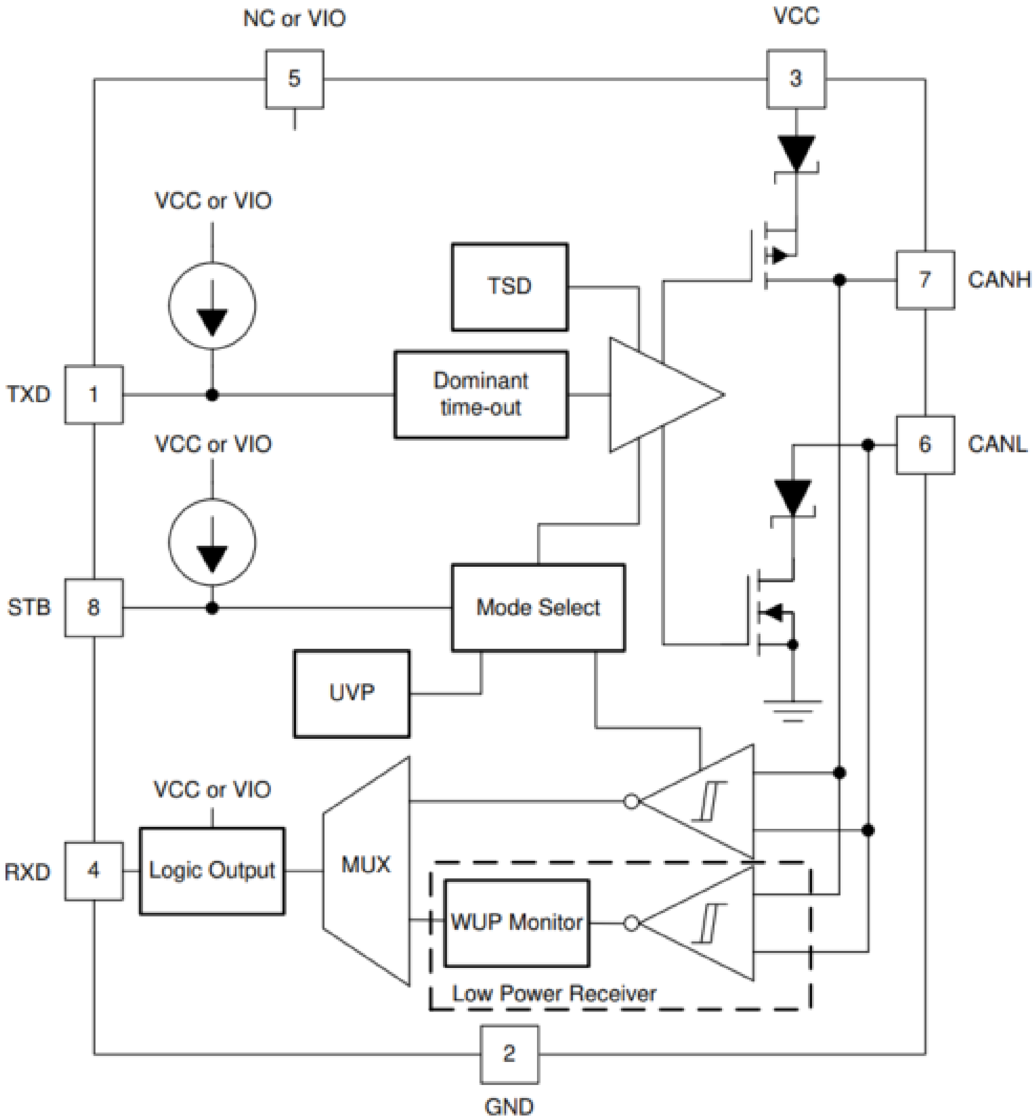


Figure 2 Block diagram of internal circuit structure

5 Bus transceiver electrical characteristics

Basic parameters

Characteristics	Symbol	Limit/standard value			Unit
		Min.	Typical	Max.	
Dominant power consumption (Normal mode), TXD=0V, R_L=60Ω, C_L=open, R_{CM}=open, STB=0V, The load conditions are shown in Figure 3.			40	70	
Bus fault explicit power consumption (Normal mode), TXD=0, V_{CANH}=-12V, R_L=open, C_L=open, R_{CM}=open, The load conditions are shown in Figure 3.				110	mA
Recessive power consumption (Normal mode), TXD=V_{CC} or V_{IO}, R_L=50Ω, C_L=open, R_{CM}=open, STB=0V, The load conditions are shown in Figure 3.	I_{CC}		1.5	2.5	
Power consumption when the load is a V device (Standby mode), TXD=V_{IO}, R_L=50Ω, C_L=open, R_{CM}=open, STB=V_{IO} , The load conditions are shown in Figure 3.			0.5	5	
Power consumption of a device without a V model (Standby mode), TXD=V_{CC}, R_L=50Ω, C_L=open, R_{CM}=open, STB=VCC, The load conditions are shown in Figure 3.				22	μA
I/O Power consumption (Normal mode)	I_{IO}		90	300	

I/O Power consumption (Standby mode)			12	17	
V_{CC} Undervoltage protection rise threshold voltage	UV_{CC}		4.2	4.4	V
V_{CC} Undervoltage protection drop threshold voltage		3.8	4.0	4.25	
U_{VCC} Hysteretic voltage	$V_{HYS(UVVCC)}$		200		mV
V_{IO} Undervoltage protection threshold	UV_{VIO}	1.3		2.75	V
U_{VVIO} Hysteretic voltage	$V_{HYS(UVVIO)}$		80		mV
Dominant output voltage (Normal mode) 50Ω≤R_L≤65Ω，C_L=open，R_{CM}=open, The load conditions are shown in Figure 3.	V_{CANH}	2.75		4.5	V
	V_{CANL}	0.5		2.25	
	V_{CANH}-V_{CANL}	1.5		3	
Recessive output voltage (Normal mode) TXD=V_{CC} or V_{IO}，V_{IO}=V_{CC}，STB=0V，R_L=open(no load)，R_{CM}=open, The load conditions are shown in Figure 3.	V_{CANH} and V_{CANL}	2	0.5×VCC	3	
	V_{CANH}-V_{CANL}	-50		50	mV
Output voltage (Standby mode) STB=V_{IO}，R_L=open(no load)，R_{CM}=open, The load conditions are shown in Figure 3.	V_{CANH}	-0.1	0	0.1	V
	V_{CANL}	-0.1	0	0.1	
	V_{CANH}-V_{CANL}	-0.2	0	0.2	
Output level matching	V_{SYM}	0.9		1.1	V/V
Dc output level matching	V_{SYM_DC}	-0.4		0.4	V
Dominant short-circuit output current (Normal mode)，VCANH=-5V~40V，CANL=open	$I_{OS(SS\_DOM)}$	-100			mA
Dominant short-circuit output current (Normal mode)，V_{CANH}=-5V~40V，CANL=open				100	
Recessive short-circuit output current (Normal	$I_{OS(SS\_REC)}$	-5		5	

mode), $V_{BUS}=V_{CANH}=V_{CANL}$, -27V≤VBUS≤32V					
Loop delay (recessive to dominant), the load conditions are shown in Figure 5.	$t_{PROP(LOOP1)}$		100	160	ns
Loop delay (recessive to dominant), the load conditions are shown in Figure 5.	$t_{PROP(LOOP2)}$		110	175	
Mode switching time from Normal to Standby	t_{MODE}		9	45	μs
Filter mode wakeup time	t_{WK_FILTER}	0.5		1.8	
Transmission delay(recessive to dominant), the load conditions are shown in Figure 3. R_L=60Ω, CL=100pF, CL(RXD)=15pF。	t_{pHR}		55		ns
Transmission delay(dominant to recessive), the load conditions are shown in Figure 3. R_L=60Ω, CL=100pF, CL(RXD)=15pF。	t_{pLD}		75		
Dominant Timeout	t_{TXD_DTO}	1.2		3.8	ms
Transmission delay(recessive to dominant), the load conditions are shown in Figure 4. $C_{L(RXD)}$=15pF。	t_{pRH}		65		ns
Transmission delay(dominant to recessive), the load conditions are shown in Figure 4. $C_{L(RXD)}$=15pF。	t_{pDL}		50		
CAN bus pin human body discharge model (HBM)	V_{ESD_HBM}		±6000		V
Module charging model (CDM)	V_{ESD_CDM}		±1500		
Mechanical model (MM)	V_{ESD_MM}		±200		

6 Test circuit waveform timing diagram

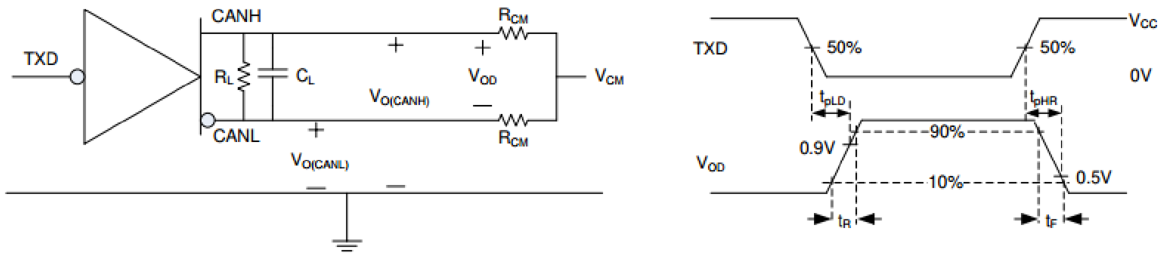


Figure 3 FDCAN transmit test circuit and timing diagram

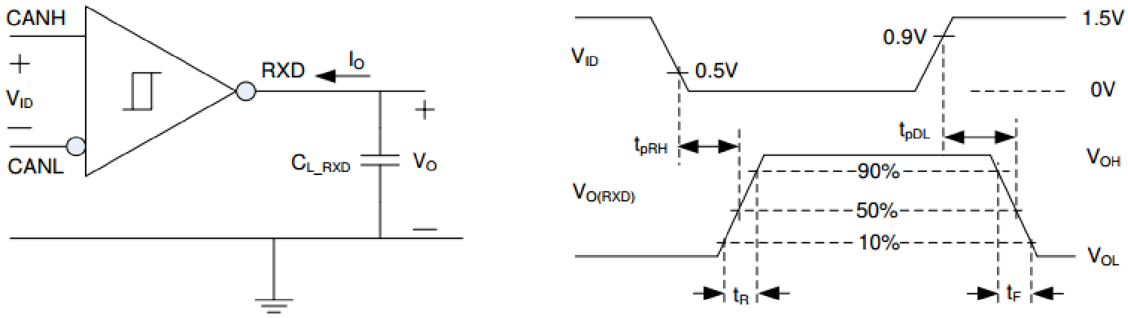


Figure 4 FDCAN receiving test circuit and timing diagram

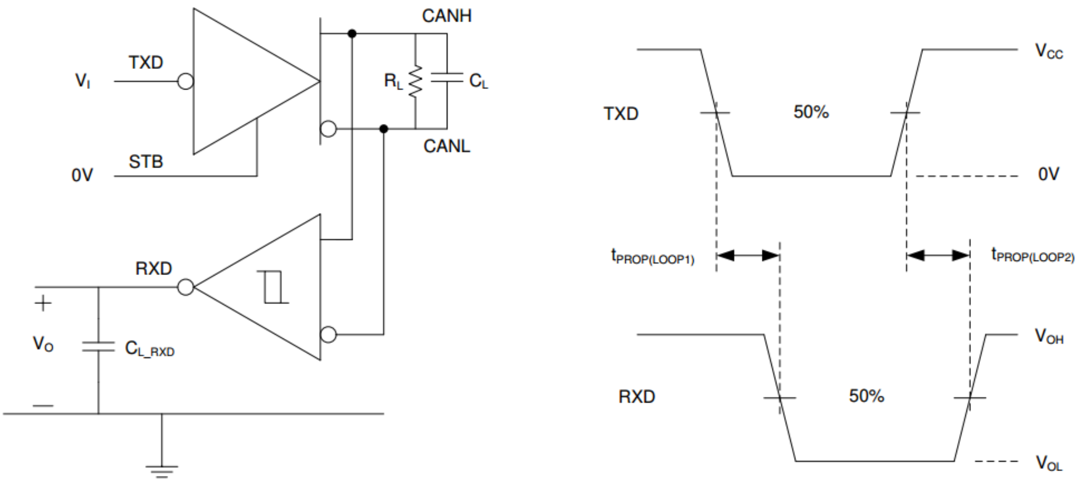


Figure 5 Loop delay time simulation circuit and timing diagram

7 Note

1 Over-temperature protection

The transceiver chip has the function of overtemperature protection. When the overtemperature protection is triggered, the drive circuit will be closed, the drive current will be reduced, and the chip temperature will be reduced.

2 Under voltage protection

The transceiver chip VCC and VIO power pins both feature undervoltage protection to protect the bus when the VCC and VIO voltages fall below the threshold voltage.

3 Standby mode

Standby mode can be activated when STB is set to high power level. Both the CAN driver and receiver are turned off at this time to save power. The STB high level signal activates the low power receiver and wake filter, and when the bus detects a primary bus level that exceeds the tWK_FILTER, the pin RXD changes to low.

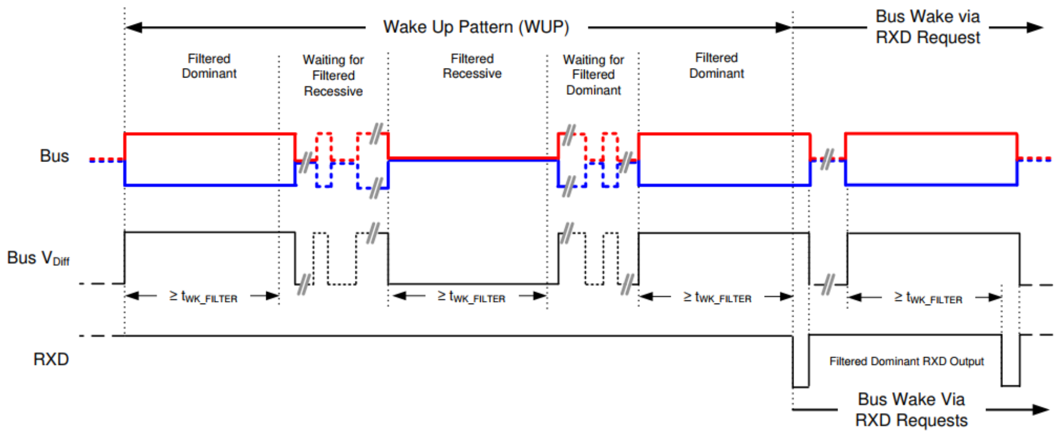


Figure 6 Wake up timing

4 Explicit timeout function

When the low-level duration on pin TXD exceeds tTXD_DTO, the transmitter is disabled and the CAN bus enters a hidden state to prevent network congestion caused by application failure on pin TXD. The TXD rising edge signal resets the dominant timeout protection.

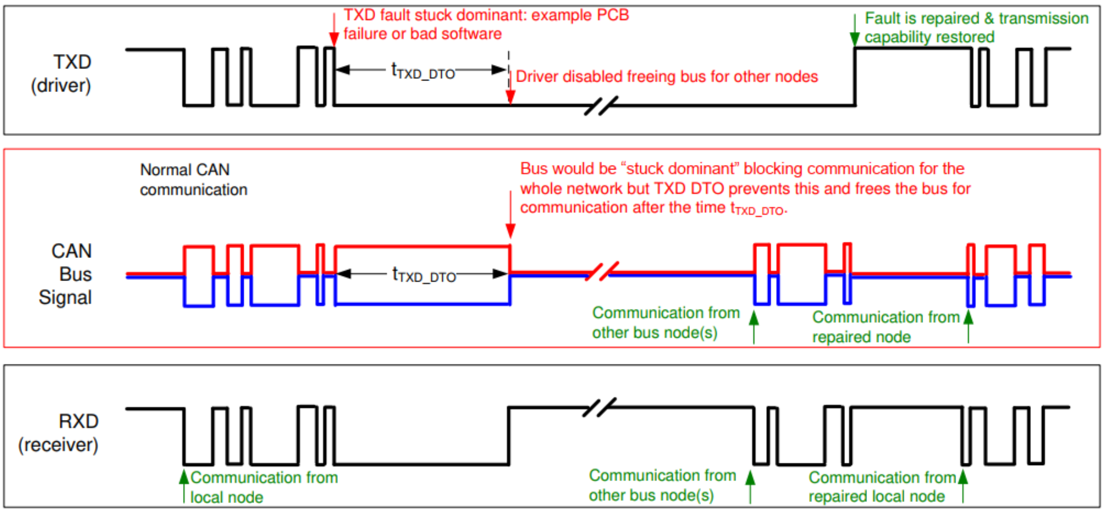


Figure 7 Sequence of explicit timeout protection

单击下面可查看定价，库存，交付和生命周期等信息

[>>ANSILIC(国科安芯)]