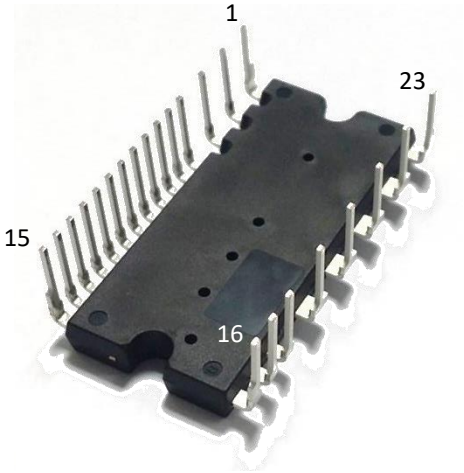
AIM5D10B060M1
AIM5D10B060M1S

Dual-In-Line Package
Intelligent Power Module

External View



Size: 33.4 x 15 x 3.6 mm

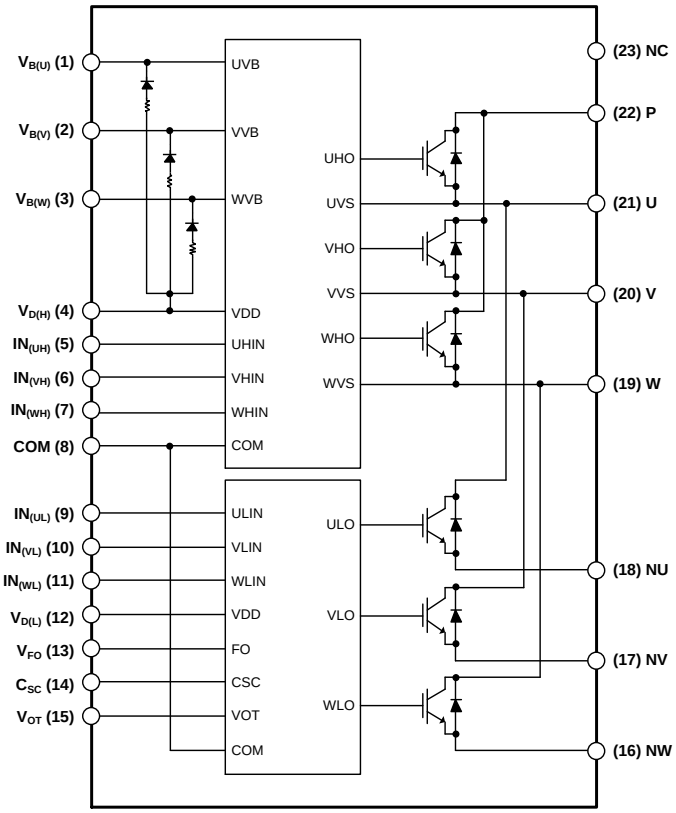
Features and Functions

- UL Recognized: UL1557 File E345245
- 600V-10A (Trench Shielded Planar Gate IGBT)
- 3 phase Inverter module including HVIC drivers
- Built-in bootstrap diodes with integrated current limiting resistor
- Control supply under-voltage lockout protection (UVLO)
- Over-temperature (OT) protection (V_{OT}) – pin open
- Temperature monitoring (V_{OT}) – 10kΩ resistor connection
- Short-circuit current protection (C_{SC})
- Fault out signal (V_{FO}) corresponding to SC, UV and OT fault
- Wide input interface (3-18V), Schmitt trigger receiver circuit (Active High)
- Isolation ratings of 2000Vrms/min

Applications

- AC 100-240Vrms class low power motor drives like refrigerators, dishwashers, fan motors, washing machines and air-conditioners

Internal Equivalent Circuit



Green

Ordering Information

Part Number	Temperature Range	Package	Description
AIM5D10B060M1	-40°C - +150°C	IPM-5	Normal pin length
AIM5D10B060M1S	-40°C - +150°C	IPM-5A	Short pin length

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Description

Part Number	Pin Name	Pin Function
1	$V_{B(U)}$	High-Side Bias Voltage for U-Phase IGBT Driving
2	$V_{B(V)}$	High-Side Bias Voltage for V-Phase IGBT Driving
3	$V_{B(W)}$	High-Side Bias Voltage for W-Phase IGBT Driving
4	$V_{D(H)}$	High-Side Common Bias Voltage for IC and IGBTs Driving
5	$IN_{(UH)}$	Signal Input for High-Side U-Phase
6	$IN_{(VH)}$	Signal Input for High-Side V-Phase
7	$IN_{(WH)}$	Signal Input for High-Side W-Phase
8	COM	Common Supply Ground
9	$IN_{(UL)}$	Signal Input for Low-Side U-Phase
10	$IN_{(VL)}$	Signal Input for Low-Side V-Phase
11	$IN_{(WL)}$	Signal Input for Low-Side W-Phase
12	$V_{D(L)}$	Low-Side Common Bias Voltage for IC and IGBTs Driving
13	V_{FO}	Fault Output
14	C_{SC}	Capacitor (Low-Pass Filter) for Short-circuit Current Detection Input
15	V_{OT}	Over-Temperature Output
16	NW	Negative DC-Link Input for W-Phase
17	NV	Negative DC-Link Input for V-Phase
18	NU	Negative DC-Link Input for U-Phase
19	W	Output for W-Phase
20	V	Output for V-Phase
21	U	Output for U-Phase
22	P	Positive DC-Link Input
23	NC	No Connection

Absolute Maximum Ratings (T_J=25°C, Unless Otherwise Specified)

Symbol	Parameter	Conditions	Ratings	Units
Inverter Part				
V_{PN}	Supply voltage	Applied between P - NU,NV,NW	450	V
$V_{PN(surge)}$	Supply voltage (surge)	Applied between P - NU,NV,NW	500	V
V_{CES}	Collector-emitter voltage		600	V
I_C	Output phase current	T_C=25°C, T_J<150°C	10	A
		T_C=100°C, T_J<150°C	5	A
$\pm I_{PK}$	Output peak phase current	T_C=25°C, less than 1ms pulse width	20	A
t_{SC}	Short circuit withstand time	V_{PN}≤400V, T_J=150°C, V_D=15V (Note 1)	5	µs
P_C	Collector dissipation	T_C=25°C, per 1 chip	23	W
T_J	Operating junction temperature		-40 - +150	°C
Control (Protection) Part				
V_D	Control supply voltage	Applied between $V_{D(H)}$-COM, $V_{D(L)}$-COM	25	V
V_{DB}	High-side control bias voltage	Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	25	V
V_{IN}	Input voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM	V_D±0.5	V
V_{FO}	Fault output supply voltage	Applied between V_{FO} - COM	V_D±0.5	V
I_{FO}	Fault output current	Sink current at V_{FO} terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between C_{SC} - COM	5±0.5	V
V_{OT}	Temperature output	Applied between V_{OT} - COM	5±0.5	V
Total System				
$V_{PN(PROT)}$	Self protection supply voltage limit (Short-circuit protection capability)	V_D=13.5-16.5V, Inverter part T_J=150°C, Non-repetitive, less than 2µs	400	V
T_C	Module case operation temperature	Measurement point of T_C is provided in Figure 1	-30 - +125	°C
T_{STG}	Storage temperature		-40 - +150	°C
V_{ISO}	Isolation voltage	60Hz, sinusoidal, AC 1min, between connected all pins and heat sink plate	2000	V_{rms}

Note:

1. Allowed number of short circuits: <1000; time between short circuit: >1s.

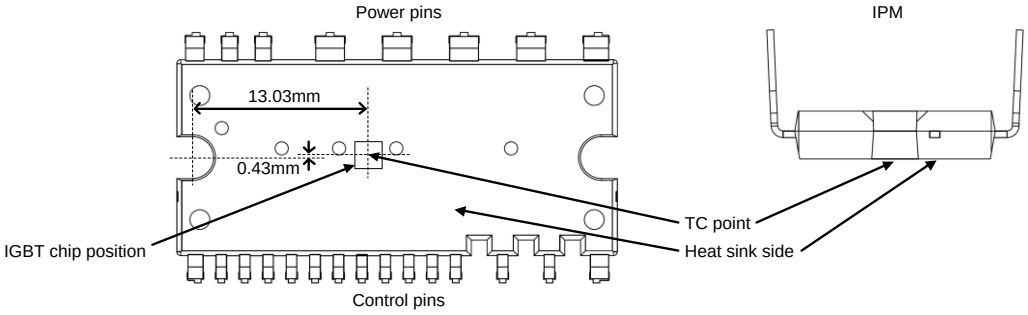


Figure 1. T_C Measurement Point

Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 2)	Inverter IGBT part (per 1/6 module)	-	-	5.4	K/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	-	-	6.9	K/W

Note:

2. For the measurement point of case temperature (T_C), please refer to Figure 1.

Electrical Characteristics (T_J=25°C, Unless Otherwise Specified)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Inverter Part							
$V_{CE(SAT)}$	Collector-emitter saturation voltage	V_D=V_{DB}=15V, V_{IN}=5V	I_C=5A, T_J=25°C	-	1.60	2.00	V
			I_C=5A, T_J=125°C	-	1.90	-	V
V_F	FWD forward voltage	V_{IN}=0	I_F=5A, T_J=25°C	-	1.48	1.90	V
t_{ON}	Switching times	V_{PN}=300V, V_D=V_{DB}=15V I_C=5A, T_J=25°C, V_{IN}=0V ↔ 5V Inductive load (high-side)		0.30	0.60	1.10	µs
$t_{C(ON)}$				-	0.10	0.20	µs
t_{OFF}				-	1.00	1.50	µs
$t_{C(OFF)}$				-	0.20	0.40	µs
t_{rr}				-	0.30	-	µs
I_{CES}	Collector-emitter leakage current	V_{CE}=V_{CES}	T_J=25°C	-	-	1	mA
			T_J=125°C	-	-	10	mA
Control (Protection) Part							
I_{QDH}	Quiescent V_D supply current	$V_{D(H)}$=15V, $IN_{(UH, VH, WH)}$=0V	$V_{D(H)}$ - COM	-	-	0.1	mA
I_{QDL}		$V_{D(L)}$=15V, $IN_{(UL, VL, WL)}$=0V	$V_{D(L)}$ - COM	-	-	2.1	mA
I_{QDB}	Quiescent V_{DB} supply current	V_{DB}=15V, $IN_{(UH, VH, WH)}$=0V	$V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$- W	-	-	0.3	mA
$V_{SC(ref)}$	Short-circuit trip level	V_D=15V (Note 3)		0.455	0.480	0.505	V
UV_{DT}	Supply circuit under-voltage protection	Trip level		9.0	10.0	11.0	V
UV_{DR}		Reset level		10.0	11.0	12.0	V
UV_{DBT}		Trip level		8.5	9.5	10.5	V
UV_{DBR}		Reset level		9.5	10.5	11.5	V
V_{OT}	Temperature output	Pull down R=10kΩ (Note 4)	LVIC temperature=90°C	2.74	2.92	3.10	V
			LVIC temperature=25°C	1.06	1.25	1.43	V
OT_T	Over-temperature protection (Note 5)	V_D=15V, detect LVIC temperature	Trip level	100	120	140	°C
OT_{HYS}			Hysteresis of trip reset	-	10	-	°C
V_{FOH}	Fault output voltage	V_{SC}=0V, V_{FO} circuit: 10kΩ to 5V pull-up		4.9	-	-	V
V_{FOL}		V_{SC}=1V, V_{FO} circuit: 10kΩ to 5V pull-up		-	-	0.5	V
t_{FO}	Fault output pulse width	(Note 6)		20	-	-	µs
I_{IN}	Input current	V_{IN}=5V		-	1.0	-	mA
$V_{th(on)}$	ON threshold voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM			2.3	2.6	V
$V_{th(off)}$	OFF threshold voltage			0.8	1.2		V
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			-	1.1	-	V
$V_{F(BSD)}$	Bootstrap diode forward voltage	I_F=10mA including voltage drop by limiting resistor (Note 7)		1.0	1.5	2.0	V
R_{BSD}	Built-in limiting resistance	Included in bootstrap diode		80	100	120	Ω

Note:

3. Short-circuit protection works only for low-sides.
4. The IPM does not shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that the user defined, the controller (MCU) should stop the IPM. Temperature of LVIC vs. V_{OT} output characteristics is described in Figure 3.
5. When the LVIC temperature exceeds OT Trip temperature level (OT_T), OT protection works and fault outputs.
6. Fault signal F_O outputs when SC, UV or OT protection works. F_O pulse width is different for each protection mode. At SC failure, F_O pulse width is a fixed width (minimum 20µs), but at UV or OT failure, F_O outputs continuously until recovering from UV or OT state. (But minimum F_O pulse width is 20µs).
7. The characteristics of bootstrap diode are described in Figure 2.

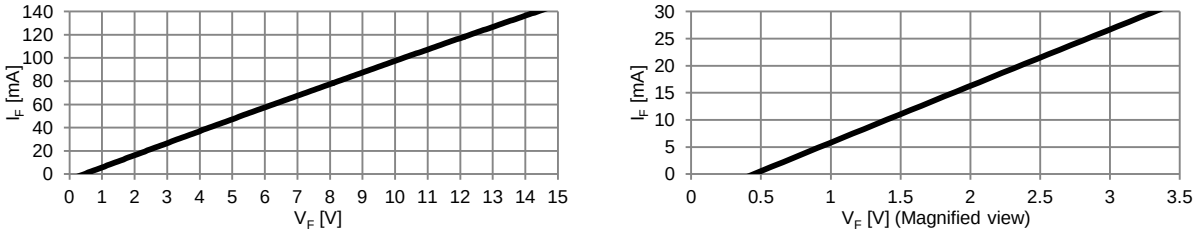


Figure 2. Built-in Bootstrap Diode V_F-I_F Characteristic (@Ta=25°C)

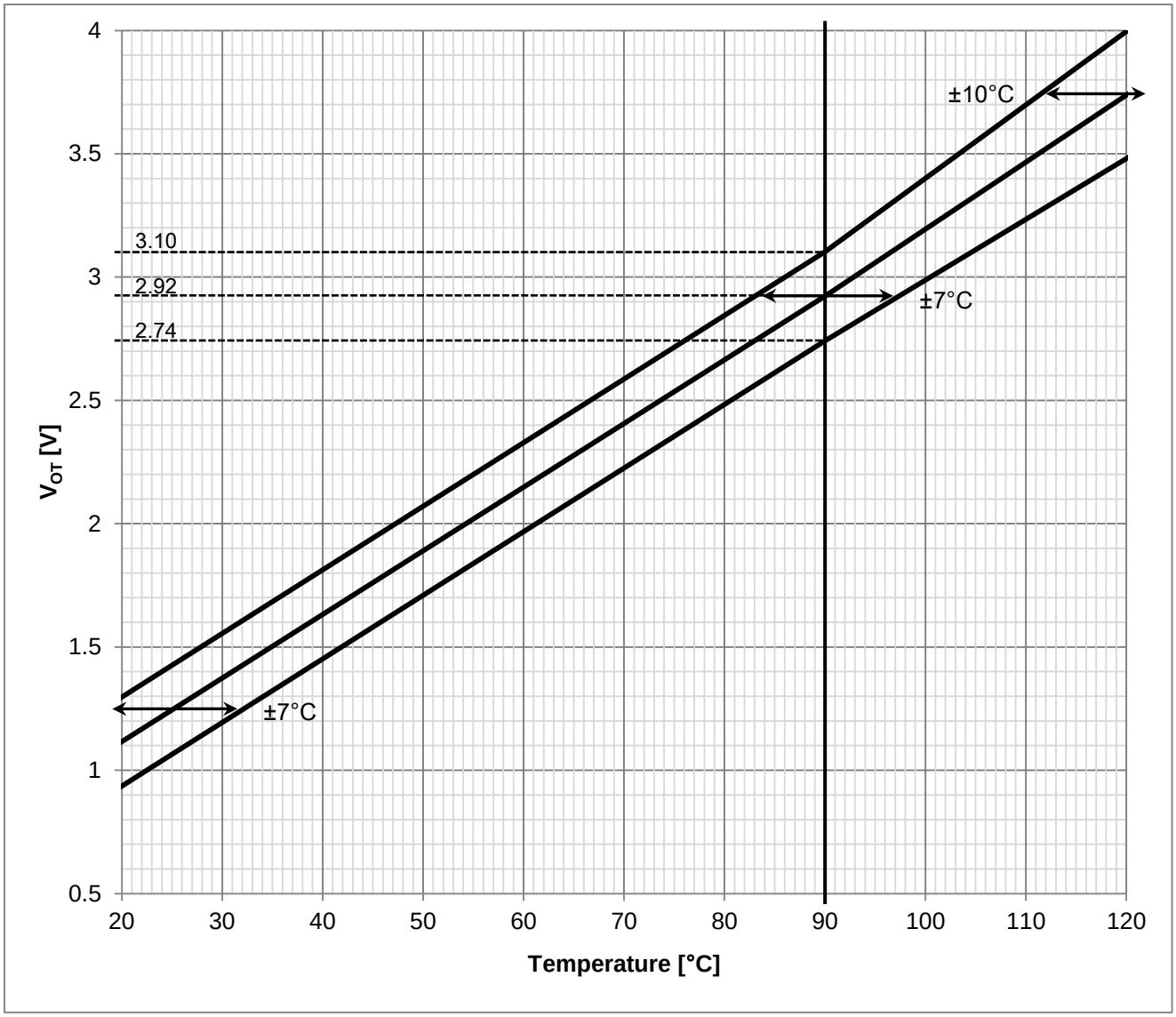
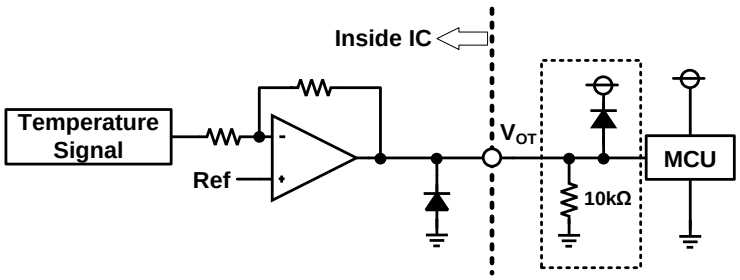


Figure 3. Temperature of LVIC vs. V_{OT} Output Characteristics



(1) Connect 10kΩ to V_{OT} pin if temperature monitoring function is used and leave the V_{OT} pin open (no connect) if not using temperature monitoring and use internal over-temperature shutdown function.

(2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp diode between control supply of the controller and V_{OT} output for preventing over voltage destruction.

Figure 4. V_{OT} Output Circuit

Mechanical Characteristics and Ratings

Parameter	Conditions		Min.	Typ.	Max.	Units
Mounting torque	Mounting screw: M3 (Note 8)	Recommended 0.69N m	0.59	0.69	0.78	N m
Weight			-	5.25	-	g
Flatness	Refer to Figure 5		-50	-	100	µm

Note:

8. Plain washers (ISO 7089-7094) are recommended.

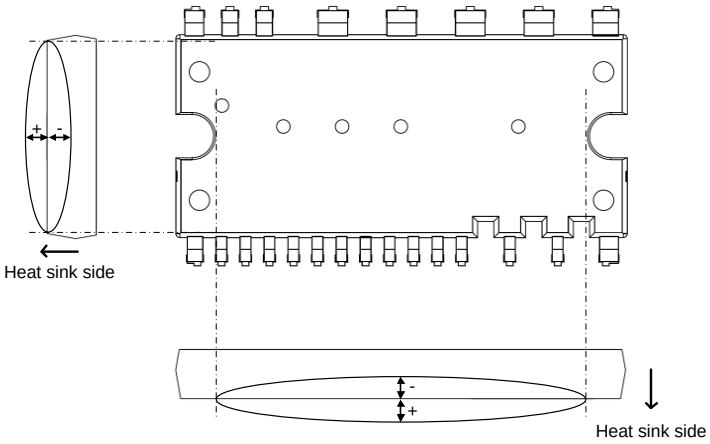


Figure 5. Flatness Measurement Position

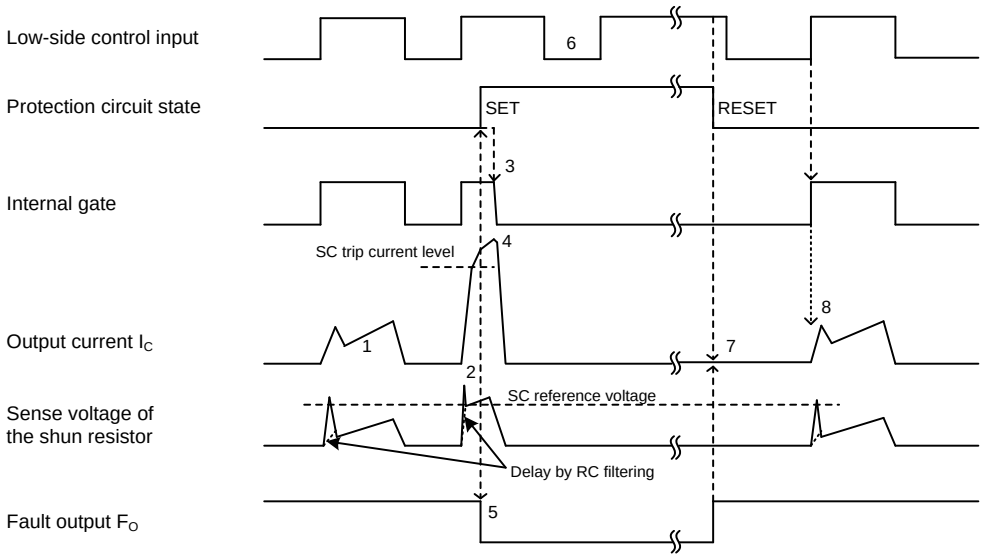
Recommended Operation Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PN}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
V_D	Control supply voltage	Applied between $V_{D(H)}$ – COM, $V_{D(L)}$ - COM	13.5	15.0	16.5	V
V_{DB}	High-side bias voltage	Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	13.5	15.0	18.5	V
dV_D/dt, dV_{DB}/dt	Control supply variation		-1	-	1	V/µs
t_{dead}	Arm shoot-through blocking time	For each input signal	1.0	-	-	µs
f_{PWM}	PWM input frequency	-40°C < T_J < 150°C	-	-	20	kHz
$P_{WIN(ON)}$	Minimum input pulse width	(Note 9)	0.4	-	-	µs
$P_{WIN(OFF)}$			0.4	-	-	µs
COM	COM variation	Between COM - NU, NV, NW (including surge)	-5.0	-	+5.0	V

Note:

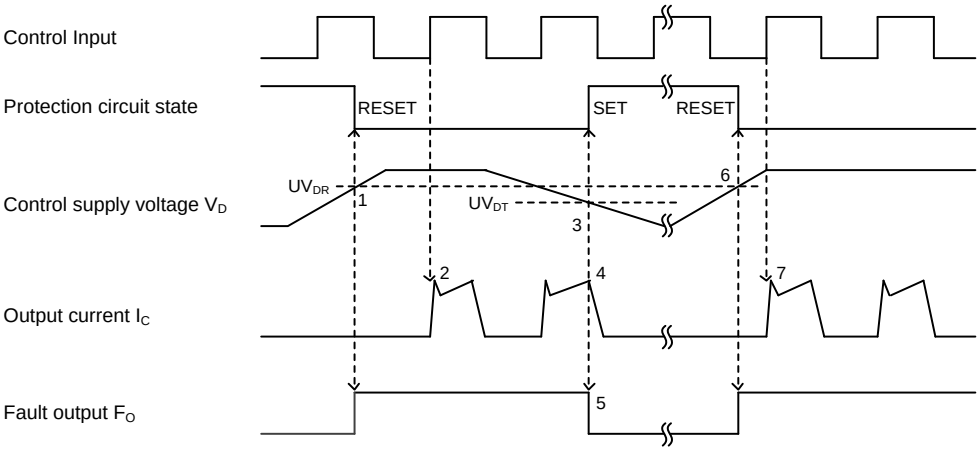
9. IPM might not make response if the input signal pulse width is less than $P_{WIN(ON)}$, $P_{WIN(OFF)}$.

Time Charts of the IPM Protective Function



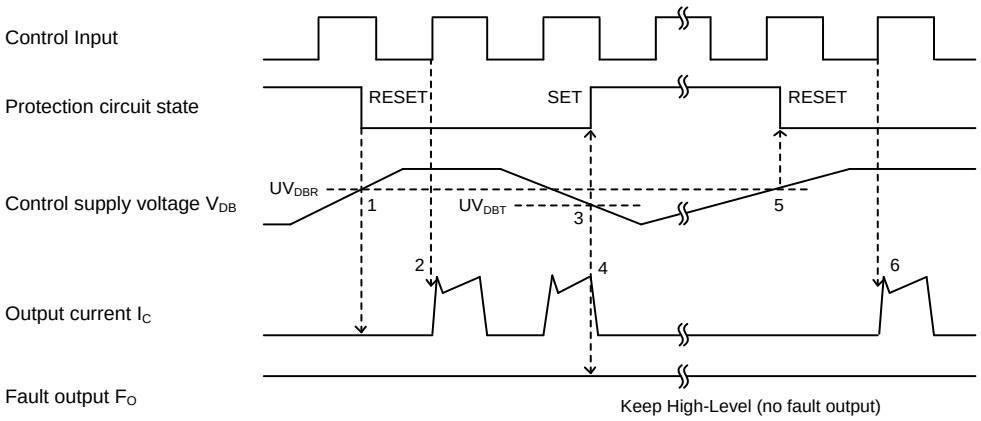
(1) Normal operation: IGBT turns on and outputs current.
(2) Short-circuit current detection (SC trigger).
(3) All low-side IGBT's gates are hard interrupted.
(4) All low-side IGBTs turn OFF.
(5) F_O outputs for t_{FO}=minimum 20μs.
(6) Input = "L" : IGBT OFF.
(7) Fault output finish, but output current will not turn on until next ON signal (L→H).
(8) Normal operation: IGBT turns on and outputs current.

Figure 6. Short-Circuit Protection (Low-side Operation only with the external shunt resistor and RC filter)



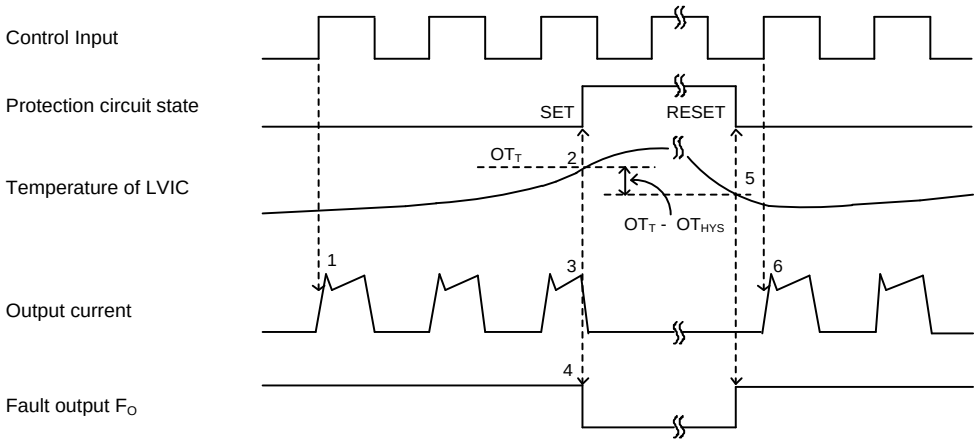
(1) Control supply voltage V_D exceeds under voltage reset level (UV_{DR}), but IGBT turns on by next ON signal (L→H).
(2) Normal operation: IGBT turns on and outputs current.
(3) V_D level drops to under voltage trip level (UV_{DT}).
(4) All low-side IGBTs turn OFF in spite of control input condition.
(5) F_O output for t_{FO}=minimum 20μs, but output is extended during V_D keeps below UV_{DR}.
(6) V_D level reaches UV_{DR}.
(7) Normal operation: IGBT turns on and outputs current.

Figure 7. Under-Voltage Protection (Low-side, UV_D)



(1) Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBR}, IGBT turns on by next ON signal (L→H).
(2) Normal operation: IGBT turns on and outputs current.
(3) V_{DB} level drops to under voltage trip level (UV_{DBT}).
(4) All high-side IGBTs turn OFF in spite of control input condition, but there is no FO signal output.
(5) V_{DB} level reaches V_{DBR}.
(6) Normal operation: IGBT turns on and outputs current.

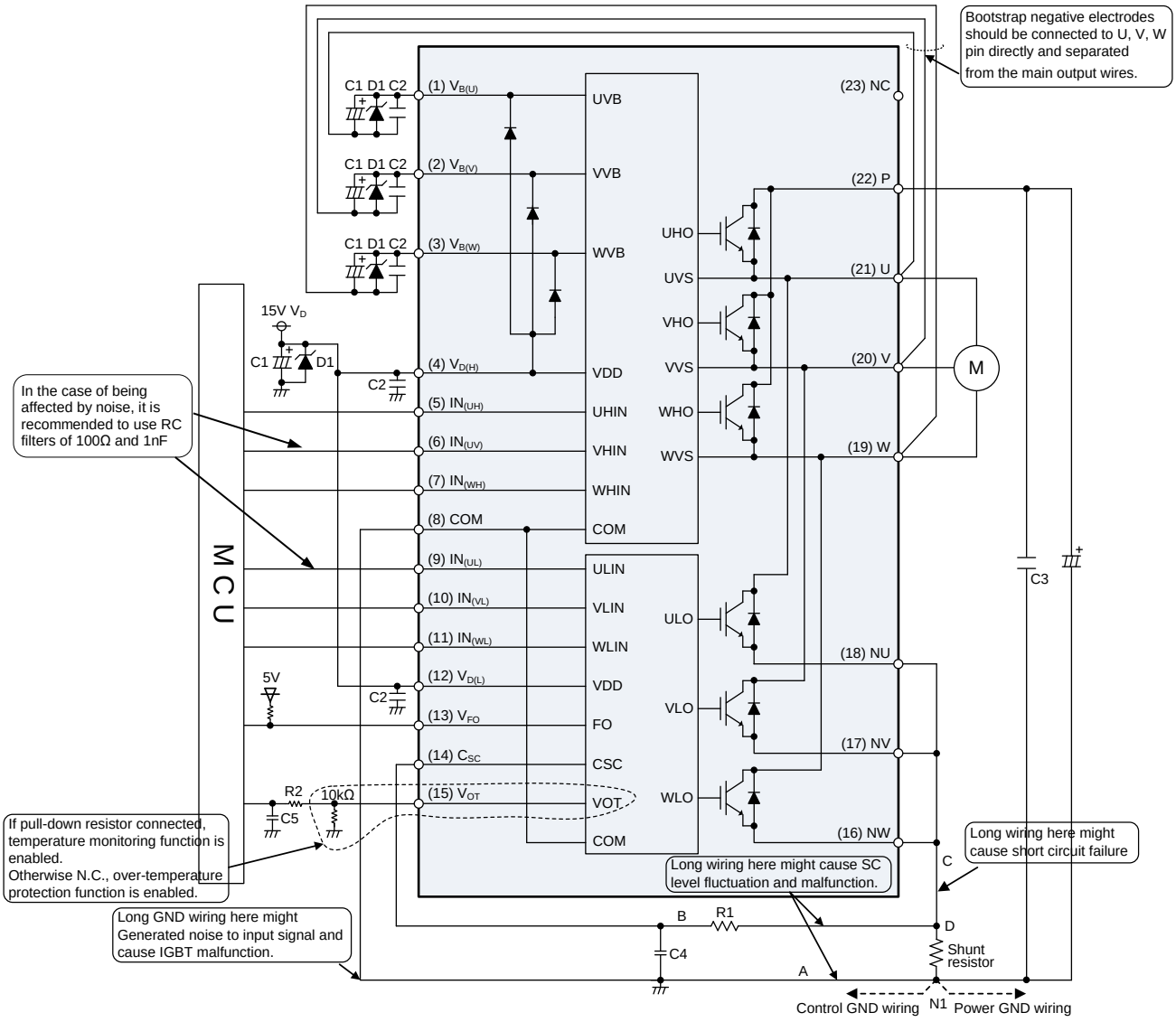
Figure 8. Under-Voltage Protection (High-side, UV_{DB})



(1) Normal operation: IGBT turns on and outputs current.
(2) LVIC temperature exceeds over-temperature trip level (OT_T).
(3) All low-side IGBTs turn OFF in spite of control input condition.
(4) F_O outputs for t_{FO}=minimum 20µs, but output is extended during LVIC temperature keeps over OT_T.
(5) LVIC temperature drops to over-temperature reset level.
(6) Normal operation: IGBT turns on by the next ON signal (L→H).

Figure 9. Over-Temperature Protection (Low-side, Detecting LVIC Temperature)

Example of Application Circuit



(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to control GND and power GND at only a point N1 (near the terminal of shunt resistor).

(2) It is recommended to insert zener diode D1 (24V/1W) between each pair of control supply pins to prevent surge destruction.

(3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

(4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1*C4 should be set so that SC current is shut down within 2μs. (1.5-2μs is general value). SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.

(5) R2, C5 of RC filter for temperature monitoring is recommended to select tight tolerance, temp-compensated type. The time constant R2C5 should be set so that V_{OT} has noise immunity. Recommended values of R2 and C5 are 2kΩ and 10nF (10 to 30μs range of time constant).

(6) To prevent malfunction, the wiring of A, B, C should be as short as possible.

(7) The point D at which the wiring to CSC filter is divided should be near the terminal of shunt resistor.

(8) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2: 0.1-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended).

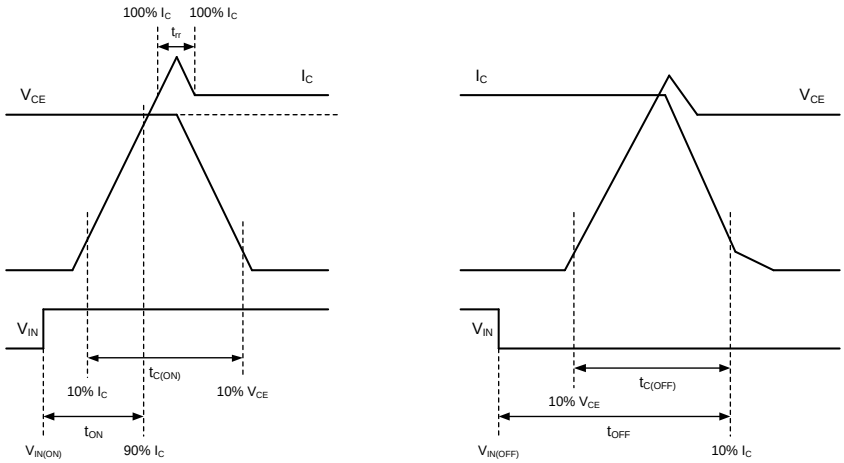
(9) Input drive is high-active type. There is a minimum 3.5kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

(10) V_{FO} output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V, 15V) by a resistor that makes I_{FO} up to 1mA. (I_{FO} is estimated roughly by the formula of control power supply voltage divided by pull-up resistor. In the case of pulled up to 5V, 10kΩ (over 5kΩ) is recommended).

(11) Thanks to build-in HVIC, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

(12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause IPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤ ±1V/μs, Vripple ≤ 2Vp-p.

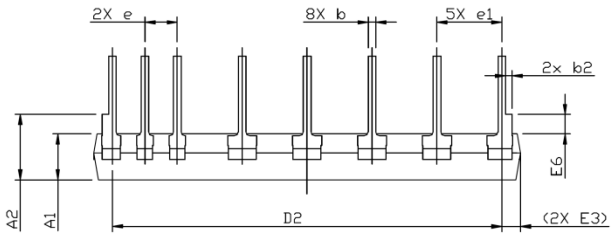
(13) For IPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other IPM.

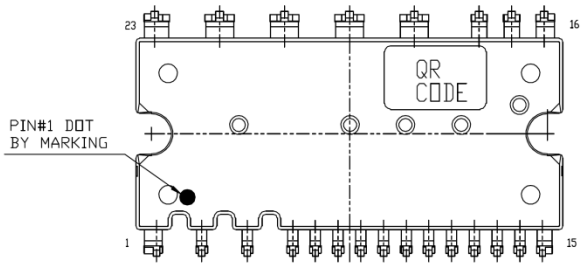


(a) Turn-on waveform **(b) Turn-off waveform**

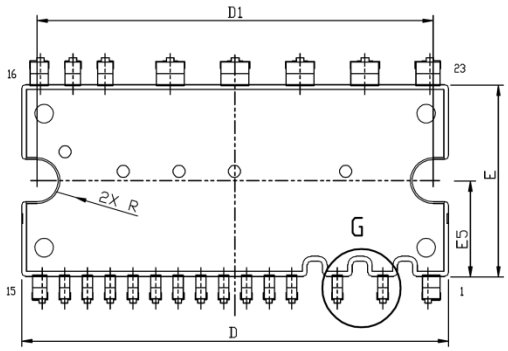
Figure 10. Switching Times Definition

Package Dimensions, IPM-5

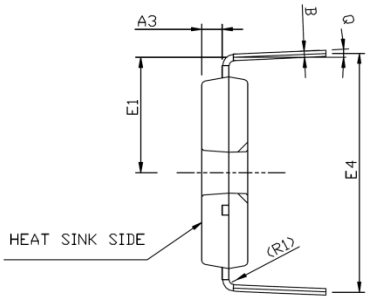


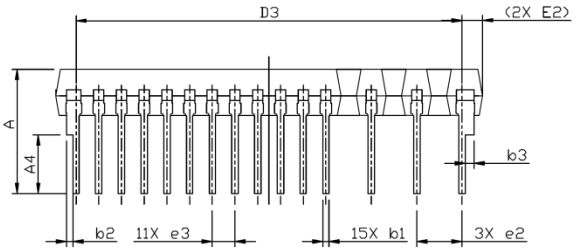


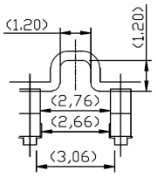
BOTTOM VIEW



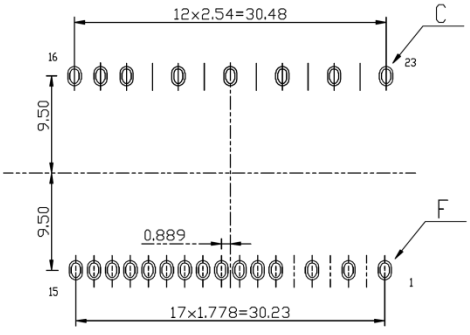
TOP VIEW



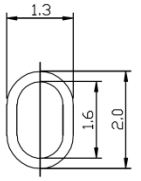




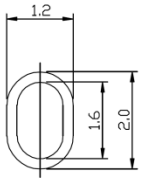
DETAIL G
SCALE 5 : 1



LAND PATTERN RECOMMENDATIONS



DETAIL C
SCALE N/A



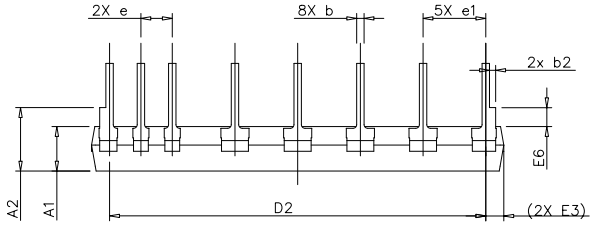
DETAIL F
SCALE N/A

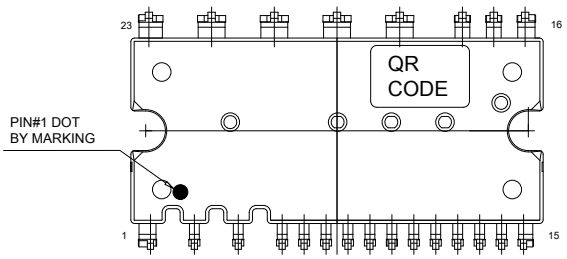
UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	9.30	9.70	10.10	0.366	0.382	0.398
A1	3.30	3.60	3.90	0.130	0.142	0.154
A2	4.70	5.10	5.50	0.185	0.201	0.217
A3	1.50	1.60	1.70	0.059	0.063	0.067
A4	4.20	4.60	5.00	0.165	0.181	0.197
B	0.40	0.50	0.60	0.016	0.020	0.024
b	0.50	0.60	0.70	0.020	0.024	0.028
b1	0.40	0.50	0.60	0.016	0.020	0.024
b2	0.40	0.50	0.60	0.016	0.020	0.024
b3	0.60	0.70	0.80	0.024	0.028	0.032
D	33.10	33.40	33.70	1.303	1.315	1.327
D1	30.80	31.00	31.20	1.213	1.220	1.228
D2	30.18	30.48	30.78	1.188	1.200	1.212
D3	29.93	30.23	30.53	1.178	1.190	1.202
E	14.70	15.00	15.30	0.579	0.591	0.602
E1	8.60	9.00	9.40	0.339	0.354	0.370
E2	1.60 REF			0.063 REF		
E3	1.50 REF			0.059 REF		
E4	18.30	18.70	19.10	0.720	0.736	0.752
E5	7.30	7.50	7.70	0.287	0.295	0.303
E6	1.10	1.50	1.90	0.043	0.059	0.075
e	2.34	2.54	2.74	0.092	0.010	0.108
e1	4.88	5.08	5.28	0.192	0.200	0.208
e2	3.356	3.556	3.756	0.132	0.140	0.148
e3	1.578	1.778	1.978	0.062	0.070	0.078
R	1.50	1.60	1.70	0.059	0.063	0.067
R1	0.40 REF			0.016 REF		
Q	2°-6°			2°-6°		

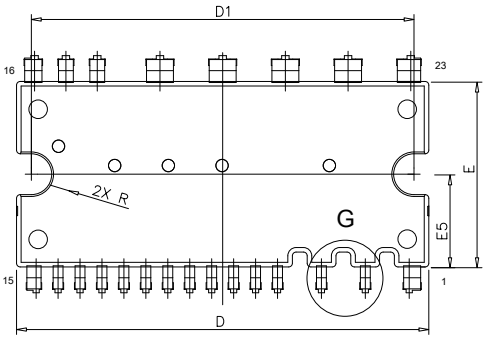
NOTE
A) PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
B) TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
C) CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
D) ( ) IS REFERENCE

Package Dimensions, IPM-5A

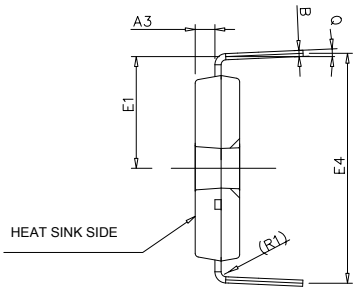


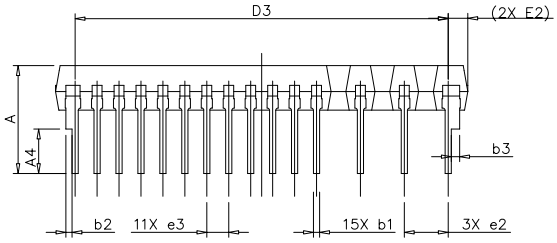


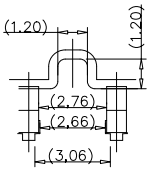
BOTTOM VIEW



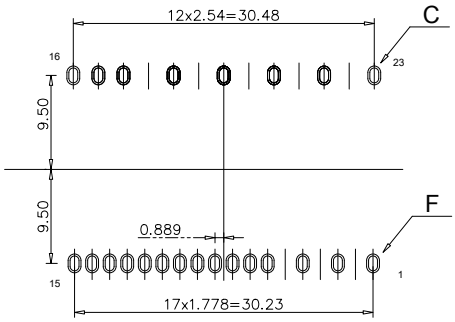
TOP VIEW



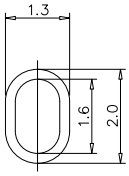




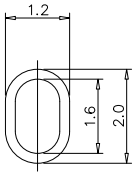
DETAIL G
SCALE 5 : 1



LAND PATTERN RECOMMENDATIONS



DETAIL C
SCALE N/A



DETAIL F
SCALE N/A

UNIT: mm

NOTE
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C) CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
D) ( ) IS For REFERENCE

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	8.30	8.70	9.10	0.326	0.342	0.358
A1	3.30	3.60	3.90	0.130	0.142	0.154
A2	4.70	5.10	5.50	0.185	0.201	0.217
A3	1.50	1.60	1.70	0.059	0.063	0.067
A4	3.20	3.60	4.00	0.125	0.141	0.157
B	0.40	0.50	0.60	0.016	0.020	0.024
b	0.50	0.60	0.70	0.020	0.024	0.028
b1	0.40	0.50	0.60	0.016	0.020	0.024
b2	0.40	0.50	0.60	0.016	0.020	0.024
b3	0.60	0.70	0.80	0.024	0.028	0.032
D	33.10	33.40	33.70	1.303	1.315	1.327
D1	30.80	31.00	31.20	1.213	1.220	1.228
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D3	29.93	30.23	30.53	1.178	1.190	1.202
E	14.70	15.00	15.30	0.579	0.591	0.602
E1	8.60	9.00	9.40	0.339	0.354	0.370
E2	1.60 REF			0.063 REF		
E3	1.50 REF			0.059 REF		
E4	18.20	18.60	19.00	0.716	0.732	0.748
E5	7.30	7.50	7.70	0.287	0.295	0.303
E6	1.10	1.50	1.90	0.043	0.059	0.075
e	2.34	2.54	2.74	0.092	0.010	0.108
e1	4.88	5.08	5.28	0.192	0.200	0.208
e2	3.356	3.556	3.756	0.132	0.140	0.148
e3	1.578	1.778	1.978	0.062	0.070	0.078
R	1.50	1.60	1.70	0.059	0.063	0.067
R1	0.40 REF			0.016 REF		
Q	2°-6°			2°-6°		

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.