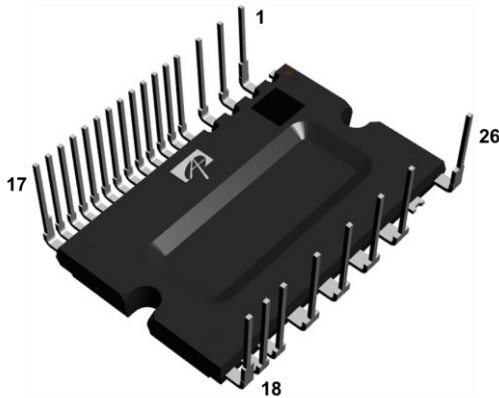


### External View



Size: 38 x 24 x 3.6 mm



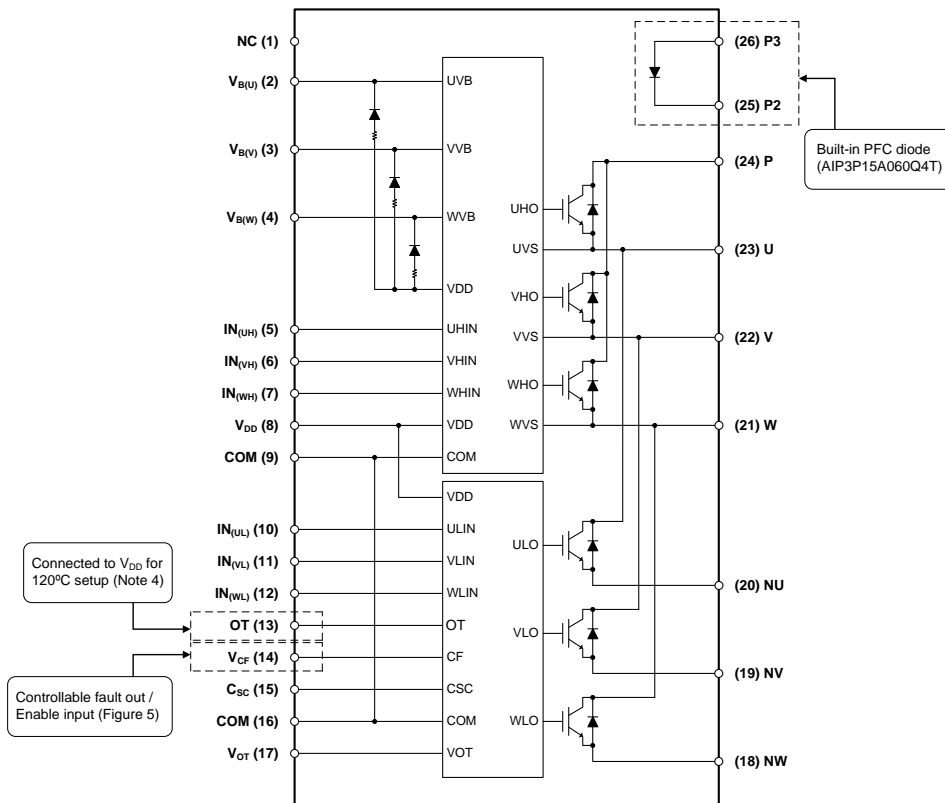
### Features

- 3-phase inverter module with optional built-in PFC diode
- 600V-15A (Trench Shielded Planar Gate IGBT)
- Low  $V_F$  and Ultra-fast recovery diode for PFC (AIP3P15A060Q4T)
- Built-in bootstrap diodes with integrated current-limiting resistor
- Control supply under-voltage lockout protection (UVLO)
- Controllable over-temperature protection (OT)
- Temperature monitoring ( $V_{OT}$ )
- Short-circuit current protection ( $C_{SC}$ )
- Controllable fault out signal ( $V_{CF}$ ) corresponding to SC, UV and OT fault
- Enable input functionality: Low-side IGBTs shut-down
- Input interface: 3 and 5V line, Schmitt trigger receiver circuit (Active high)
- Isolation ratings of 2000Vrms/min

### Applications

- AC 100-240Vrms class low power motor drives
- Air-conditioners, Washing machines, Compressors and Fan Motors

### Internal Equivalent Circuit / Pin Configuration



## Ordering Information

Part Number	Temperature Range	Package	Terminal type
AIP3D15A060Q4T	-40°C to 150°C	IPM-3E	Long with stopper
AIP3P15A060Q4T	-40°C to 150°C	IPM-3F	Long with stopper



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant. Please visit [www.aosmd.com/media/AOSGreenPolicy.pdf](http://www.aosmd.com/media/AOSGreenPolicy.pdf) for additional information.

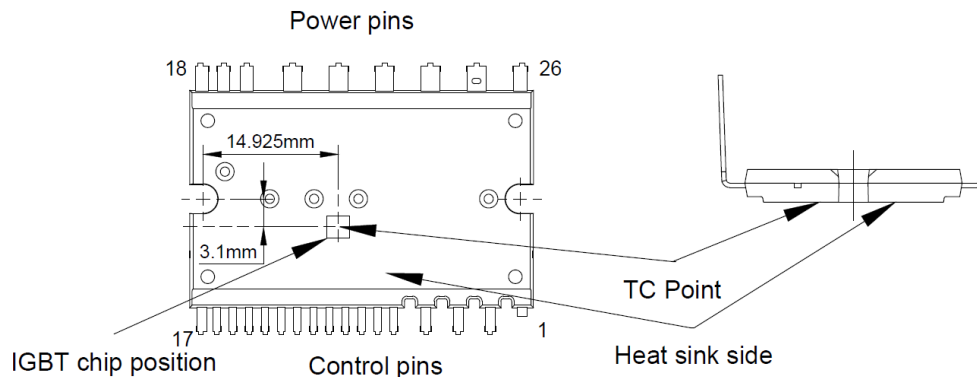
## Pin Description

Pin Number	Pin Name	Pin Function
1	NC	No Connection
2	V <sub>B(U)</sub>	High-Side Bias Voltage for U-Phase IGBT Driving
3	V <sub>B(V)</sub>	High-Side Bias Voltage for V-Phase IGBT Driving
4	V <sub>B(W)</sub>	High-Side Bias Voltage for W-Phase IGBT Driving
5	IN <sub>(UH)</sub>	Signal Input for High-Side U-Phase
6	IN <sub>(VH)</sub>	Signal Input for High-Side V-Phase
7	IN <sub>(WH)</sub>	Signal Input for High-Side W-Phase
8	V <sub>DD</sub>	Common Bias Voltage for IC and IGBTs Driving
9	COM	Common Supply Ground
10	IN <sub>(UL)</sub>	Signal Input for Low-Side U-Phase
11	IN <sub>(VL)</sub>	Signal Input for Low-Side V-Phase
12	IN <sub>(WL)</sub>	Signal Input for Low-Side W-Phase
13	OT	Controllable Over Temperature Protection (Connected to V <sub>DD</sub> for 120°C setup)
14	V <sub>CF</sub>	Controllable Fault Output
15	C <sub>SC</sub>	Capacitor (Low-Pass Filter) for Short-circuit Current Detection Input
16	COM	Common Supply Ground
17	V <sub>OT</sub>	Voltage Output of LVIC Temperature
18	NW	Negative DC-Link Input for W-Phase
19	NV	Negative DC-Link Input for V-Phase
20	NU	Negative DC-Link Input for U-Phase
21	W	Output for W-Phase
22	V	Output for V-Phase
23	U	Output for U-Phase
24	P	Positive DC-Link Input
25	P2	PFC Diode Cathode (AIP3P15A060Q4T)
26	P3	PFC Diode Anode (AIP3P15A060Q4T)

**Absolute Maximum Ratings**

T<sub>J</sub> = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Ratings	Units
<b>Inverter</b>				
V <sub>PN</sub>	Supply Voltage	Applied between P - NU,NV,NW	450	V
V <sub>PN(surge)</sub>	Supply Voltage (surge)	Applied between P - NU,NV,NW	500	V
V <sub>CES</sub>	Collector-Emitter Voltage		600	V
I <sub>C</sub>	Output Phase Current	T <sub>C</sub> =25°C, T <sub>J</sub> <150°C	15	A
		T <sub>C</sub> =80°C, T <sub>J</sub> <150°C	10	A
±I <sub>PK</sub>	Output Peak Phase Current	T <sub>C</sub> =25°C, less than 1ms pulse width	30	A
t <sub>SC</sub>	Short Circuit Withstand Time	V <sub>PN</sub> ≤400V, T <sub>J</sub> =150°C, V <sub>DD</sub> =15V	5	µs
P <sub>C</sub>	Collector Dissipation	T <sub>C</sub> =25°C, per chip	33	W
T <sub>J</sub>	Operating Junction Temperature		-40 to 150	°C
<b>PFC Diode</b>				
V <sub>RRM</sub>	Repetitive peak Reverse Voltage	Applied between P2 – P3	650	V
I <sub>F</sub>	Output Phase Current	T <sub>C</sub> =25°C, T <sub>J</sub> <150°C	30	A
		T <sub>C</sub> =100°C, T <sub>J</sub> <150°C	15	A
<b>Control (Protection)</b>				
V <sub>DD</sub>	Control Supply Voltage	Applied between V <sub>DD</sub> -COM	25	V
V <sub>DB</sub>	High-Side Control Bias Voltage	Applied between V <sub>B(U)</sub> -U, V <sub>B(V)</sub> -V, V <sub>B(W)</sub> -W	25	V
V <sub>IN</sub>	Input Voltage	Applied between I <sub>N(UH)</sub> , I <sub>N(VH)</sub> , I <sub>N(WH)</sub> , I <sub>N(UL)</sub> , I <sub>N(VL)</sub> , I <sub>N(WL)</sub> – COM	V <sub>DD</sub> +0.3	V
V <sub>CF</sub>	Fault Output Supply Voltage	Applied between V <sub>CF</sub> -COM	COM+5.5	V
I <sub>CF</sub>	Fault Output Current	Sink current at V <sub>CF</sub> terminal	1	mA
V <sub>SC</sub>	Current Sensing Input Voltage	Applied between C <sub>SC</sub> -COM	COM+5.5	V
V <sub>OT</sub>	Temperature Output	Applied between V <sub>OT</sub> -COM	COM+5.5	V
<b>Total System</b>				
V <sub>PN(PROT)</sub>	Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	V <sub>DD</sub> =13.5-16.5V, Inverter part T <sub>J</sub> =150°C, Non-repetitive, less than 2µs	400	V
T <sub>C</sub>	Module Case Operation Temperature	Measurement point of T <sub>C</sub> is provided in Figure 1	-30 to 125	°C
T <sub>STG</sub>	Storage Temperature		-40 to 150	°C
V <sub>ISO</sub>	Isolation Voltage	60Hz, sinusoidal, AC 1min, between connected all pins and heat sink plate	2000	V <sub>rms</sub>



**Figure 1. T<sub>C</sub> Measurement Point**

## Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance <sup>(1)</sup>	Inverter IGBT (per 1/6 module)	-	-	3.8	K/W
$R_{th(j-c)F}$		Inverter FWD (per 1/6 module)	-	-	4.97	K/W
$R_{th(j-c)D}$		PFC Diode (AIP3P15A060Q4T)	-	-	2.58	K/W

**Note:**

- For the measurement point of case temperature ( $T_c$ ), please refer to Figure 1.

## Electrical Characteristics

 $T_J = 25^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
<b>Inverter</b>							
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	$V_{DD}=V_{DB}=15V$ , $V_{IN}=5V$	$I_C=7.5A$ , $T_J=25^\circ\text{C}$	-	1.40	1.90	V
			$I_C=7.5A$ , $T_J=125^\circ\text{C}$	-	1.60	-	V
$V_F$	FWD Forward Voltage	$V_{IN}=0$	$I_F=7.5A$ , $T_J=25^\circ\text{C}$	-	1.55	2.00	V
$t_{ON}$	Switching Times	$V_{PN}=300V$ , $V_{DD}=V_{DB}=15V$ $I_C=10A$ , $T_J=25^\circ\text{C}$ , $V_{IN}=0V \leftrightarrow 5V$ Inductive load		0.40	0.70	1.20	$\mu\text{s}$
$t_{C(ON)}$				-	0.15	0.40	$\mu\text{s}$
$t_{OFF}$				-	1.25	1.75	$\mu\text{s}$
$t_{C(OFF)}$				-	0.10	0.30	$\mu\text{s}$
$t_{rr}$				-	0.10	-	$\mu\text{s}$
$I_{CES}$	Collector-Emitter Leakage Current	$V_{CE}=V_{CES}$	$T_J=25^\circ\text{C}$	-	-	1	mA
			$T_J=125^\circ\text{C}$	-	-	10	mA
<b>PFC Diode</b>							
$V_F$	FWD Forward Voltage		$I_F=20A$ , $T_J=25^\circ\text{C}$	-	1.45	-	V
$T_{rr}$	Reverse recovery time	$T_J=25^\circ\text{C}$ , $V_R=400V$ , $I_F=20A$ , $di_F/dt=300A/\mu\text{s}$			55		ns
$Q_{rr}$	Reverse recovery Charge				0.55		$\mu\text{C}$
$I_{rr}$	Peak reverse recovery current				16		A
<b>Control (Protection)</b>							
$I_{QDD}$	Quiescent $V_{DD}$ Supply Current	$V_{DD}=15V$ , $I_{N(UH,VH,WH,UL,VL,WL)}=0V$	$V_{DD-COM}$	-	-	2.1	mA
$I_{QDB}$	Quiescent $V_{DB}$ Supply Current	$V_{DB}=15V$ , $I_{N(UH, VH, WH)}=0V$	$V_{B(U)-U}$ , $V_{B(V)-V}$ , $V_{B(W)-W}$	-	-	0.3	mA
$V_{SC(ref)}$	Short-Circuit Trip Level	$V_{DD}=15V$ <sup>(2)</sup>		0.455	0.48	0.505	V
$UV_{DT}$	Supply Circuit Under-Voltage Protection	Trip Level		10.3	11.4	12.5	V
$UV_{DR}$		Reset Level		10.8	11.9	13.0	V
$UV_{DBT}$		Trip Level		8.5	9.5	10.5	V
$UV_{DBR}$		Reset Level		9.5	10.5	11.5	V
$V_{OT}$	Temperature Output <sup>(3)</sup>		LVIC Temperature= $90^\circ\text{C}$	2.67	2.77	2.86	V
			LVIC Temperature= $25^\circ\text{C}$	0.8	1.05	1.3	V
$OT_T$	Over-Temperature Protection <sup>(4)</sup>	The OT Pin is connected to $V_{DD}$ or open	Trip Level	100	120	140	$^\circ\text{C}$
$OT_{HYS}$			Hysteresis of Trip Reset	-	30	-	$^\circ\text{C}$

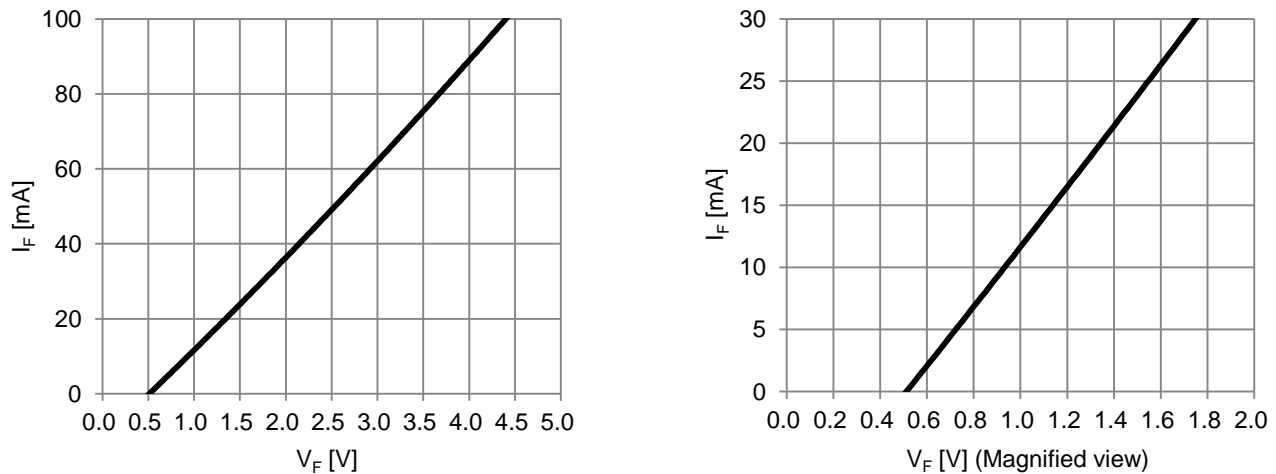
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Control (Protection)</b>						
$V_{CFH}$	Fault Output Voltage	$V_{SC}=0V$ , $V_{CF}$ Circuit: 10k $\Omega$ to 5V pull-up	4.9	-	-	V
$V_{CFL}$		$V_{SC}=1V$ , $V_{CF}$ Circuit: 10k $\Omega$ to 5V pull-up	-	-	0.5	V
$V_{CF+}$	CF positive going threshold		-	1.9	2.2	V
$V_{CF-}$	CF negative going threshold		0.8	1.1	-	V
$t_{FO}$	Fault Output Pulse Width <sup>(5)</sup>	Pull-up resistor only	20	-	-	$\mu$ s
		Pull-up resistor with pull-down capacitor ( $R_{CF}=2.2M\Omega$ , $C_{CF}=1nF$ , 5V pull-up) <sup>(Figure 5)</sup>	-	1	-	ms
$I_{IN}$	Input Current	$V_{IN}=5V$	-	0.72	-	mA
$V_{th(on)}$	ON Threshold Voltage	Applied between $IN_{(UH)}$ , $IN_{(VH)}$ , $IN_{(WH)}$ , $IN_{(UL)}$ , $IN_{(VL)}$ , $IN_{(WL)}$ -COM		2.3	2.6	V
$V_{th(off)}$	OFF Threshold Voltage		0.8	1.2		V
$V_{th(hys)}$	ON/OFF Threshold Hysteresis Voltage		-	1.1	-	V
$V_{F(BSD)}$	Bootstrap Diode Forward Voltage	$I_F=10mA$ Including Voltage Drop by Limiting Resistor <sup>(6)</sup>	0.5	1.0	1.5	V
$R_{BSD}$	Built-in Limiting Resistance	Included in Bootstrap Diode	80	100	120	$\Omega$

**Notes:**

- Short-circuit protection works only for low sides.
- When temperature exceeds the protective level that the user defined, the controller (MCU) should stop the IPM. Temperature of LVIC vs.  $V_{OT}$  output characteristics is described in Figure 3.
- When the LVIC temperature exceeds OT Trip temperature level ( $OT_T$ ), OT protection is triggered and fault outputs. OT Trip level can be adjusted by pull-down resistors values as shown in the table below.

OT Pin	$OT_T$ [°C]
10k $\Omega$	Disable
100k $\Omega$	130
400k $\Omega$	110
$V_{DD}$ or Open	120

- Fault signal ( $F_o$ ) outputs when SC, UV or OT protection is triggered.  $F_o$  pulse width is different for each protection mode. At SC failure,  $F_o$  pulse width is fixed (minimum 20 $\mu$ s) or controlled by RC network (see Figure 5), but at UV or OT failure,  $F_o$  outputs continuously until recovering from UV or OT state.
- The characteristics of bootstrap diodes are shown in Figure 2.



**Figure 2. Built-in Bootstrap Diode  $V_F$ - $I_F$  Characteristic ( $T_C=25^\circ C$ )**

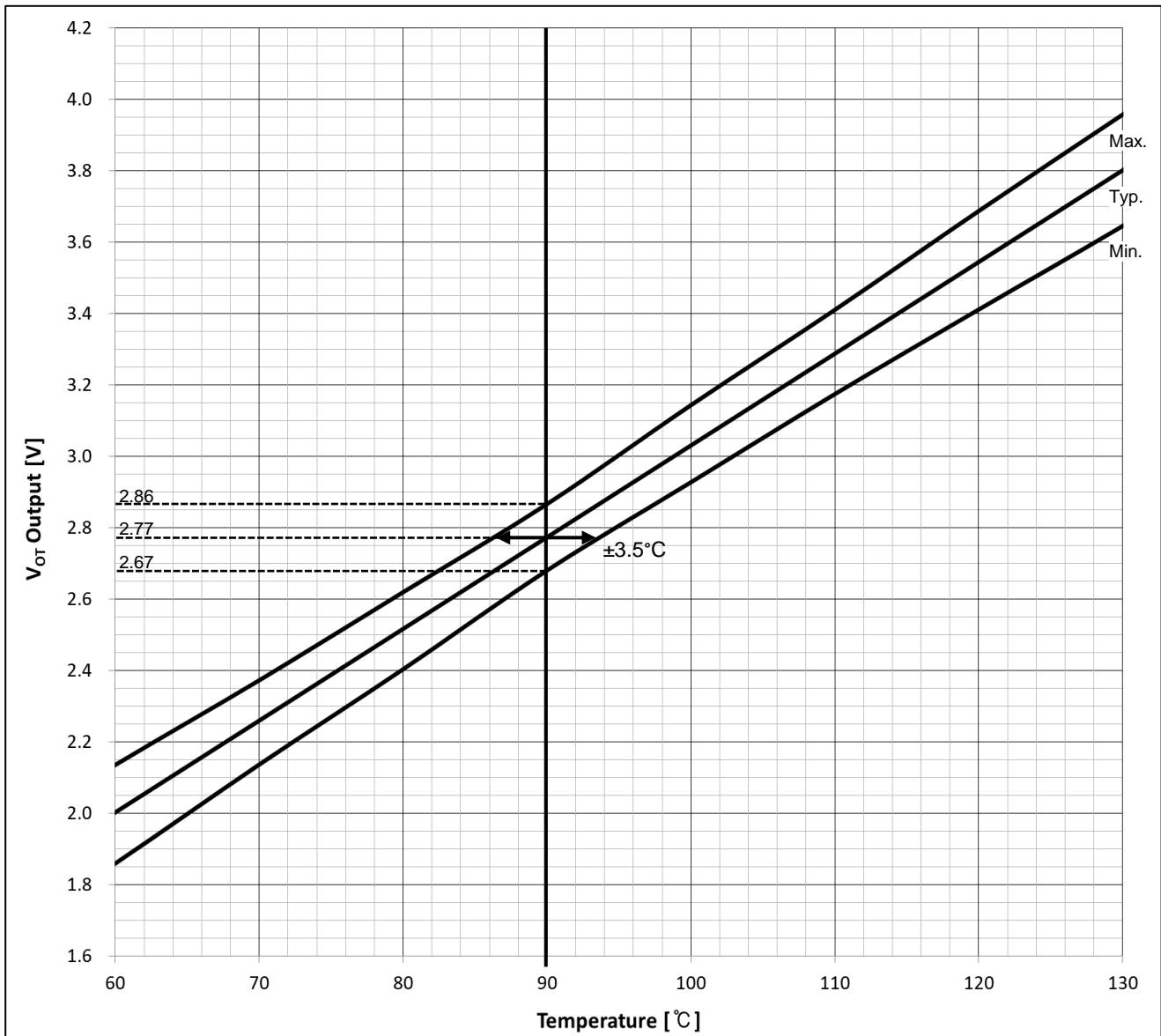
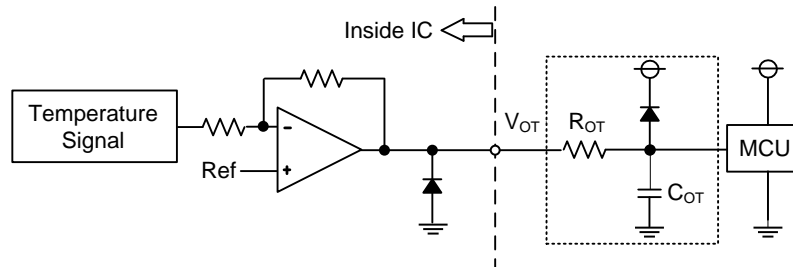
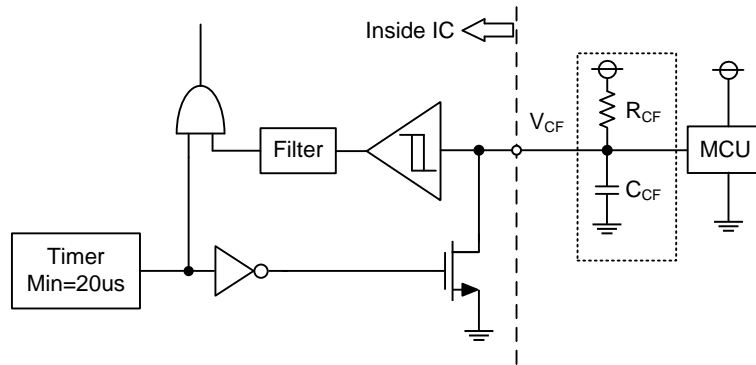


Figure 3. Temperature of LVIC vs. V<sub>OT</sub> Output Characteristics



- (1) In the case of using V<sub>OT</sub> with low voltage controller like 3.3V MCU, V<sub>OT</sub> output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp diode between control supply of the controller and V<sub>OT</sub> output for preventing over voltage destruction.
- (2) When V<sub>OT</sub> is connected to MCU, to use RC (R<sub>OT</sub>=2kΩ, C<sub>OT</sub>=10nF) filter is recommended.
- (3) In the case of not using V<sub>OT</sub>, leave V<sub>OT</sub> output NC (No connection).

Figure 4. Interface Circuit at Pin V<sub>OT</sub>



- (1) The  $V_{CF}$  pin combines three functions in one pin: Fixed fault out, Controllable fault out pulse width based on RC network, and Enable input.
- (2) The  $V_{CF}$  pin provides an enable functionality that allows it to shut down the all low-side IGBTs. When the  $V_{CF}$  pin is in the high state the IPM is able to operate normally. If the  $V_{CF}$  pin is in a low state, the low-side IGBTs are turned off until the enable condition is restored. In addition, the  $V_{CF}$  pin can provide the fault output signal with the fixed or controlled fault out pulse width.
- (3) If a pull-up resistor (10k $\Omega$ ) only is connected to the  $V_{CF}$  pin, the fault output pulse width is fixed at minimum 20us.
- (4) If a capacitor ( $C_{CF}$ ) is connected with a pull-up resistor ( $R_{CF}$ ) together, the fault output pulse width can be controlled according to the resistor and the capacitor values. The length of fault output pulse width is determined by the following formula ;
  - $t_{FO} = -(R_{CF} * C_{CF}) * \ln(1 - V_{CF} / V_{DD}) + 100ns + 20us(\text{min.})$
  - ex)  $V_{DD}=5V$ ,  $R_{CF}=2.2M\Omega$ ,  $C_{CF}=1nF$ ,  $t_{FO}\approx 1.07ms$ . Recommended parameters in the design are  $C_{CF}$  of  $\leq 1nF$  and  $R_{CF}$  of 0.1M to 2.2M $\Omega$ .

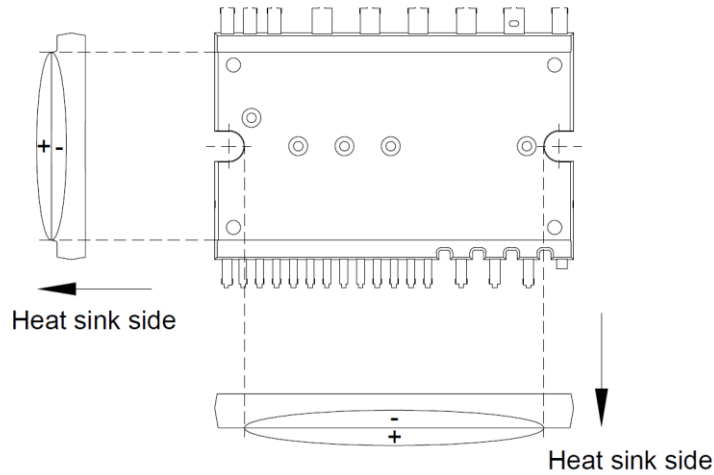
**Figure 5. Interface Circuit at Pin  $V_{CF}$**

**Mechanical Characteristics and Ratings**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Mounting Torque	Mounting Screw: M3 <sup>(7)</sup>		0.59	0.69	0.78	N m
Weight			-	9.12	-	g
Flatness	Refer to Figure 6		-50	-	100	μm

**Note:**

7. Plain washers (ISO 7089-7094) are recommended.



**Figure 6. Flatness Measurement Position**

**Recommended Operation Conditions**

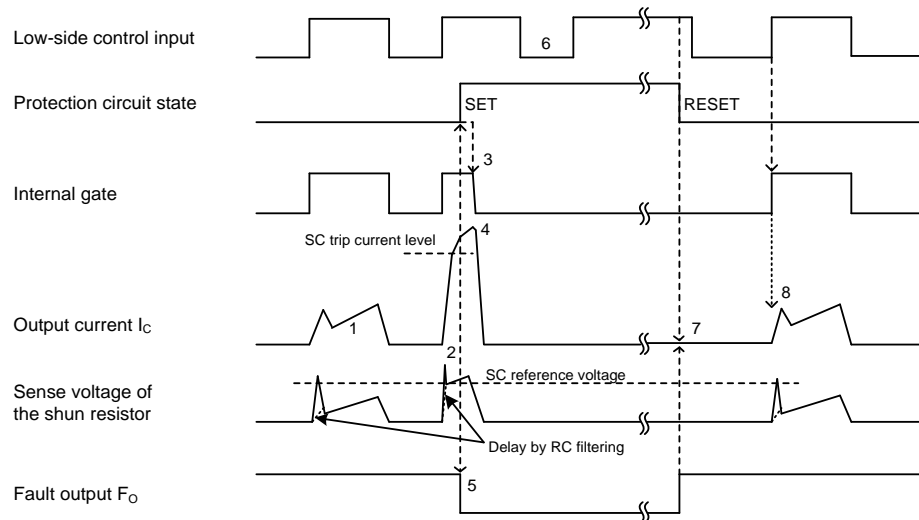
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>PN</sub>	Supply Voltage	Applied between P-NU, NV, NW	0	300	400	V
V <sub>DD</sub>	Control Supply Voltage	Applied between V <sub>DD</sub> -COM	13.5	15.0	16.5	V
V <sub>DB</sub>	High-Side Bias Voltage	Applied between V <sub>B(U)</sub> -U, V <sub>B(V)</sub> -V, V <sub>B(W)</sub> -W	13.5	15.0	18.5	V
dV <sub>DD</sub> /dt, dV <sub>DB</sub> /dt	Control Supply Variation		-1	-	+1	V/μs
t <sub>dead</sub>	Arm Shoot-Through Blocking Time	For each input signal	1.0	-	-	μs
f <sub>PWM</sub>	PWM Input Frequency	-40°C < T <sub>J</sub> < 150°C	-	-	20	kHz
PW <sub>IN(ON)</sub>	Minimum Input Pulse Width <sup>(8)</sup>		0.5	-	-	μs
PW <sub>IN(OFF)</sub>			0.5	-	-	μs
COM	COM Variation	Between COM-NU, NV, NW (including surge)	-5.0	-	5.0	V

**Note:**

8. IPM may not respond if the input pulse width is less than PW<sub>IN(ON)</sub>, PW<sub>IN(OFF)</sub>.

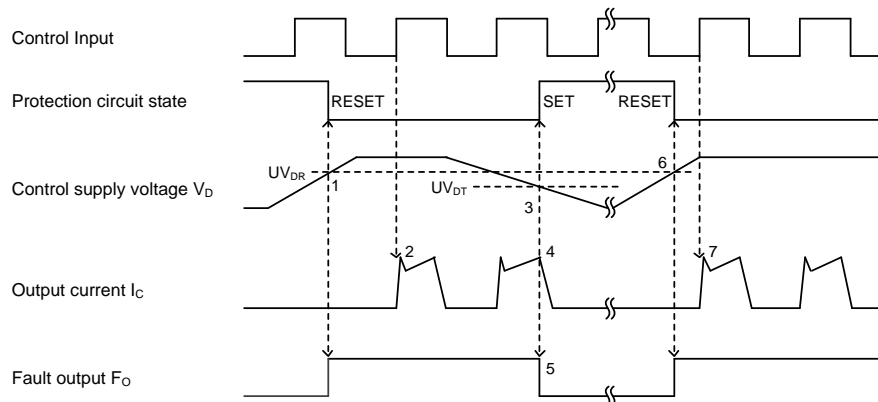


## Time Charts of the IPM Protective Function



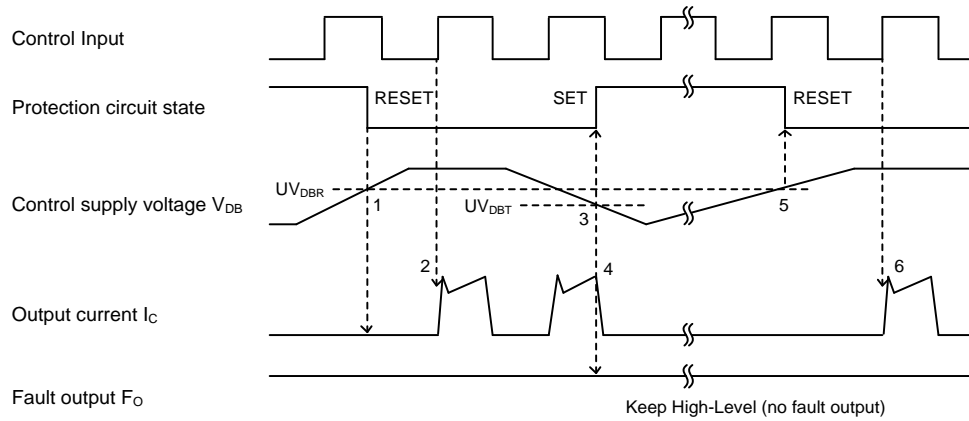
- (1) Normal operation: IGBT turns on and outputs current.
- (2) Short-circuit current detection (SC triggered).
- (3) All low-side IGBTs' gates are hard interrupted.
- (4) All low-side IGBTs turn OFF.
- (5)  $F_o$  output time ( $t_{FO}$ )=minimum 20 $\mu$ s.
- (6) Input = "L" : IGBT OFF.
- (7) Fault output finishes, but output current will not turn on until next ON signal (L $\rightarrow$ H).
- (8) Normal operation: IGBT turns on and outputs current.

**Figure 7. Short-Circuit Protection  
(Low-side Operation Only with the External Shunt Resistor and RC Filter)**



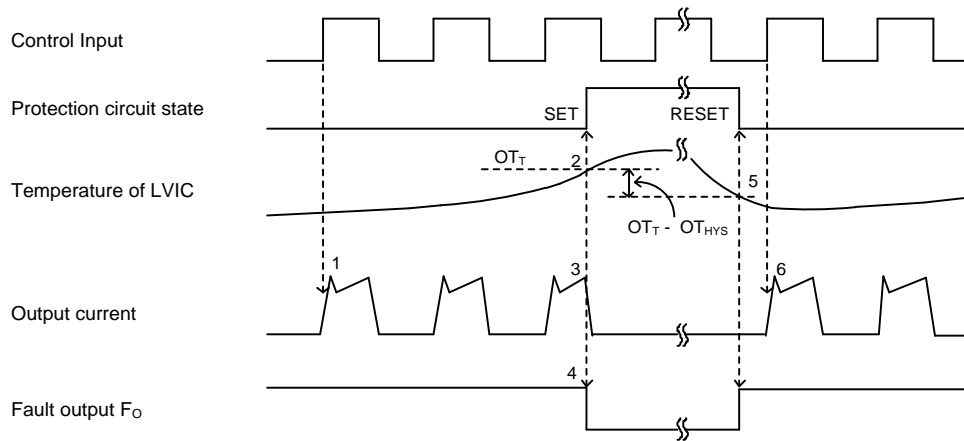
- (1) Control supply voltage  $V_{DD}$  exceeds under voltage reset level ( $UV_{DR}$ ), but IGBT turns on by next ON signal (L $\rightarrow$ H).
- (2) Normal operation: IGBT turns on and outputs current.
- (3)  $V_{DD}$  level drops to under voltage trip level ( $UV_{DT}$ ).
- (4) All low-side IGBTs turn OFF regardless of control input condition.
- (5)  $F_o$  output time ( $t_{FO}$ )=minimum 20 $\mu$ s, and  $F_o$  stays low as long as  $V_{DD}$  is below  $UV_{DR}$ .
- (6)  $V_{DD}$  level reaches  $UV_{DR}$ .
- (7) Normal operation: IGBT turns on and outputs current.

**Figure 8. Under-Voltage Protection (Low-side,  $UV_D$ )**



- (1) Control supply voltage  $V_{DB}$  rises. After the voltage reaches under voltage reset level  $UV_{DBR}$ , IGBT turns on by next ON signal (L→H).
- (2) Normal operation: IGBT turns on and outputs current.
- (3)  $V_{DB}$  level drops to under voltage trip level ( $UV_{DBT}$ ).
- (4) All high-side IGBTs turn OFF regardless of control input condition, but there is no  $F_O$  signal output.
- (5)  $V_{DB}$  level reaches  $UV_{DBR}$ .
- (6) Normal operation: IGBT turns on and outputs current.

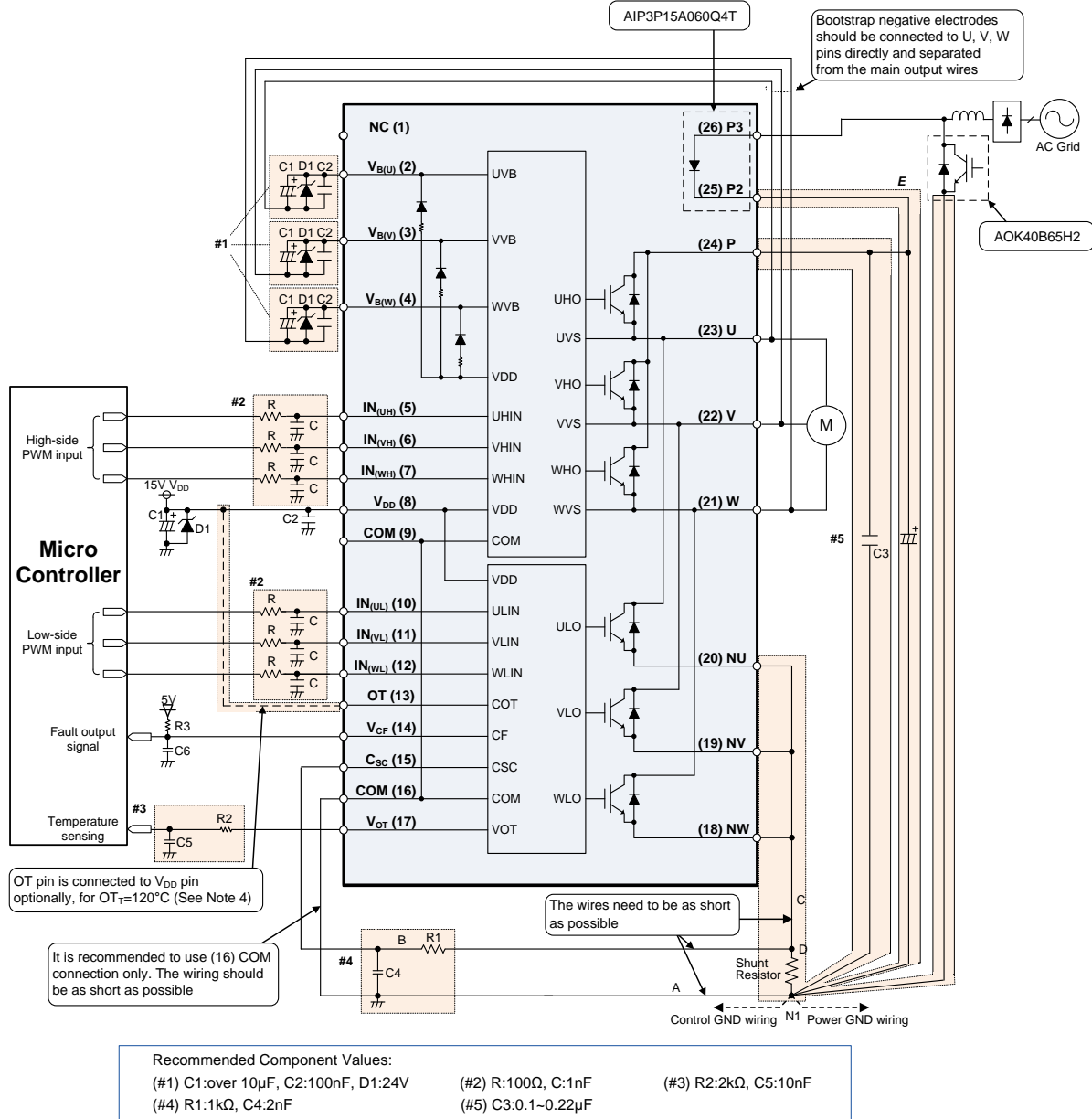
Figure 9. Under-Voltage Protection (High-side,  $UV_{DB}$ )



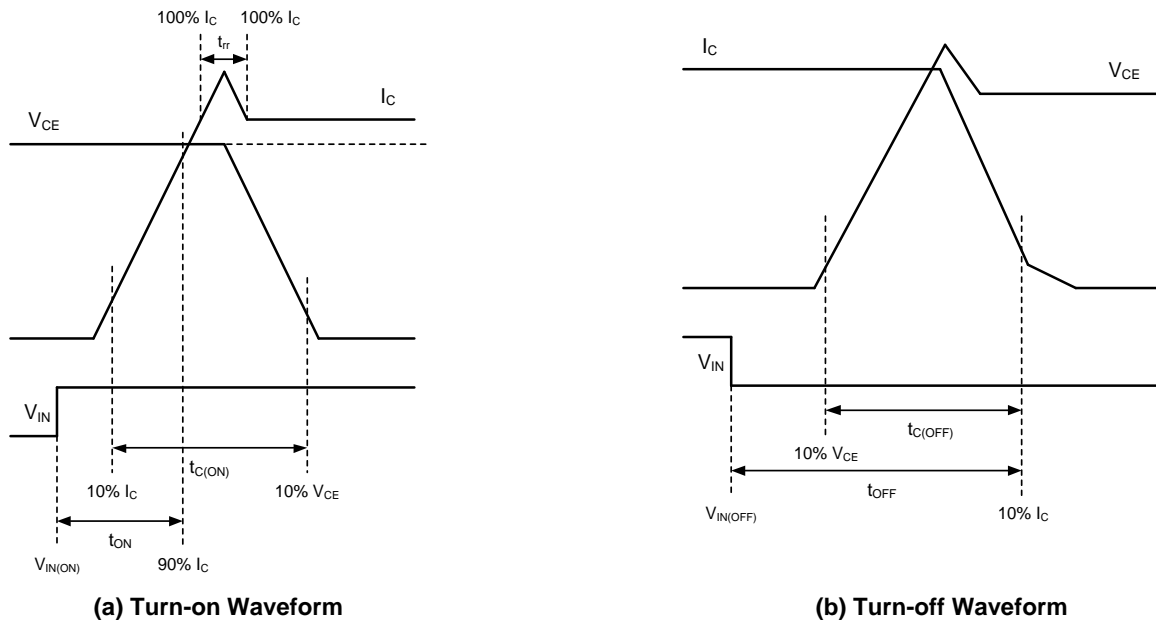
- (1) Normal operation: IGBT turns on and outputs current.
- (2) LVIC temperature exceeds over-temperature trip level ( $OT_T$ ).
- (3) All low-side IGBTs turn off regardless of control input condition.
- (4)  $F_O$  output time ( $t_{FO}$ )=minimum  $20\mu s$ , and  $F_O$  stays low as long as LVIC temperature is over  $OT_T$ .
- (5) LVIC temperature drops to over-temperature reset level ( $OT_T - OT_{HYS}$ ).
- (6) Normal operation: IGBT turns on by the next ON signal (L→H).

Figure 10. Over-Temperature Protection (Low-side, Detecting LVIC Temperature)

Example of Application Circuit

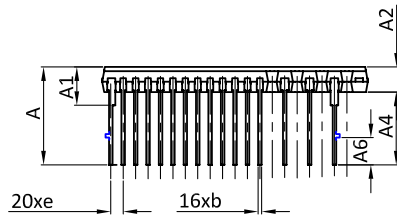


- (1) GND pattern: The star ground design is recommended. GND pattern should be separated at the one point of the shunt resistors.
- (2) COM pin: It is recommended to only use the (16) COM pin to minimize SC detection noise. Leave pin (9) NC (No Connection).
- (3) A Zener diode D1 (24V/1W) is recommended between each pair of control supply pins to prevent surge destruction.
- (4) Snubber capacitor: The wiring between the IPM and snubber capacitor (C3) including the shunt resistors should be as short as possible.
- (5) C<sub>SC</sub> pin circuit: C4 should be placed as close to C<sub>SC</sub> pin and COM (16) pin as possible to prevent protection function errors.
- (6) P2 pin connection: The pin P2 (PFC diode cathode) should be connected directly to the positive terminal of DC-link capacitor as shown in the trace E.
- (7) Bootstrap capacitors: It is recommended that all capacitors are mounted as close to the IPM as possible.
- (8) Input circuit: The R and C filter circuit should be mounted to reduce input signal noise by high speed switching. C should be placed as close to COM (16) pin as possible.
- (9) V<sub>CF</sub> pin circuit: V<sub>CF</sub> output is open drain type. The signal line should be pulled up to the positive side of the 5V/3.3V logic power supply with a proper resistor R3. For the detailed design guide, please refer to the Figure 5.

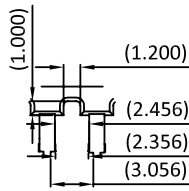


**Figure 11. Switching Times Definition**

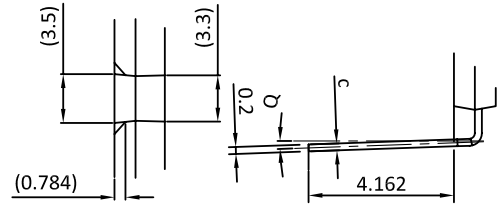
**Package Dimensions, IPM3-3E**



**SIDE VIEW**

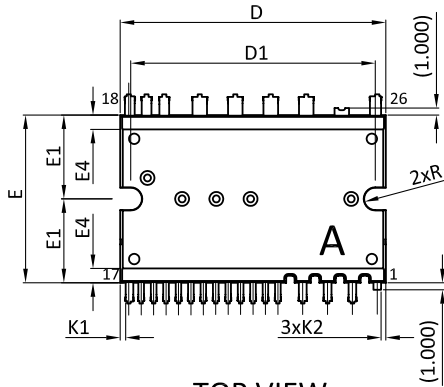


**Detail A**

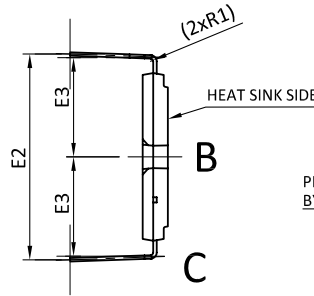


**Detail B**

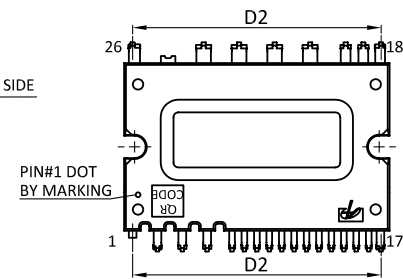
**Detail C**



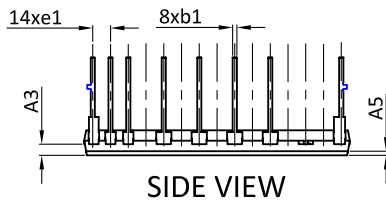
**TOP VIEW**



**SIDE VIEW**

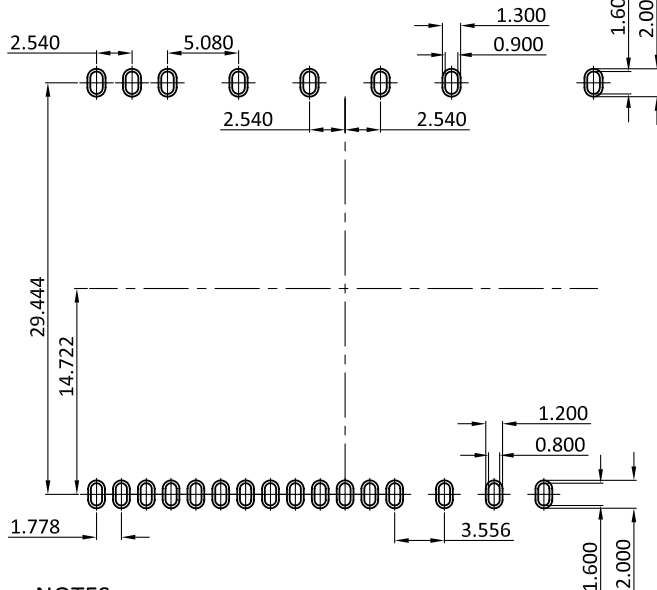


**BOTTOM VIEW**



**SIDE VIEW**

**LAND PATTERN RECOMMENDATIONS**



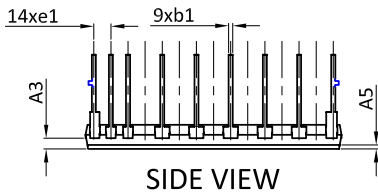
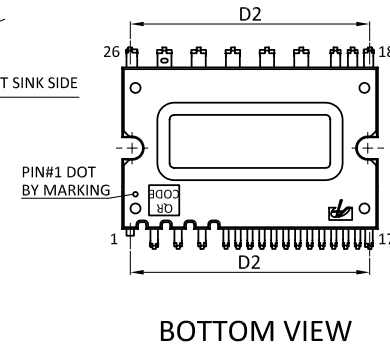
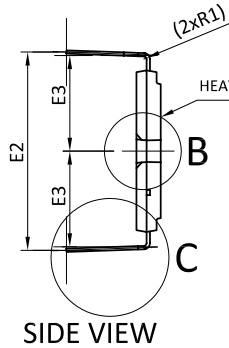
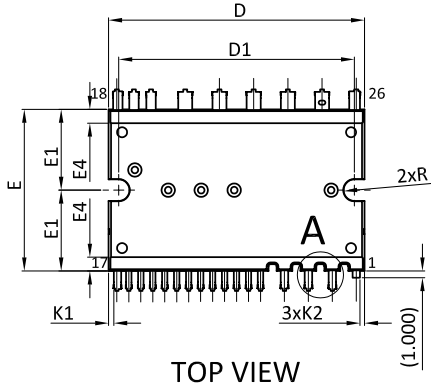
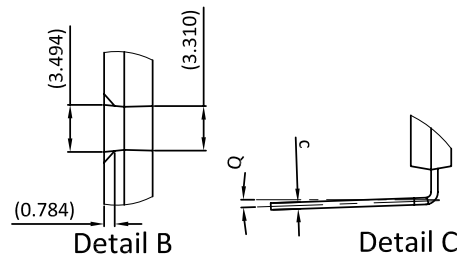
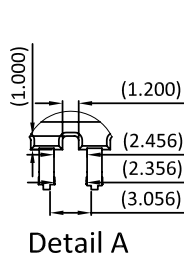
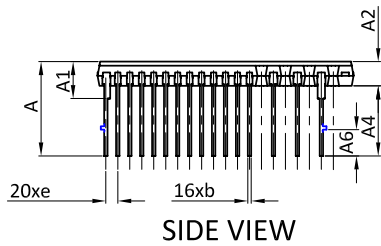
SYMBOLS	DIMENSION IN MILLIMETRES			DIMENSION IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	13.600	14.000	14.400	0.535	0.551	0.567
A1	5.200	5.500	5.800	0.205	0.217	0.228
A2	3.400	3.600	3.800	0.134	0.142	0.150
A3	1.550	1.600	1.650	0.061	0.063	0.065
A4	10.000	10.400	10.800	0.394	0.409	0.425
A5	0.400	0.600	0.800	0.016	0.024	0.031
A6	3.700	3.900	4.100	0.146	0.154	0.161
b	0.400	0.500	0.600	0.016	0.020	0.024
b1	0.500	0.600	0.700	0.020	0.024	0.028
c	0.400	0.500	0.600	0.016	0.020	0.024
D	37.700	38.000	38.300	1.484	1.496	1.508
D1	34.800	35.000	35.200	1.370	1.378	1.386
D2	35.260	35.560	35.860	1.388	1.400	1.412
E	23.700	24.000	24.300	0.933	0.945	0.957
E1	11.600	12.000	12.400	0.457	0.472	0.488
E2	29.000	29.400	29.800	1.142	1.157	1.173
E3	13.800	14.200	14.600	0.543	0.559	0.575
E4	1.750	2.050	2.350	0.069	0.081	0.093
e	1.578	1.778	1.978	0.062	0.070	0.078
e1	2.340	2.540	2.740	0.092	0.100	0.108
K1	0.620	0.820	1.020	0.024	0.032	0.040
K2	0.370	0.570	0.770	0.015	0.022	0.030
R	1.500	1.600	1.700	0.059	0.063	0.067
R1	0.400REF			0.016REF		
Q	2° - 6°			2° - 6°		

UNIT: mm

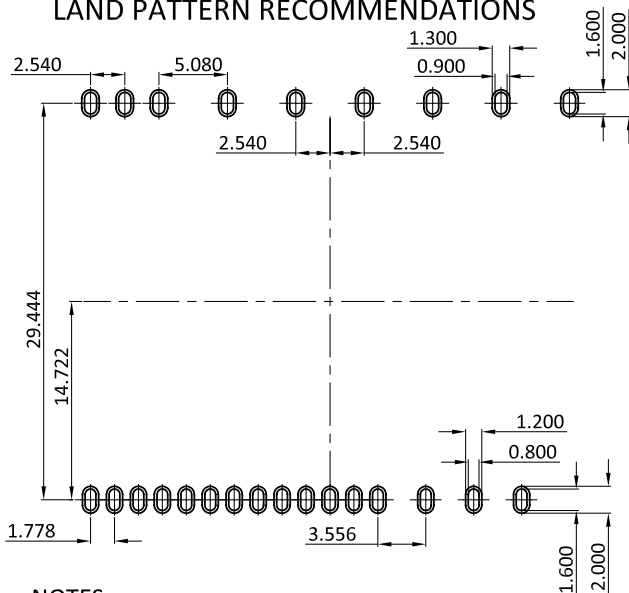
**NOTES**

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS, MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
4. ( ) IS REFERENCE.

**Package Dimensions, IPM3-3F**



**LAND PATTERN RECOMMENDATIONS**



SYMBOLS	DIMENSION IN MILLIMETRES			DIMENSION IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	13.600	14.000	14.400	0.535	0.551	0.567
A1	5.200	5.500	5.800	0.205	0.217	0.228
A2	3.400	3.600	3.800	0.134	0.142	0.150
A3	1.550	1.600	1.650	0.061	0.063	0.065
A4	10.000	10.400	10.800	0.394	0.409	0.425
A5	0.400	0.600	0.800	0.016	0.024	0.031
A6	3.700	3.900	4.100	0.146	0.154	0.161
b	0.400	0.500	0.600	0.016	0.020	0.024
b1	0.500	0.600	0.700	0.020	0.024	0.028
c	0.400	0.500	0.600	0.016	0.020	0.024
D	37.700	38.000	38.300	1.484	1.496	1.508
D1	34.800	35.000	35.200	1.370	1.378	1.386
D2	35.260	35.560	35.860	1.388	1.400	1.412
E	23.700	24.000	24.300	0.933	0.945	0.957
E1	11.600	12.000	12.400	0.457	0.472	0.488
E2	29.000	29.400	29.800	1.142	1.157	1.173
E3	13.800	14.200	14.600	0.543	0.559	0.575
E4	1.750	2.050	2.350	0.069	0.081	0.093
e	1.578	1.778	1.978	0.062	0.070	0.078
e1	2.340	2.540	2.740	0.092	0.100	0.108
K1	0.620	0.820	1.020	0.024	0.032	0.040
K2	0.370	0.570	0.770	0.015	0.022	0.030
R	1.500	1.600	1.700	0.059	0.063	0.067
R1	0.400REF			0.016REF		
Q	2° - 6°			2° - 6°		

UNIT: mm

**NOTES**

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS, MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
4. ( ) IS REFERENCE.

## LEGAL DISCLAIMER

Applications or uses as critical components in life support devices or systems are not authorized. AOS does not assume any liability arising out of such applications or uses of its products. AOS reserves the right to make changes to product specifications without notice. It is the responsibility of the customer to evaluate suitability of the product for their intended application. Customer shall comply with applicable legal requirements, including all applicable export control rules, regulations and limitations.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:

[http://www.aosmd.com/terms\\_and\\_conditions\\_of\\_sale](http://www.aosmd.com/terms_and_conditions_of_sale)

## LIFE SUPPORT POLICY

ALPHA & OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

单击下面可查看定价，库存，交付和生命周期等信息

[>>AOS\(万代\)](#)