



ALPHA & OMEGA
SEMICONDUCTOR

AO4630

30V Complementary MOSFET

General Description

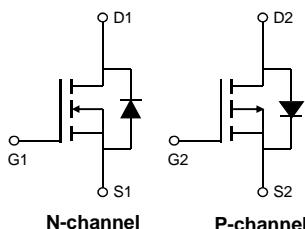
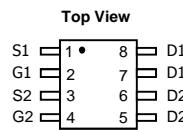
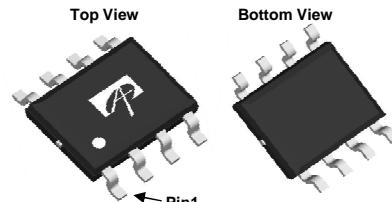
AO4630 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This complementary N and P channel MOSFET configuration is ideal for low Input Voltage inverter applications.

Product Summary

N-Channel	P-Channel
$V_{DS} = 30V$	-30V
$I_D = 7A$ ($V_{GS} = 10V$)	-5A ($V_{GS} = -10V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 23mΩ ($V_{GS} = 10V$)	< 48mΩ ($V_{GS} = -10V$)
< 28mΩ ($V_{GS} = 4.5V$)	< 57mΩ ($V_{GS} = -4.5V$)
< 36mΩ ($V_{GS} = 2.5V$)	< 78mΩ ($V_{GS} = -2.5V$)
100% UIS Tested	100% UIS Tested
100% R_g Tested	100% R_g Tested



SOIC-8



Orderable Part Number

Orderable Part Number	Package Type	Form	Minimum Order Quantity
AO4630	SO-8	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max N-channel	Max P-channel	Units	
Drain-Source Voltage	V_{DS}	30	-30	V	
Gate-Source Voltage	V_{GS}	± 12	± 12	V	
Continuous Drain Current	I_D	7	-5	A	
$T_A=70^\circ\text{C}$		5.6	-4		
Pulsed Drain Current ^C	I_{DM}	30	-25		
Avalanche Current ^C	I_{AS}	14	18	A	
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}	10	16	mJ	
V_{DS} Spike	$10\mu\text{s}$	V_{SPIKE}	36	-36	V
Power Dissipation ^B	P_D	2	1.3	W	
$T_A=70^\circ\text{C}$					
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C	

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10\text{s}$	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient ^{A,D} Steady-State		74	90	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	32	40 °C/W

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		1	5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 12\text{V}$			± 100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.65	1.05	1.45	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=7\text{A}$ $T_J=125^\circ\text{C}$		17.8	23	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=6\text{A}$		28	40	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_D=5\text{A}$		19	28	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=7\text{A}$		24	36	$\text{m}\Omega$
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$		670		pF
C_{oss}	Output Capacitance			75		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
R_g	Gate resistance	$f=1\text{MHz}$	1.5	3	4.5	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=7\text{A}$		13	20	nC
$Q_g(4.5\text{V})$	Total Gate Charge			6	12	nC
Q_{gs}	Gate Source Charge			1.3		nC
Q_{gd}	Gate Drain Charge			1.8		nC
$t_{D(\text{on})}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=2.2\Omega, R_{\text{GEN}}=3\Omega$		3		ns
t_r	Turn-On Rise Time			2.5		ns
$t_{D(\text{off})}$	Turn-Off DelayTime			25		ns
t_f	Turn-Off Fall Time			4		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=7\text{A}, di/dt=500\text{A}/\mu\text{s}$		6.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=7\text{A}, di/dt=500\text{A}/\mu\text{s}$		7.5		nC

A. The value of R_{QJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.

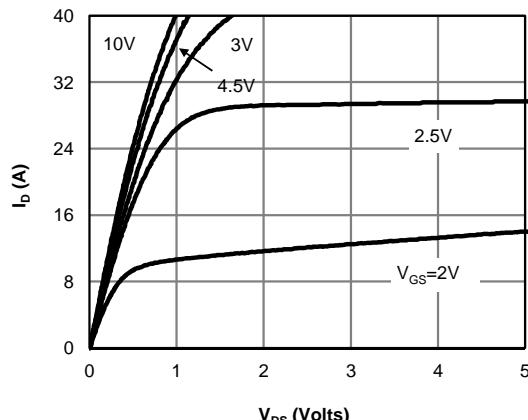
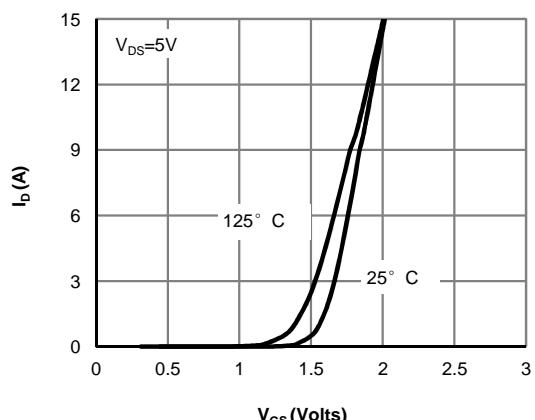
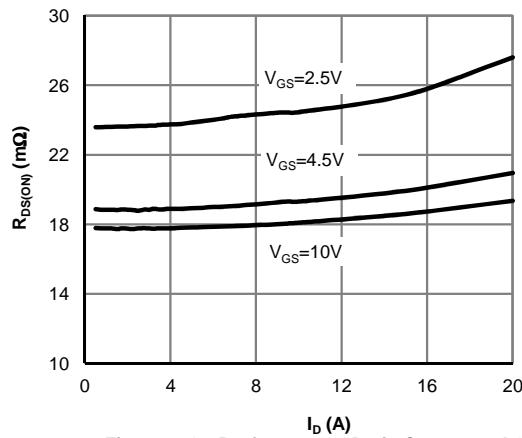
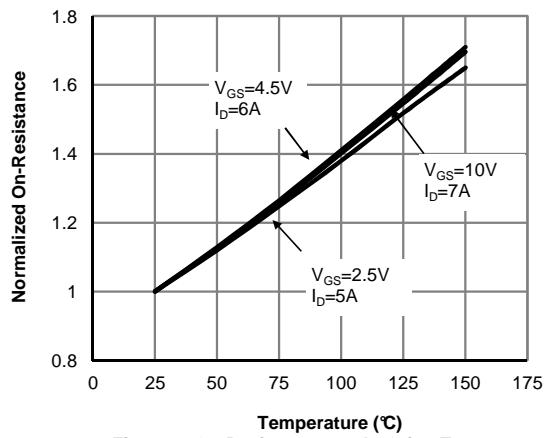
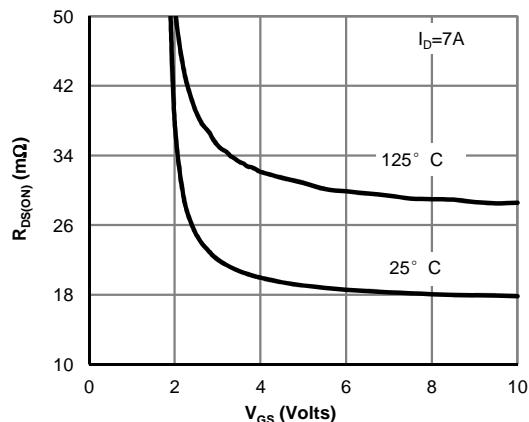
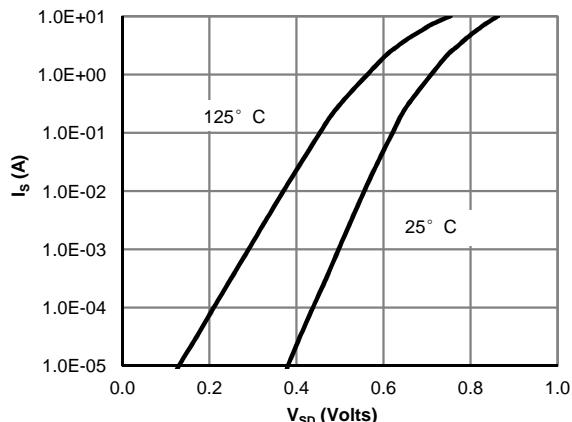
C. Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D. The R_{QJA} is the sum of the thermal impedance from junction to lead R_{QUL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(\text{MAX})}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

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N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

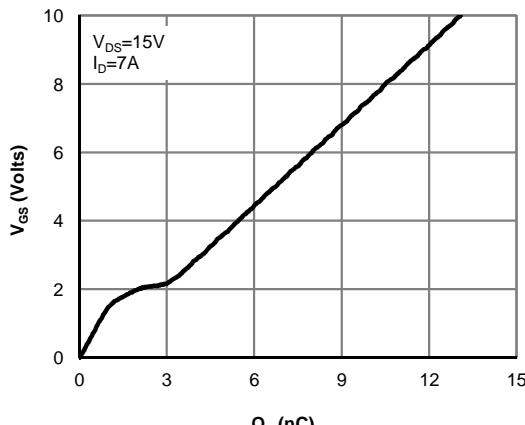
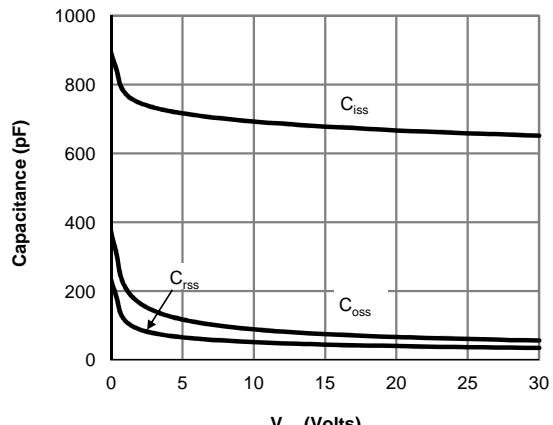
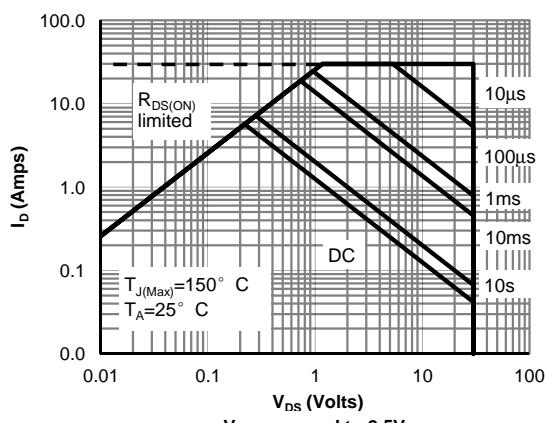
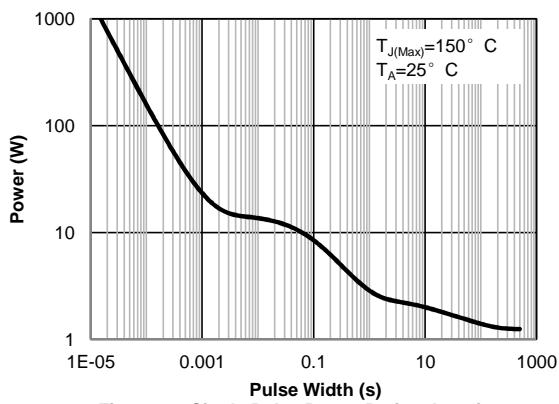
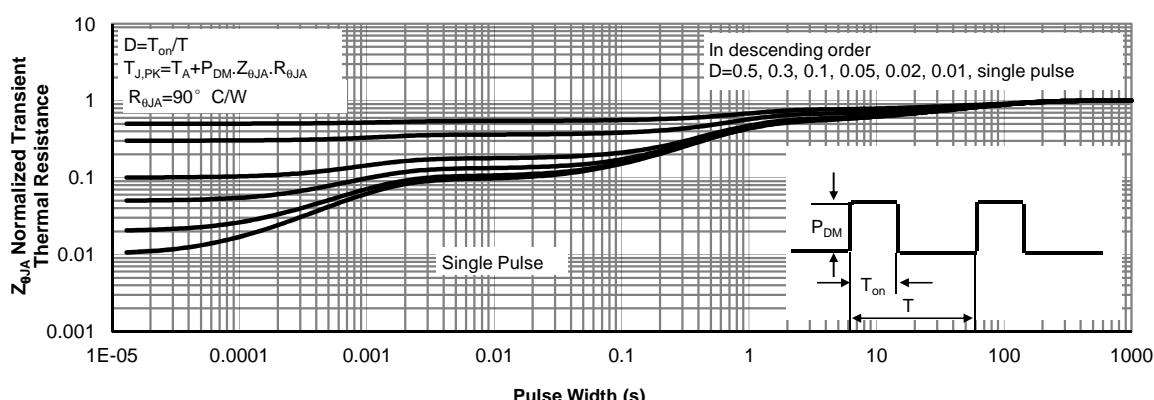
N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Figure A: Gate Charge Test Circuit & Waveforms

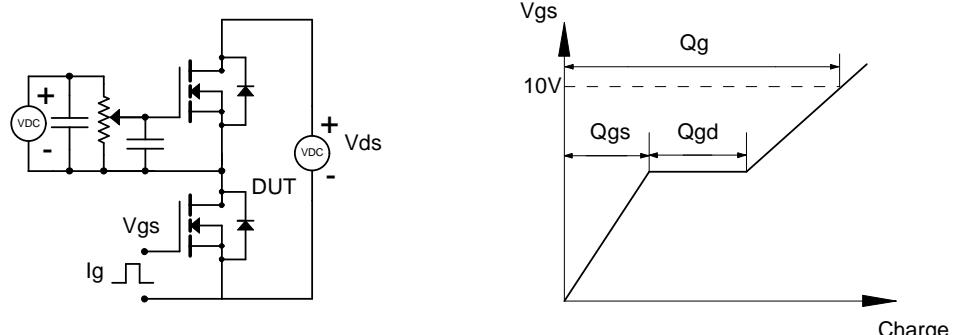


Figure B: Resistive Switching Test Circuit & Waveforms

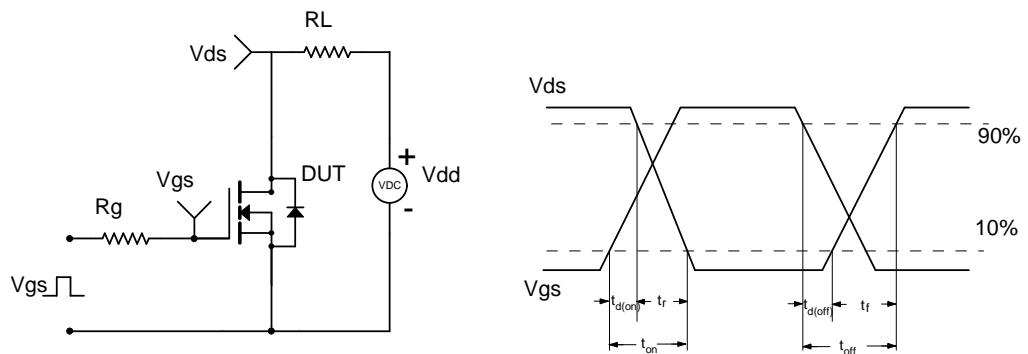


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

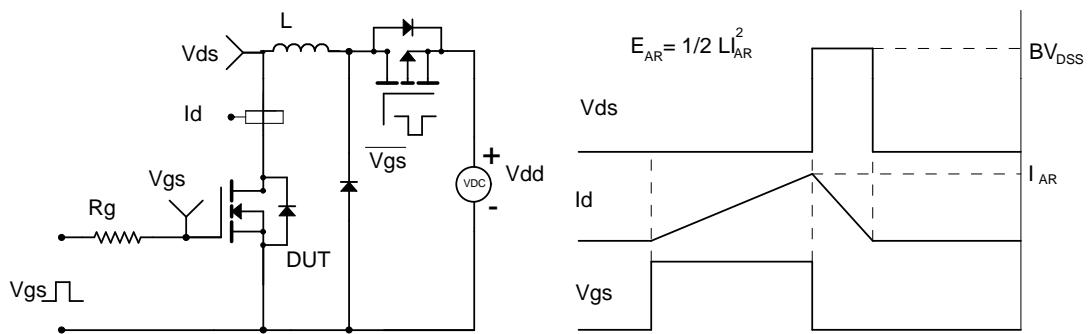
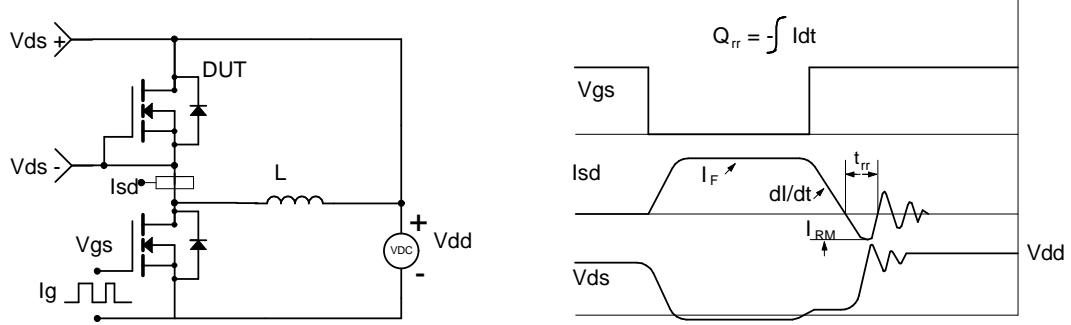


Figure D: Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$			-1	μA
				$T_J=55^\circ\text{C}$		-5
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			± 100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-0.5	-0.9	-1.3	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-5\text{A}$		40	48	$\text{m}\Omega$
				$T_J=125^\circ\text{C}$	48	60
		$V_{GS}=-4.5\text{V}$, $I_D=-3.5\text{A}$			45	57
		$V_{GS}=-2.5\text{V}$, $I_D=-2.5\text{A}$			60	78
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-5\text{A}$			18	S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$			-0.7	-1
I_S	Maximum Body-Diode Continuous Current				-2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-15\text{V}$, $f=1\text{MHz}$		700		pF
C_{oss}	Output Capacitance			80		pF
C_{rss}	Reverse Transfer Capacitance			60		pF
R_g	Gate resistance	$f=1\text{MHz}$	4	8	12	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $I_D=-5\text{A}$		14	25	nC
$Q_g(4.5\text{V})$	Total Gate Charge			7	15	nC
Q_{gs}	Gate Source Charge			1.5		nC
Q_{gd}	Gate Drain Charge			2.5		nC
$t_{D(\text{on})}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-15\text{V}$, $R_L=3\Omega$, $R_{\text{GEN}}=3\Omega$		6.5		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(\text{off})}$	Turn-Off DelayTime			41		ns
t_f	Turn-Off Fall Time			9		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-5\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		15		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-5\text{A}$, $dI/dt=500\text{A}/\mu\text{s}$		40		nC

A. The value of R_{QJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.

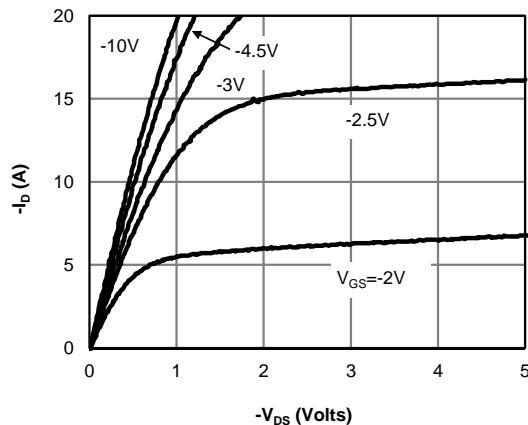
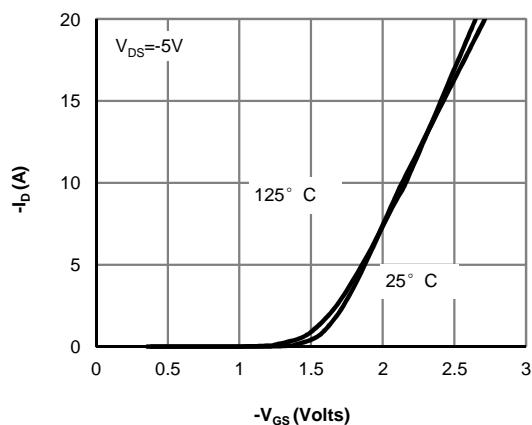
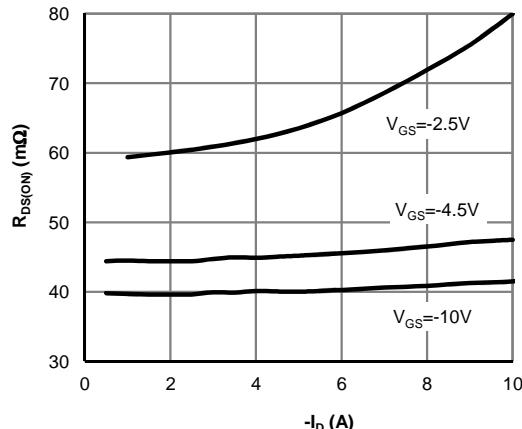
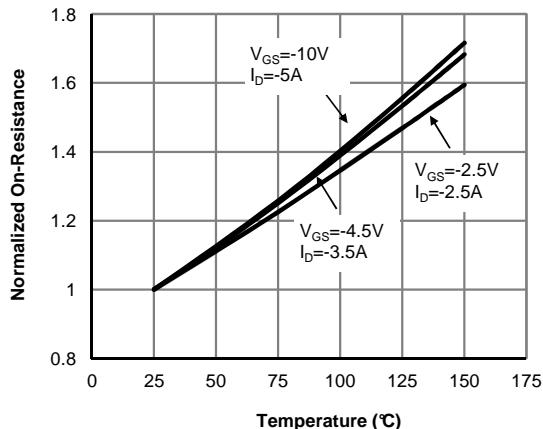
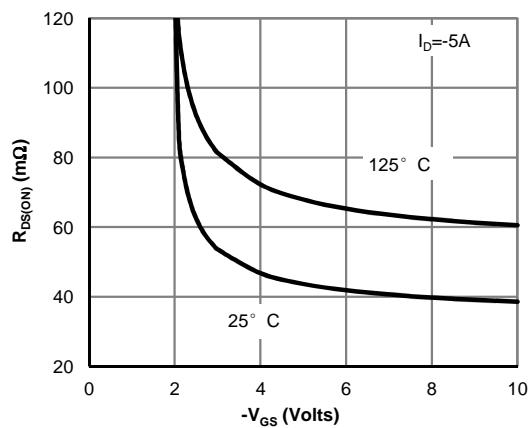
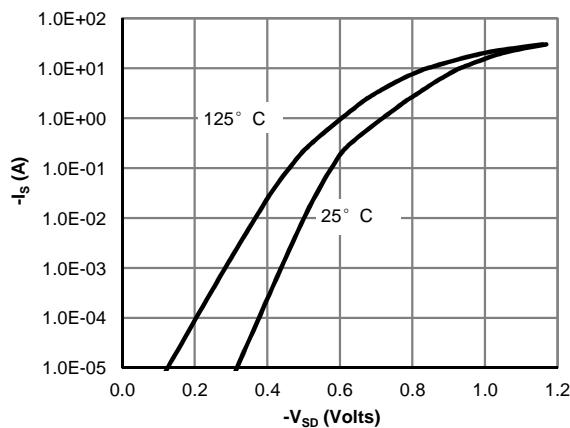
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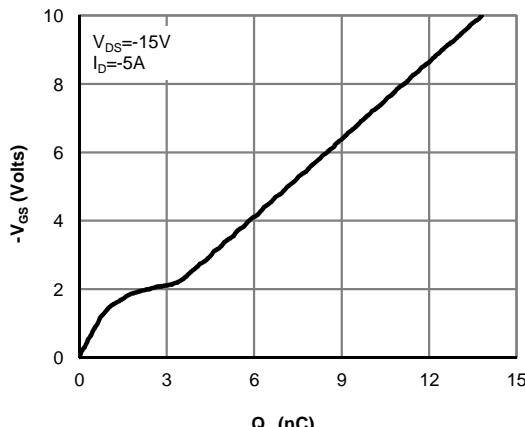
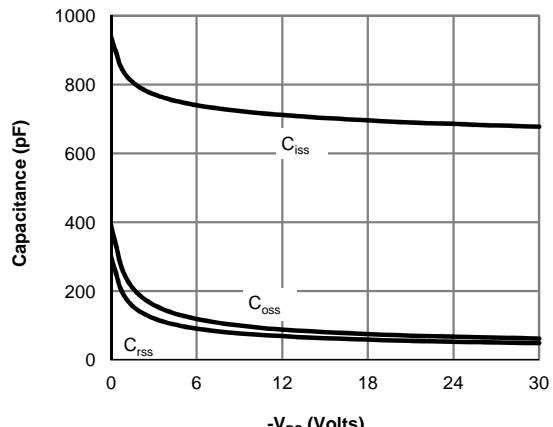
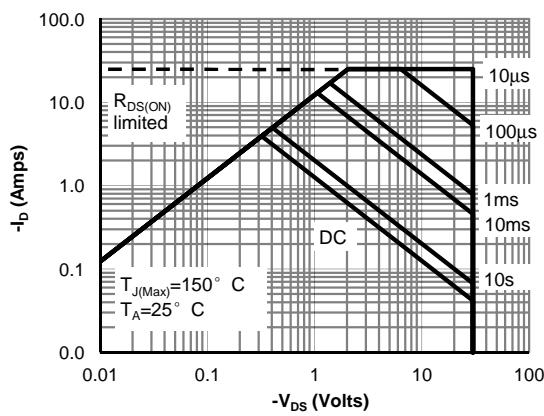
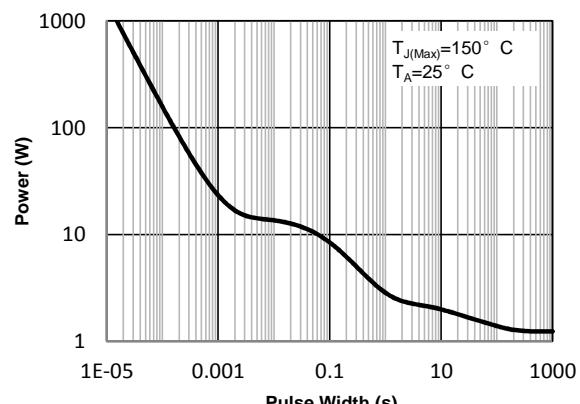
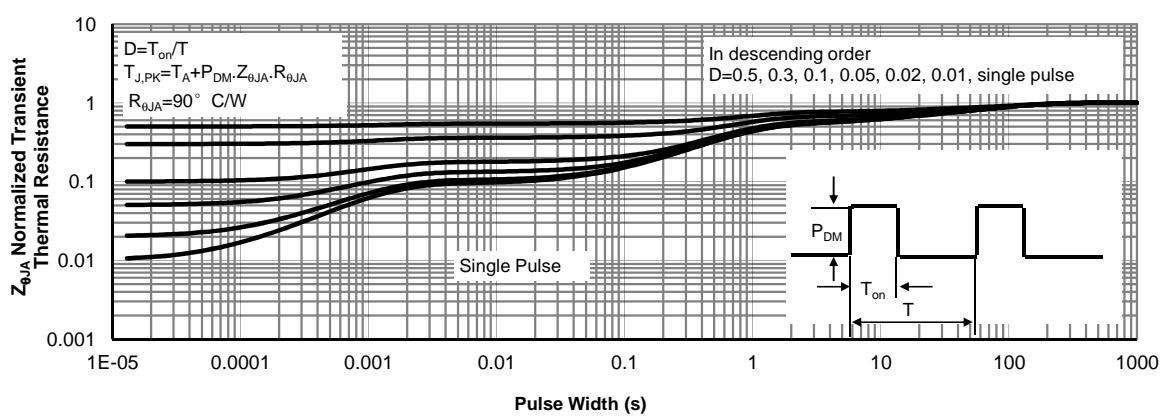
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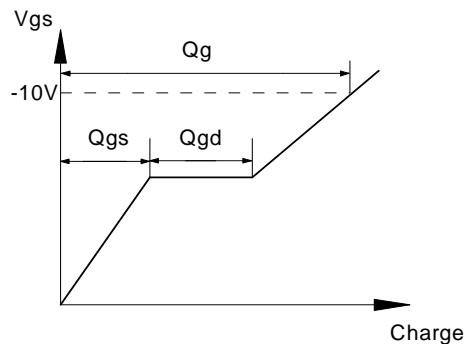
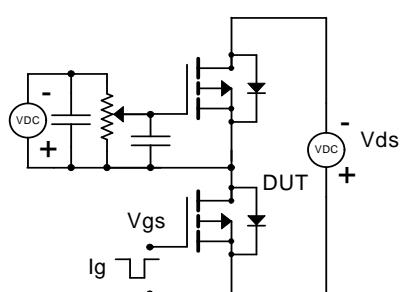
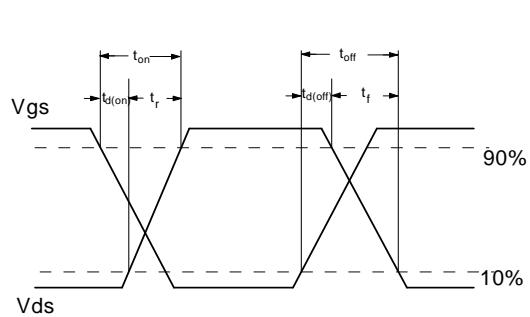
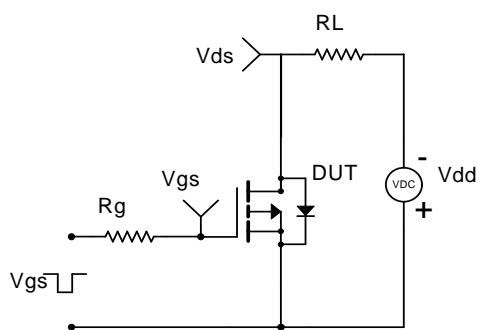
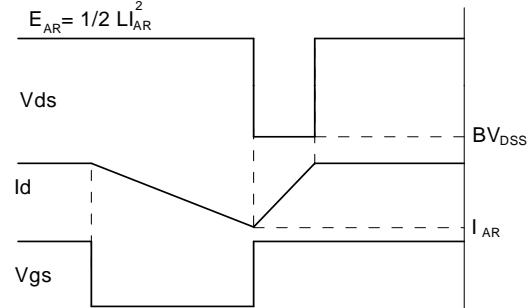
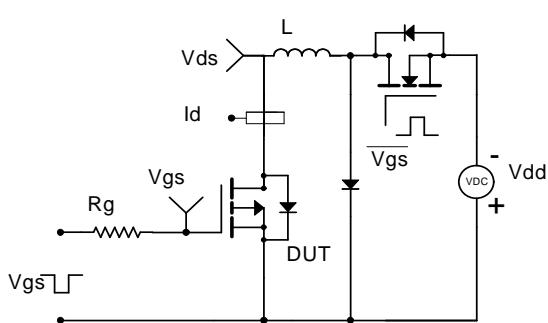
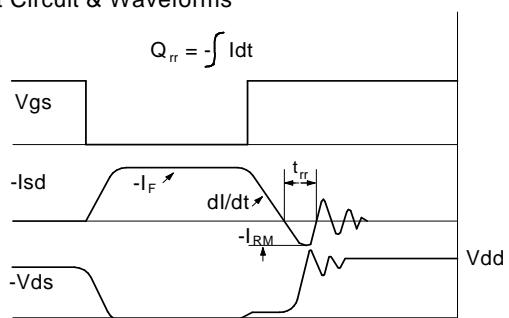
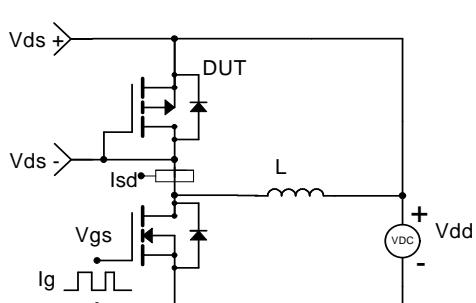
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Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

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Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Diode Recovery Test Circuit & Waveforms




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