# AO6602

## 30V Complementary MOSFET

## General Description

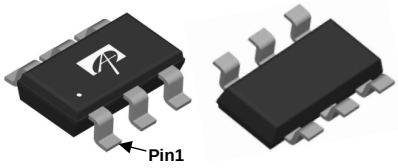
The AO6602 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications.

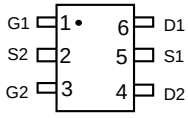
## Product Summary

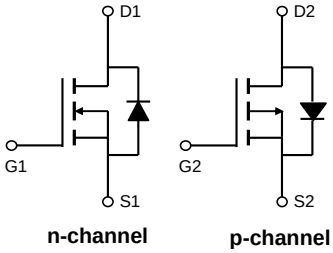
| N-Channel | P-Channel |
|---|---|
| $V_{DS}$= 30V | -30V |
| $I_D$= 3.5A ($V_{GS}$=10V) | -2.7A ($V_{GS}$=-10V) |
| $R_{DS(ON)}$ | $R_{DS(ON)}$ |
| < 50mΩ ($V_{GS}$=10V) | < 100mΩ ($V_{GS}$=-10V) |
| < 70mΩ ($V_{GS}$=4.5V) | < 170mΩ ($V_{GS}$=-4.5V) |

Green Product

**TSOP6**




**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | Max n-channel | Max p-channel | Units |
|---|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 30 | -30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | ±20 | V |
| Continuous Drain Current | $T_A$=25°C | $I_D$ | 3.5 | -2.7 | A |
| | $T_A$=70°C | | 3 | -2.1 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 20 | -15 | |
| Power Dissipation [B] | $T_A$=25°C | $P_D$ | 1.15 | 1.15 | W |
| | $T_A$=70°C | | 0.73 | 0.73 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | | °C |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 78 | 110 | °C/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 106 | 150 | °C/W |
| Maximum Junction-to-Lead | Steady-State | $R_{\theta JL}$ | 64 | 80 | °C/W |

**N-Channel Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=30V, $V_{GS}$=0V | | | 1 | µA |
| | | $T_J$=55°C | | | 5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±20V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250µA | 1.5 | 2 | 2.5 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 20 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=3.5A | | 40 | 50 | mΩ |
| | | $T_J$=125°C | | 61 | 77 | |
| | | $V_{GS}$=4.5V, $I_D$=2A | | 52 | 70 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=3.5A | | 12 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.79 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 1.5 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=15V, f=1MHz | | 170 | 210 | pF |
| $C_{oss}$ | Output Capacitance | | | 35 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 23 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 1.7 | 3.5 | 5.3 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=15V, $I_D$=3.5A | | 4.05 | 5 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 2 | 3 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 0.55 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 1 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=15V, $R_L$=4.2Ω, $R_{GEN}$=3Ω | | 4.5 | | ns |
| $t_r$ | Turn-On Rise Time | | | 1.5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 18.5 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 15.5 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=3.5A, dI/dt=100A/µs | | 7.5 | 10 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=3.5A, dI/dt=100A/µs | | 2.5 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial$T_J$=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse ratin g.

## N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

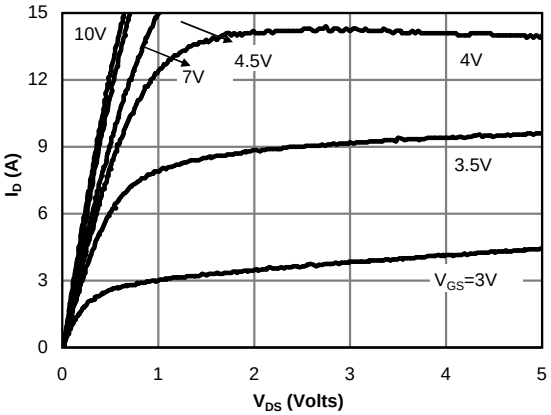



Fig 1: On-Region Characteristics (Note E)

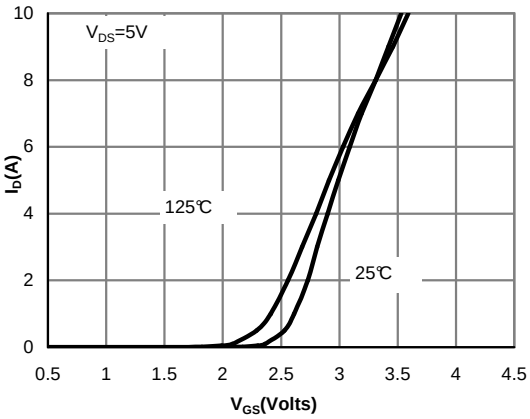



Figure 2: Transfer Characteristics (Note E)

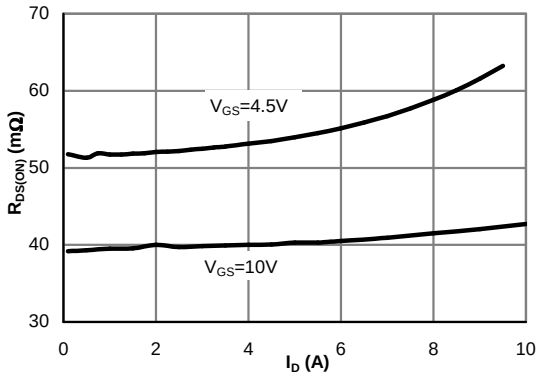



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

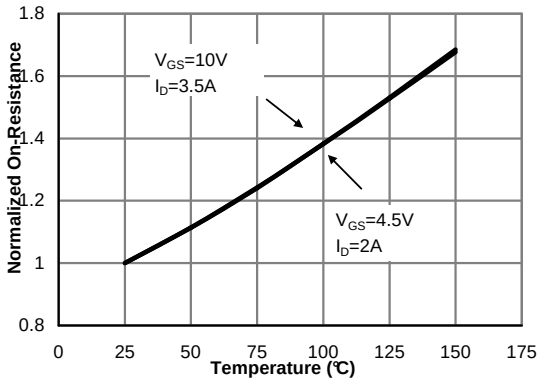



Figure 4: On-Resistance vs. Junction Temperature (Note E)

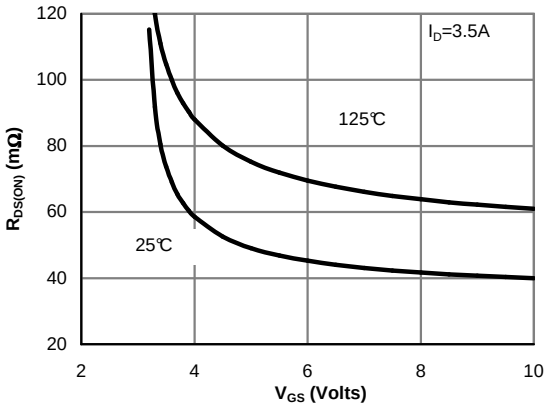



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

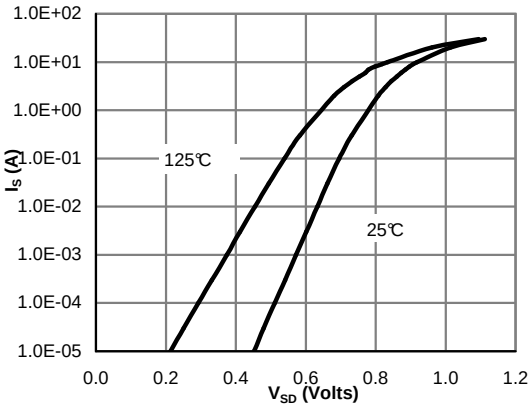



Figure 6: Body-Diode Characteristics (Note E)

## N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

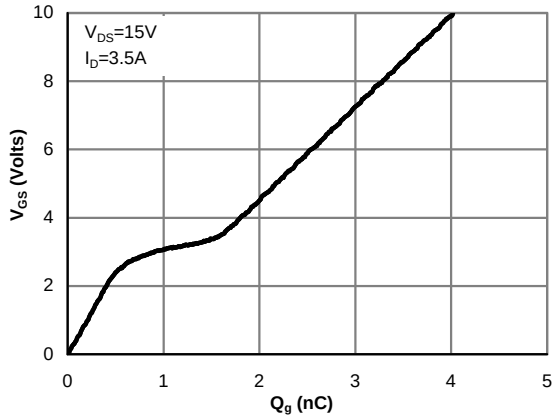



Figure 7: Gate-Charge Characteristics

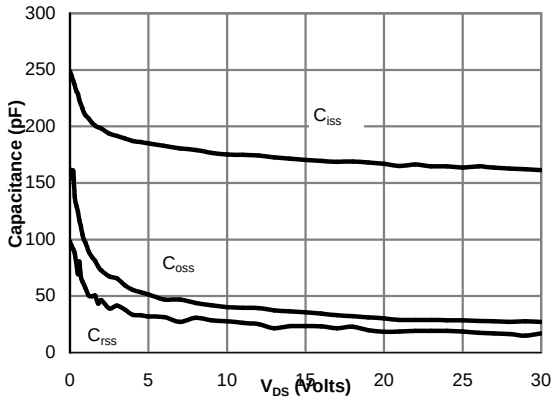



Figure 8: Capacitance Characteristics

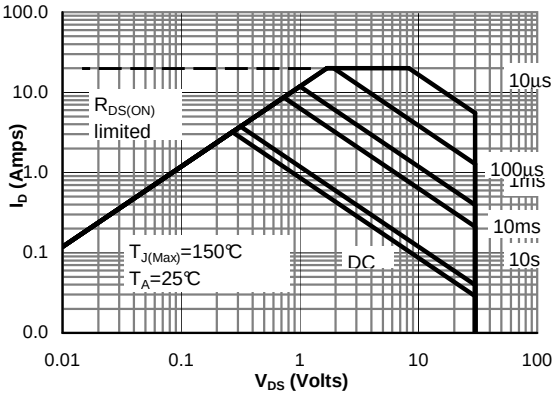



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

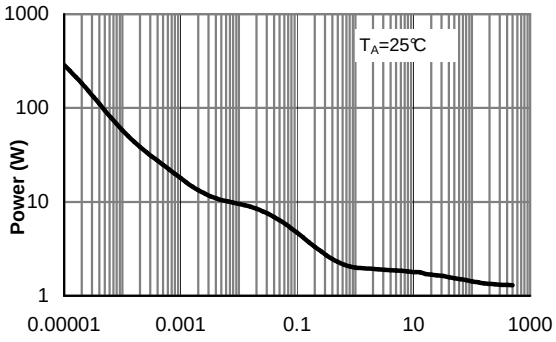



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

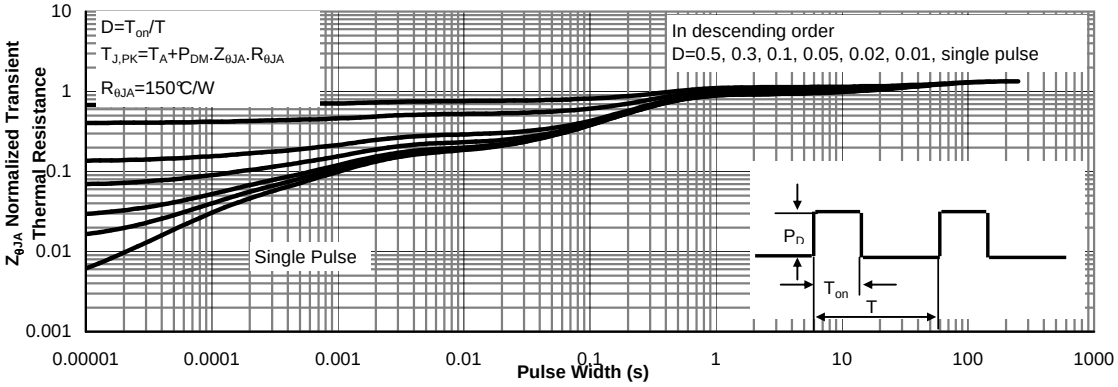
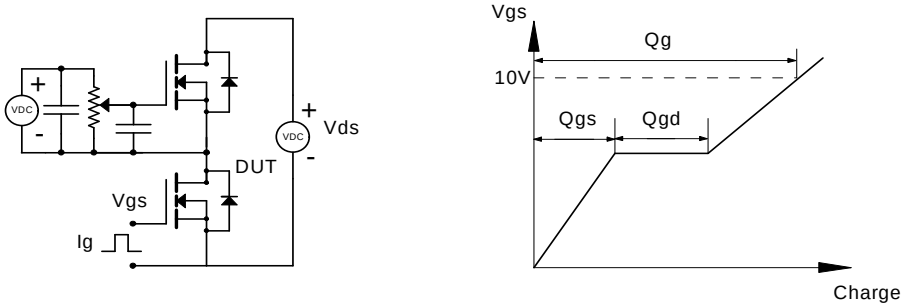
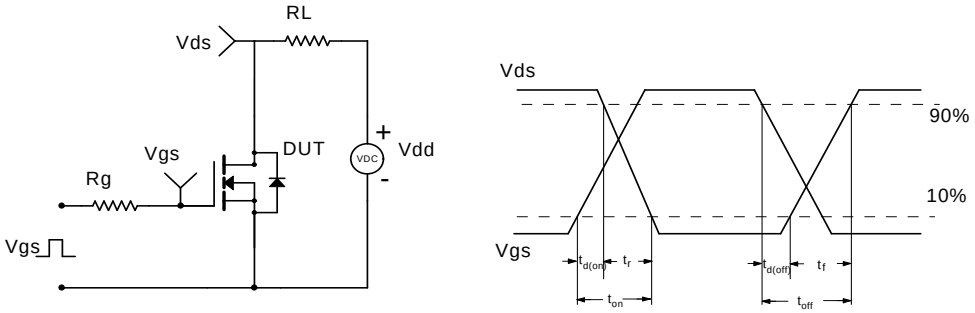



Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

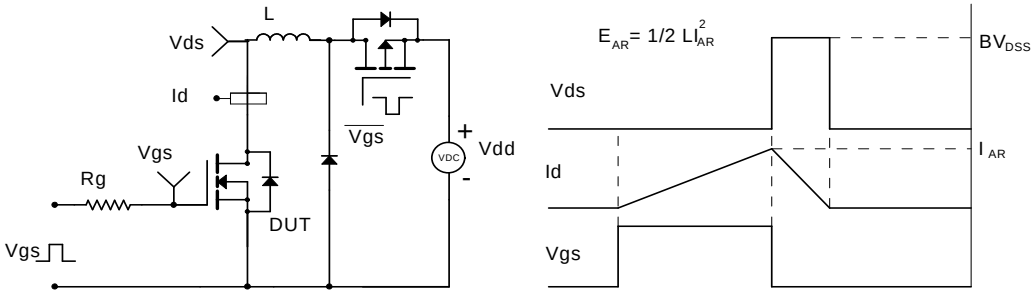
## Gate Charge Test Circuit & Waveform



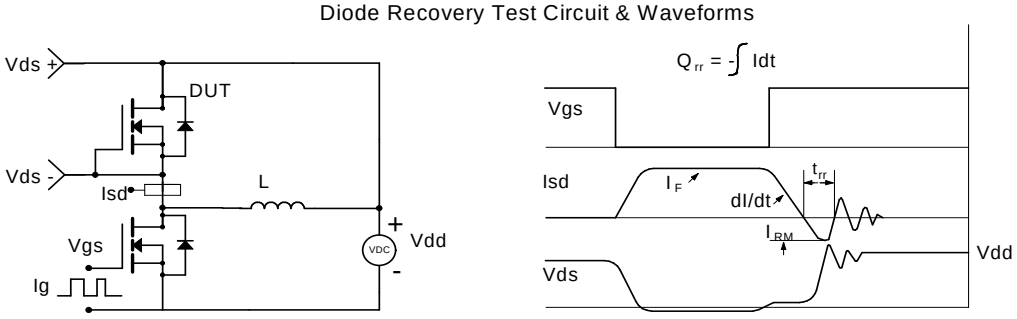

## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms



**P-Channel Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=-250µA, $V_{GS}$=0V | -30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=-30V, $V_{GS}$=0V | | | -1 | µA |
| | | $T_J$=55°C | | | -5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±20V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=-250µA | -1.4 | -1.9 | -2.4 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=-10V, $V_{DS}$=-5V | -15 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=-10V, $I_D$=-2.7A | | 82 | 100 | mΩ |
| | | $T_J$=125°C | | 115 | 140 | |
| | | $V_{GS}$=-4.5V, $I_D$=-2A | | 130 | 170 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=-5V, $I_D$=-2.7A | | 5.5 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=-1A,$V_{GS}$=0V | | -0.8 | -1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | -1.5 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=-15V, f=1MHz | | 197 | 240 | pF |
| $C_{oss}$ | Output Capacitance | | | 42 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 26 | 37 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 3.5 | 7.2 | 11.0 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=-15V, $I_D$=2.7A | | 4.3 | 5.2 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 2.2 | 3 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 0.7 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 1.1 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=-15V, $R_L$=5.55Ω, $R_{GEN}$=3Ω | | 7.5 | | ns |
| $t_r$ | Turn-On Rise Time | | | 4.1 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 11.8 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 3.8 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=-2.7A, dI/dt=100A/µs | | 11.3 | 14 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=-2.7A, dI/dt=100A/µs | | 4.4 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial$T_J$=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse ratin g.

## P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

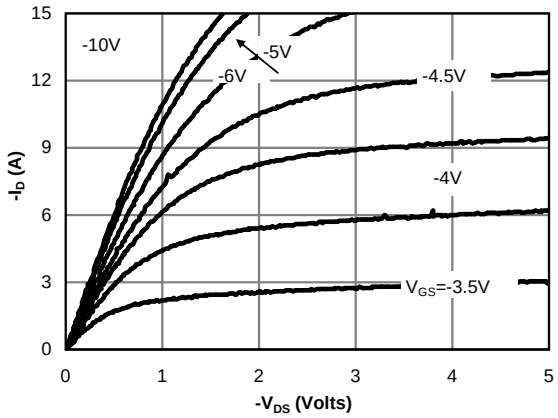



Fig 1: On-Region Characteristics (Note E)

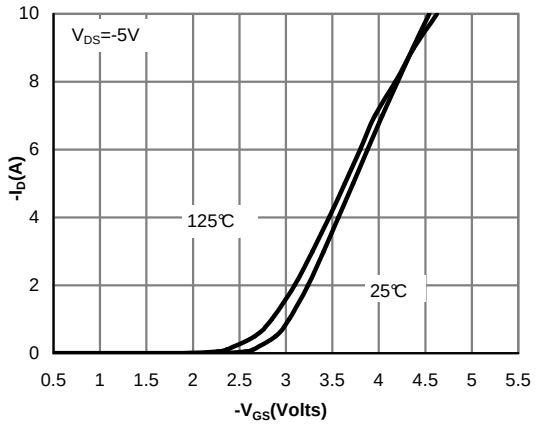



Figure 2: Transfer Characteristics (Note E)

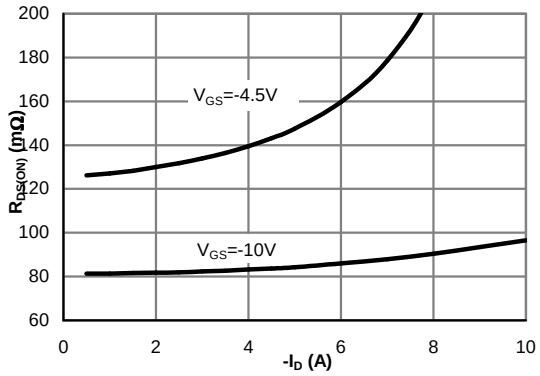



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

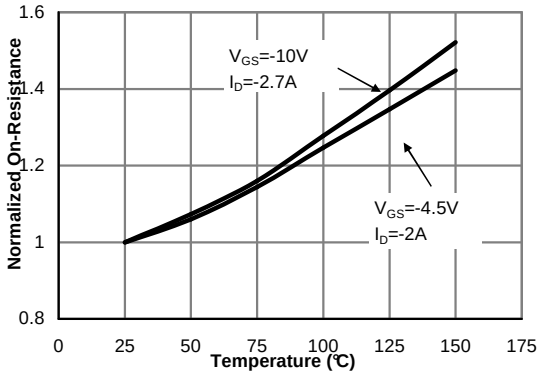



Figure 4: On-Resistance vs. Junction Temperature (Note E)

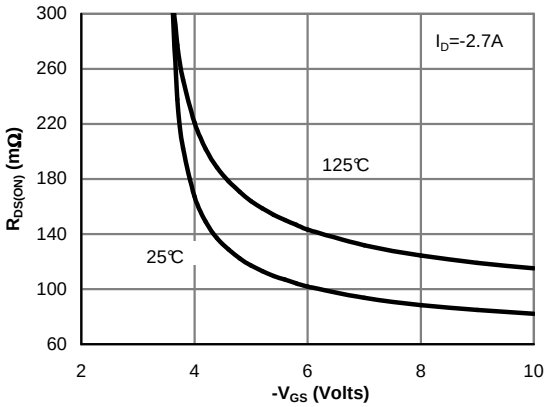



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

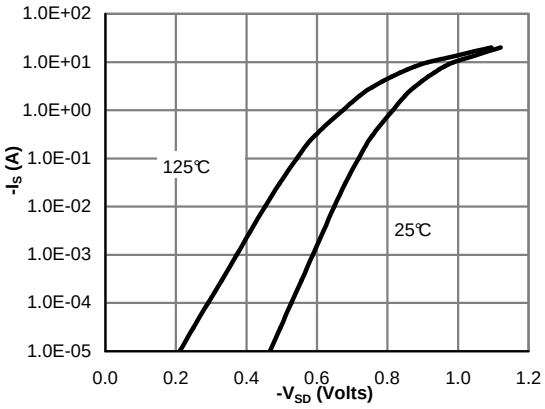



Figure 6: Body-Diode Characteristics (Note E)

## P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

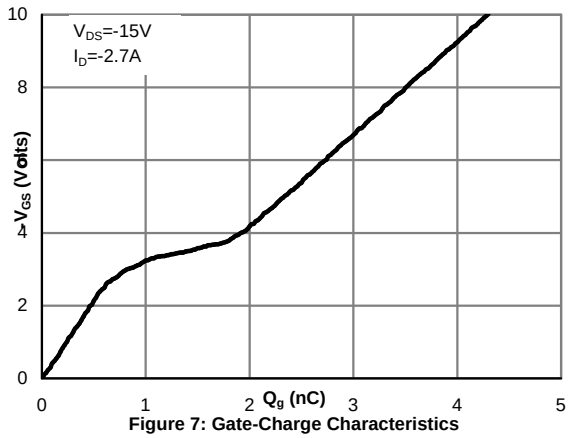



Figure 7: Gate-Charge Characteristics

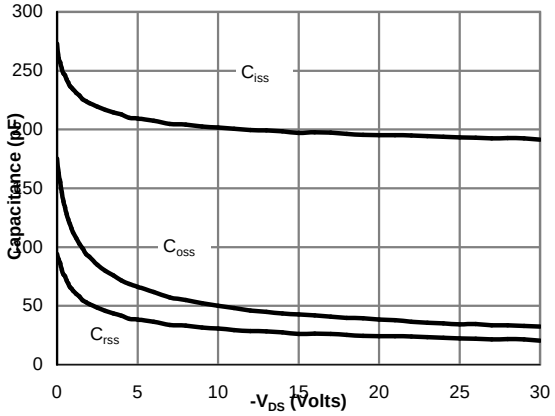



Figure 8: Capacitance Characteristics

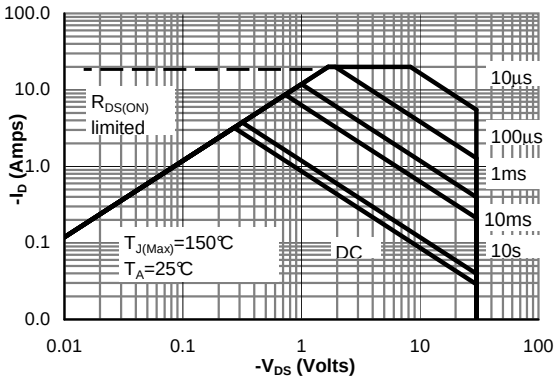



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

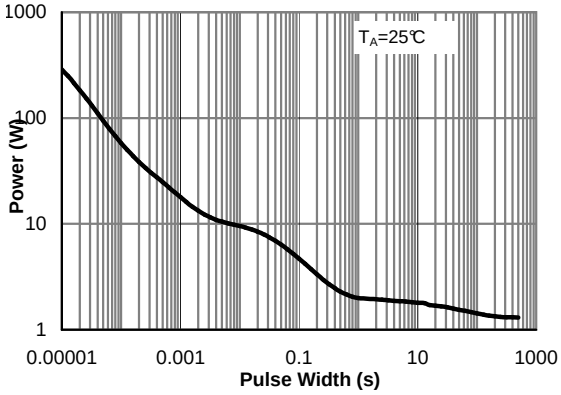



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

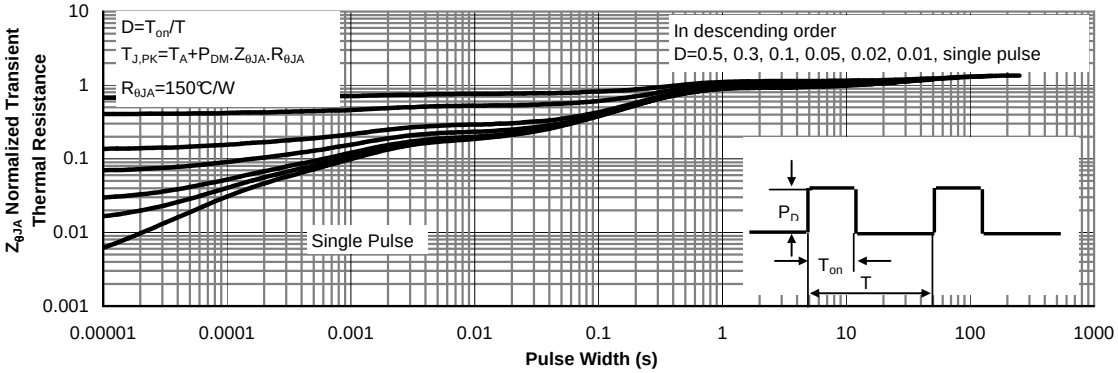
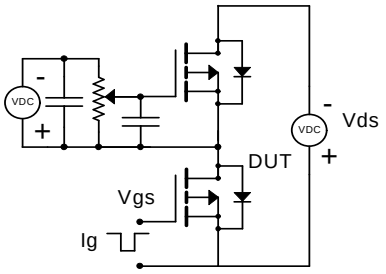
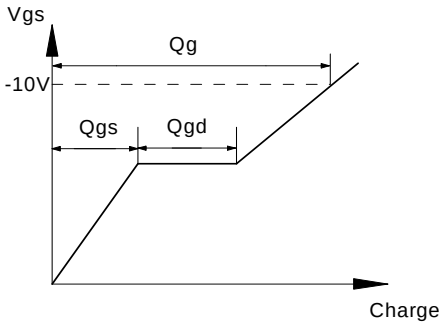


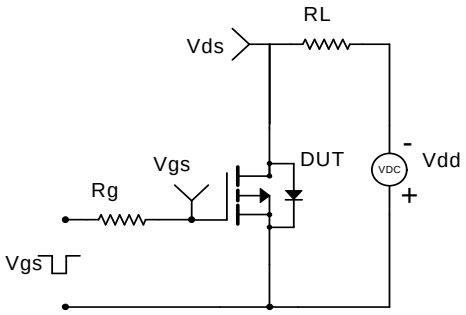

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

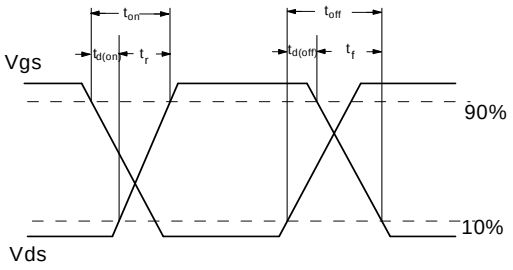
## Gate Charge Test Circuit & Waveform



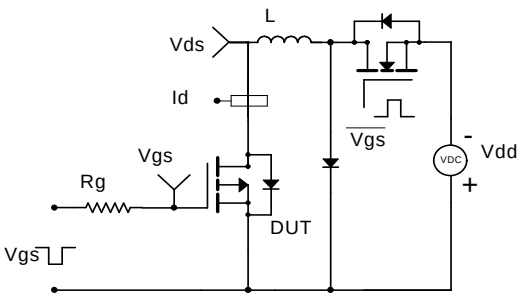



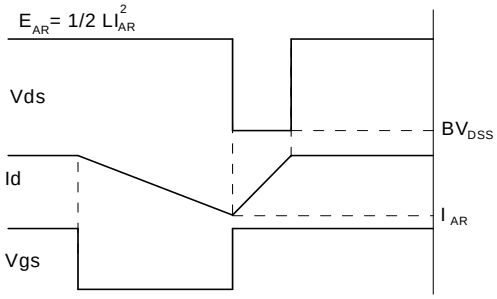

## Resistive Switching Test Circuit & Waveforms



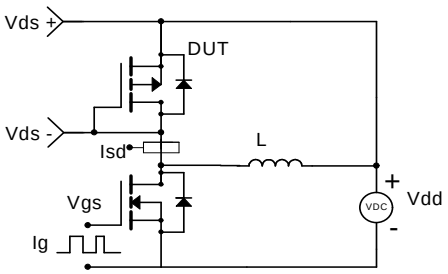



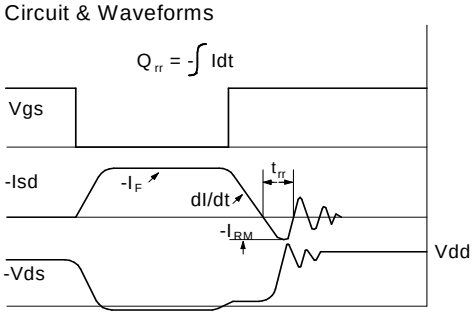

## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms



单击下面可查看定价，库存，交付和生命周期等信息

>>AOS(万代)