



General Description

The AO6608 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

- RoHS and Halogen-Free Compliant

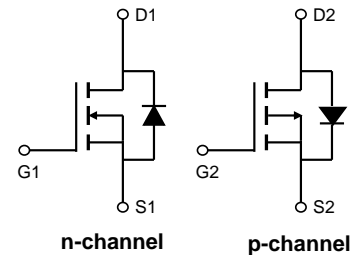
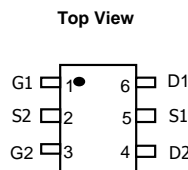
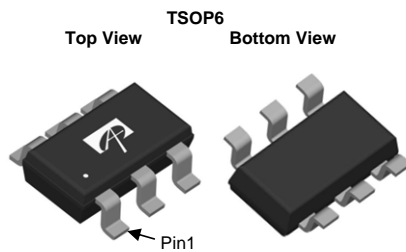
Product Summary

N-Channel

$V_{DS} = 30V$
 $I_D = 3.4A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 60m\Omega$ ($V_{GS} = 10V$)
 $< 70m\Omega$ ($V_{GS} = 4.5V$)
 $< 90m\Omega$ ($V_{GS} = 2.5V$)

P-Channel

$-20V$
 $-3.3A$ ($V_{GS} = -4.5V$)
 $R_{DS(ON)} < 75m\Omega$ ($V_{GS} = -4.5V$)
 $< 105m\Omega$ ($V_{GS} = -2.5V$)
 $< 135m\Omega$ ($V_{GS} = -1.8V$)



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	30	-20	V
Gate-Source Voltage	V_{GS}	± 12	± 8	V
Continuous Drain Current	I_D	$T_A = 25^\circ C$	-3.3	A
		$T_A = 70^\circ C$	-2.5	
Pulsed Drain Current ^C	I_{DM}	20	-13	
Power Dissipation ^B	P_D	$T_A = 25^\circ C$	1.25	W
		$T_A = 70^\circ C$	0.80	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	75	100	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	105	130
Maximum Junction-to-Lead	$R_{\theta JL}$	50	65	$^\circ C/W$

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.5	1	1.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =3.4A T _J =125°C		46 73	60 88	mΩ
		V _{GS} =4.5V, I _D =3A		50	70	
		V _{GS} =2.5V, I _D =2A		62	90	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =3.4A		14		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				1.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		235		pF
C _{oss}	Output Capacitance			35		pF
C _{rss}	Reverse Transfer Capacitance			18		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =3.4A		6	10	nC
Q _g (4.5V)	Total Gate Charge			3		nC
Q _{gs}	Gate Source Charge			0.55		nC
Q _{gd}	Gate Drain Charge			0.8		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =4.4Ω, R _{GEN} =3Ω		1.5		ns
t _r	Turn-On Rise Time			2.5		ns
t _{D(off)}	Turn-Off DelayTime			16		ns
t _f	Turn-Off Fall Time			2		ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =3.4A, di/dt=100A/μs		6	
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =3.4A, di/dt=100A/μs		1.2		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

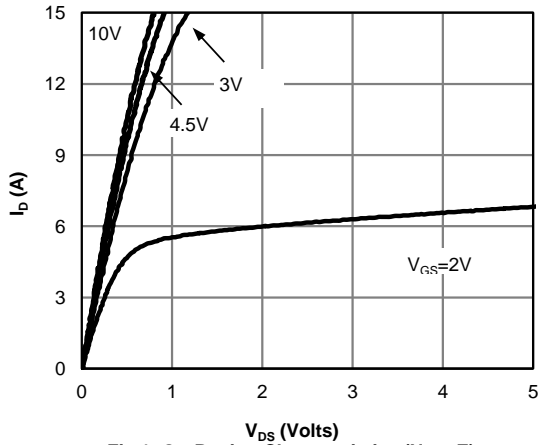


Figure 1: On-Region Characteristics (Note E)

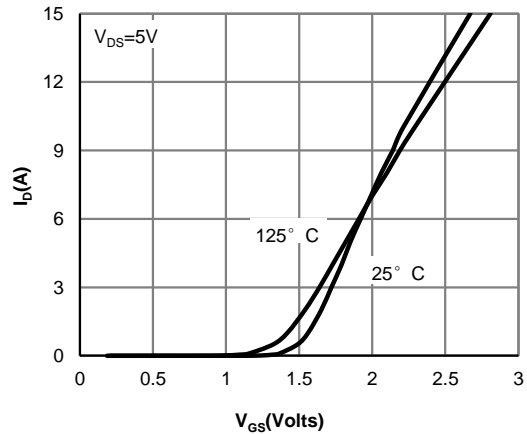


Figure 2: Transfer Characteristics (Note E)

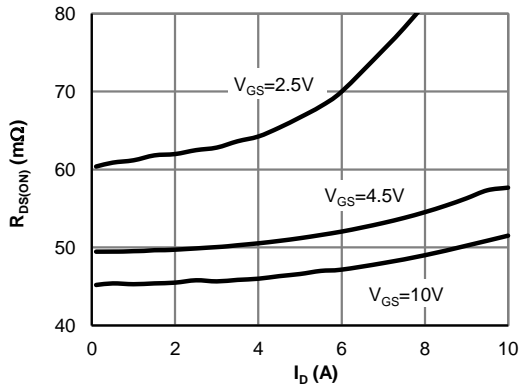


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

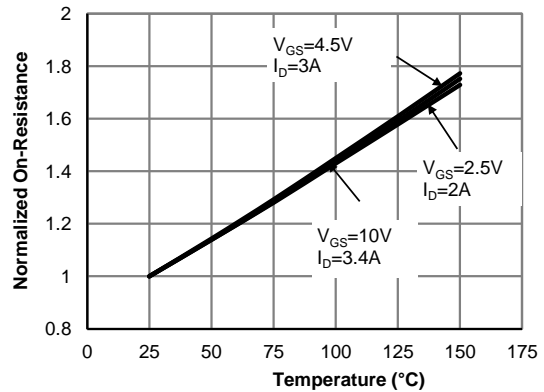


Figure 4: On-Resistance vs. Junction Temperature (Note E)

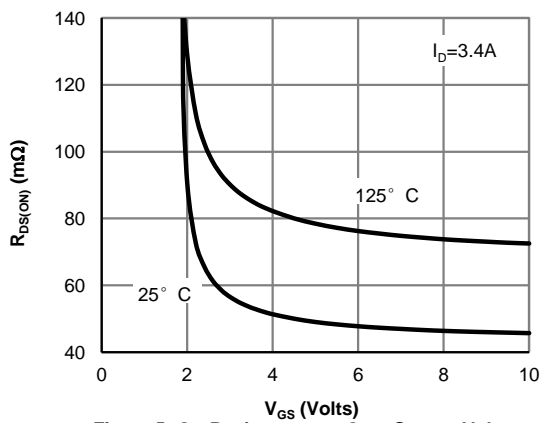


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

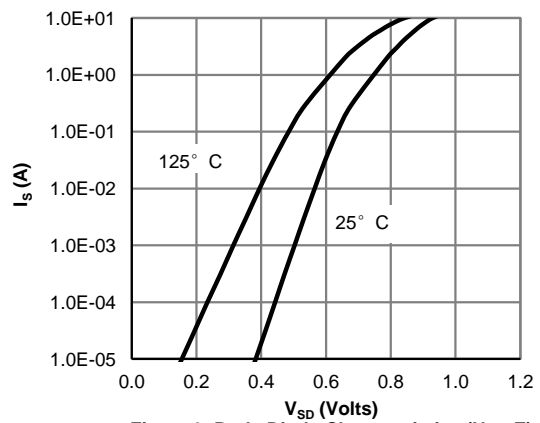


Figure 6: Body-Diode Characteristics (Note E)

N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

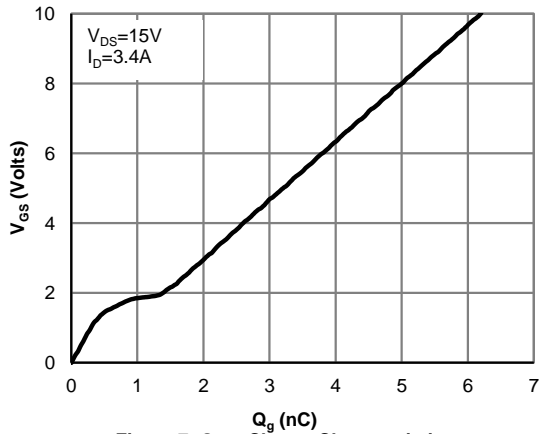


Figure 7: Gate-Charge Characteristics

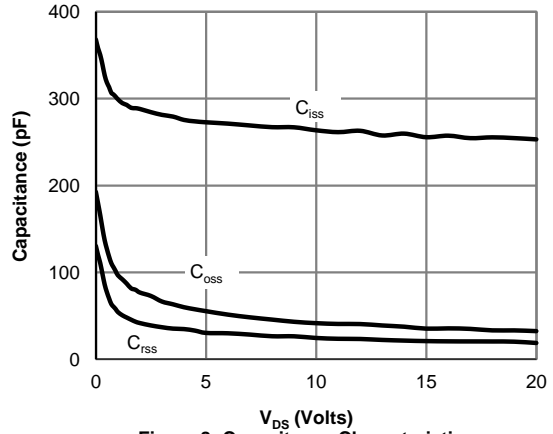


Figure 8: Capacitance Characteristics

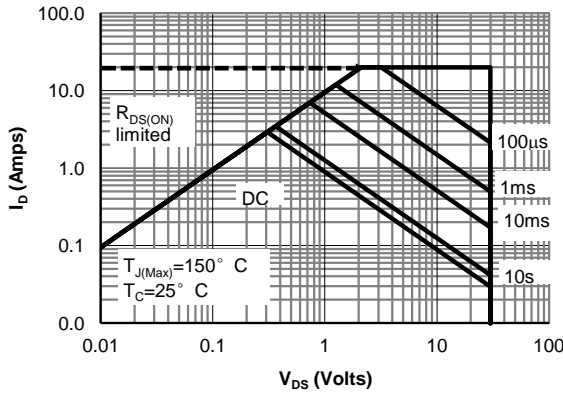


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

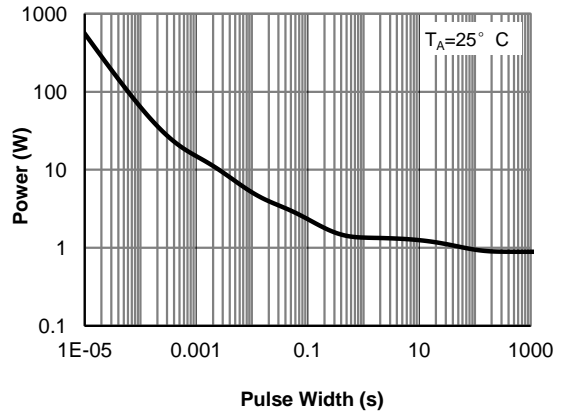


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

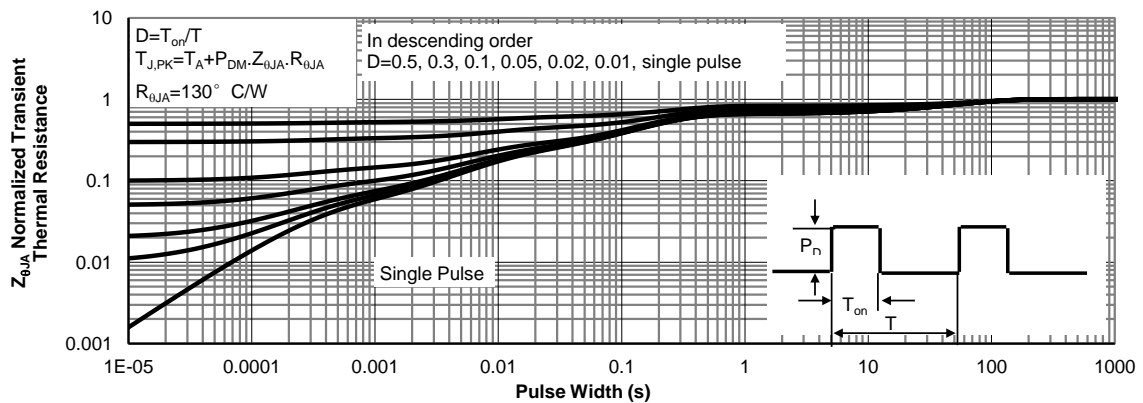
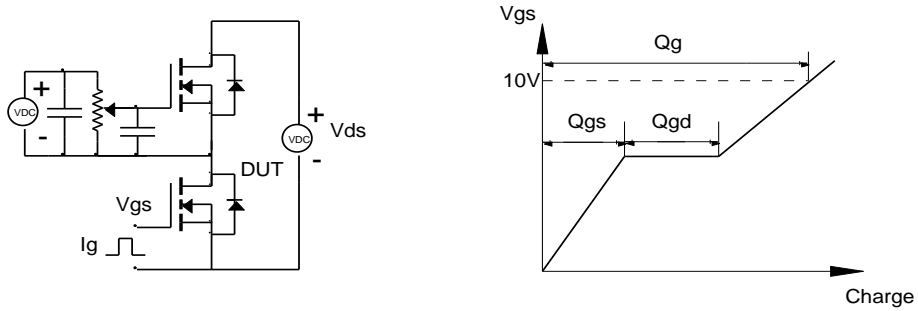
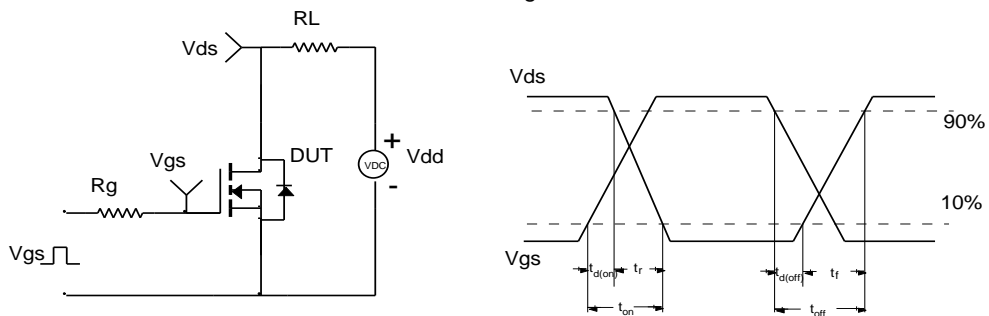


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

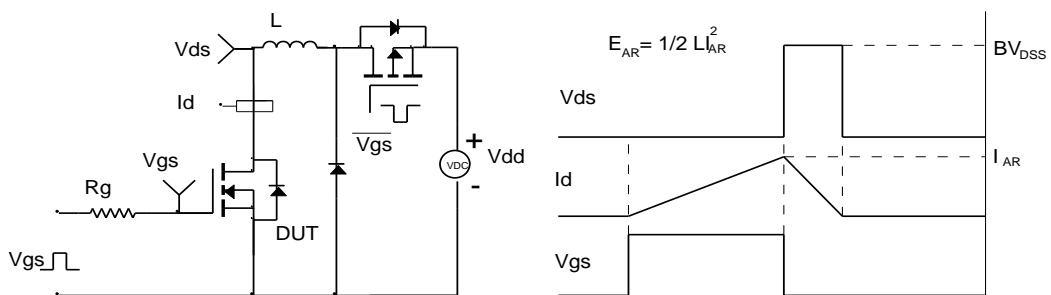
Gate Charge Test Circuit & Waveform



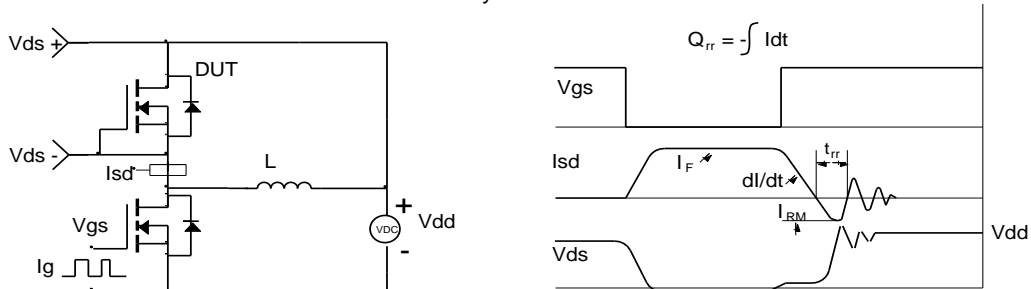
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±8V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-0.4	-0.65	-1	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-3.3A T _J =125°C		63	75	mΩ
		V _{GS} =-2.5V, I _D =-2.5A		78	105	
		V _{GS} =-1.8V, I _D =-1A		96	135	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-3.3A		13		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1	V
I _S	Maximum Body-Diode Continuous Current				-1.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-10V, f=1MHz		510		pF
C _{oss}	Output Capacitance			70		pF
C _{riss}	Reverse Transfer Capacitance			50		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		15	30	Ω
SWITCHING PARAMETERS						
Q _{g(4.5V)}	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-3.3A		6	10	nC
Q _{gs}	Gate Source Charge			0.6		nC
Q _{gd}	Gate Drain Charge			1.8		nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =-4.5V, V _{DS} =-10V, R _L =4Ω, R _{GEN} =6Ω		11		ns
t _r	Turn-On Rise Time			11		ns
t _{D(off)}	Turn-Off Delay Time			60		ns
t _f	Turn-Off Fall Time			30		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-3.3A, dI/dt=100A/μs		16		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-3.3A, dI/dt=100A/μs		4		nC

A. The value of R_{th(j-a)} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_a=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{th(j-a)} is the sum of the thermal impedance from junction to lead R_{th(j-l)} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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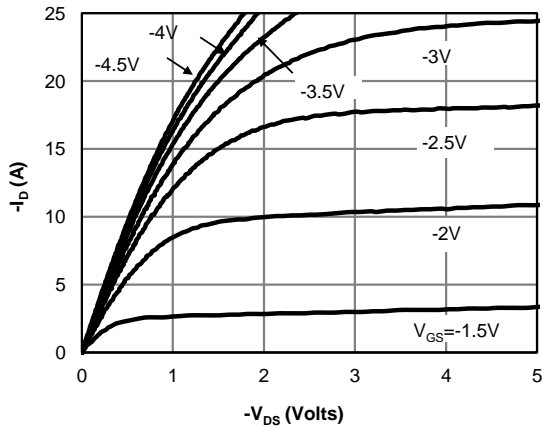


Fig 1: On-Region Characteristics (Note E)

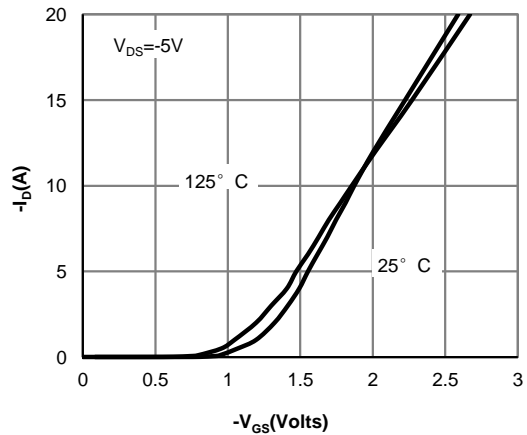


Figure 2: Transfer Characteristics (Note E)

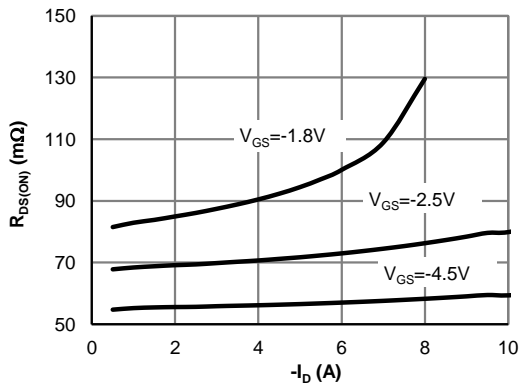


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

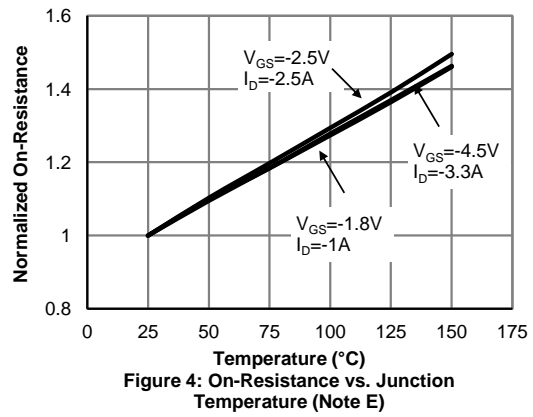


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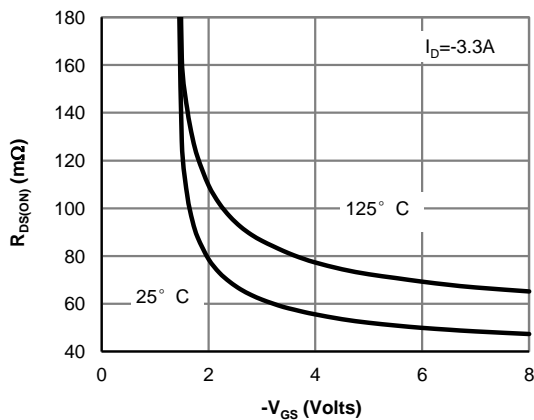


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

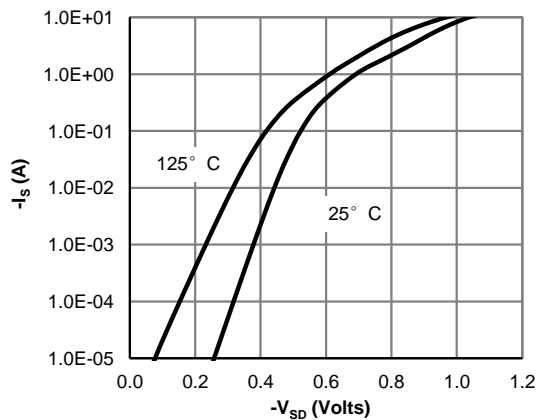


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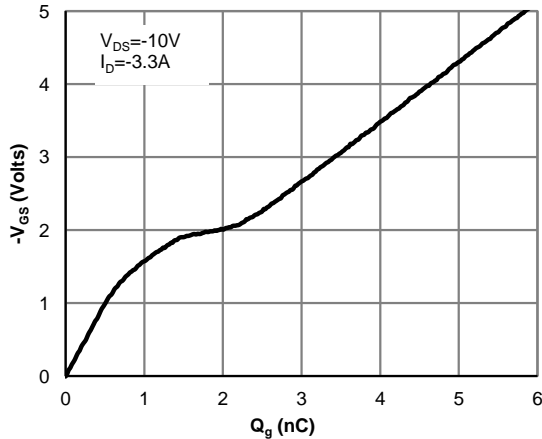


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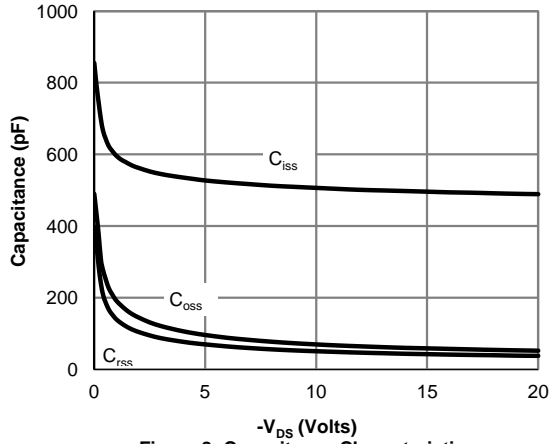


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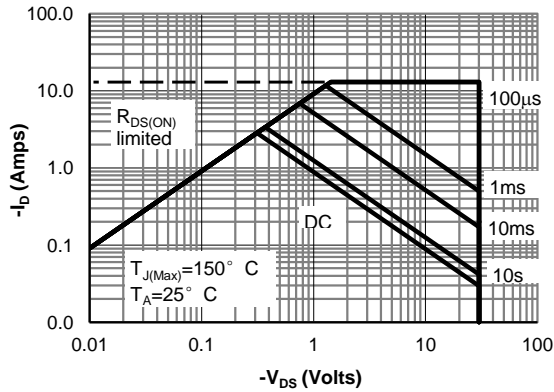


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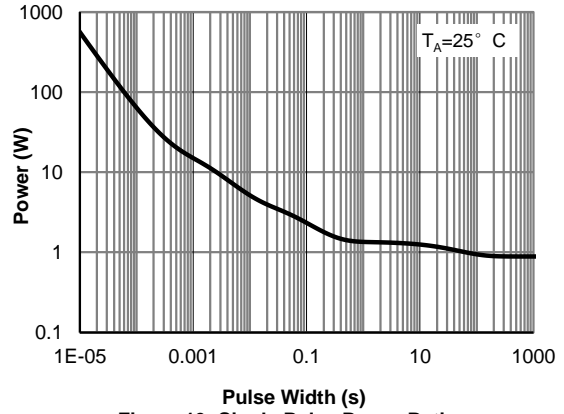


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

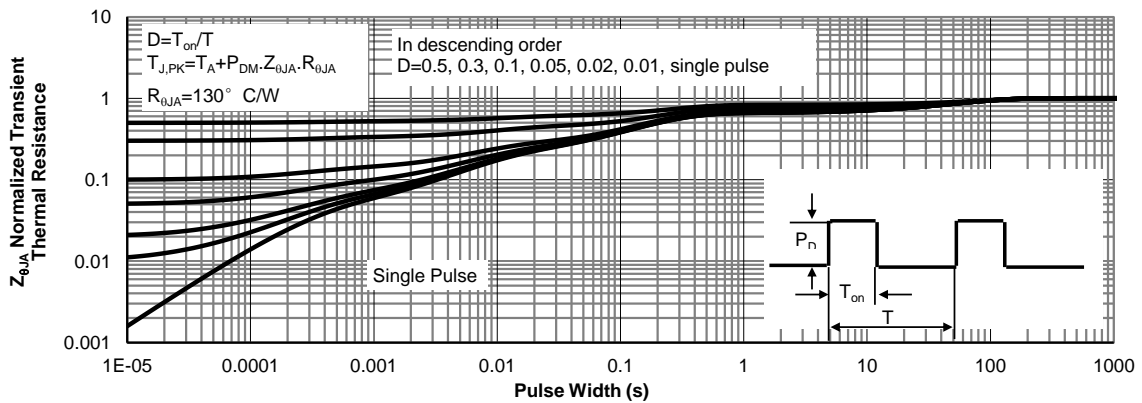
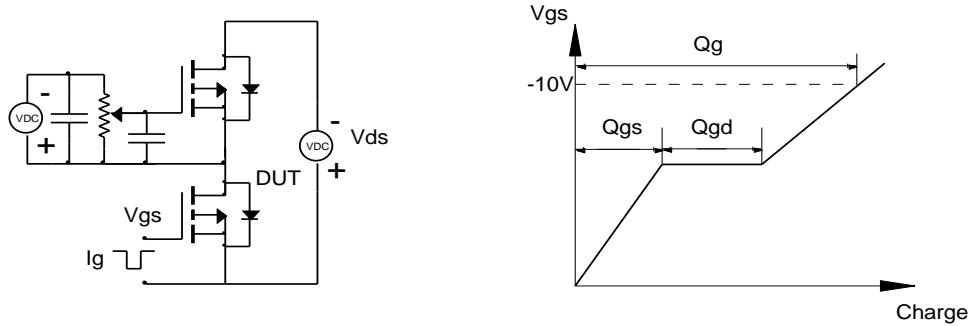
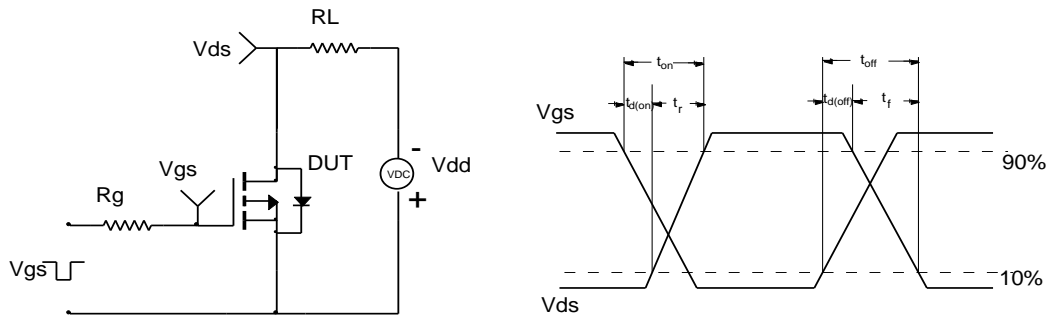


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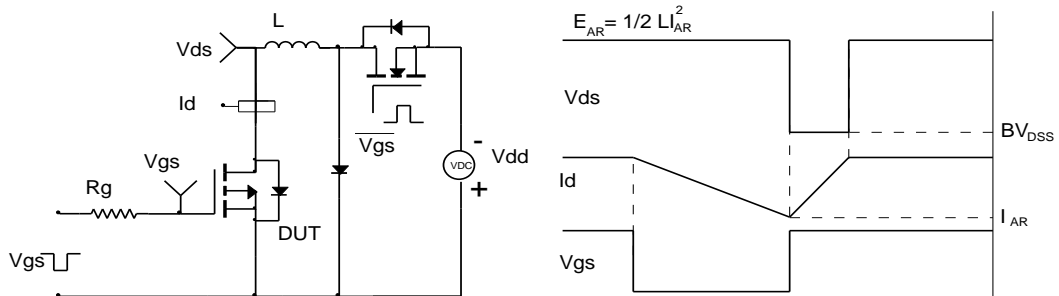
Gate Charge Test Circuit & Waveform



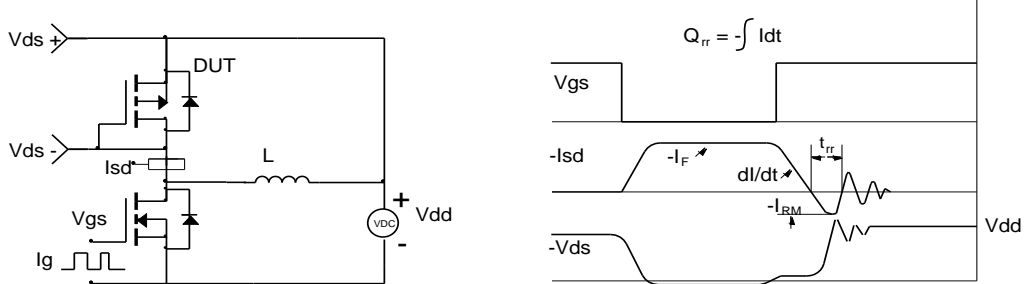
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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