

AO7801 Dual P-Channel Enhancement Mode Field Effect Transistor

General Description

The AO7801 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge, and operation with gate voltages as low as 1.8V, in the small SOT363 footprint. It can be used for a wide variety of applications, including load switching, low current inverters and low current DC-DC converters. It is ESD protected to 2KV HBM.

Features

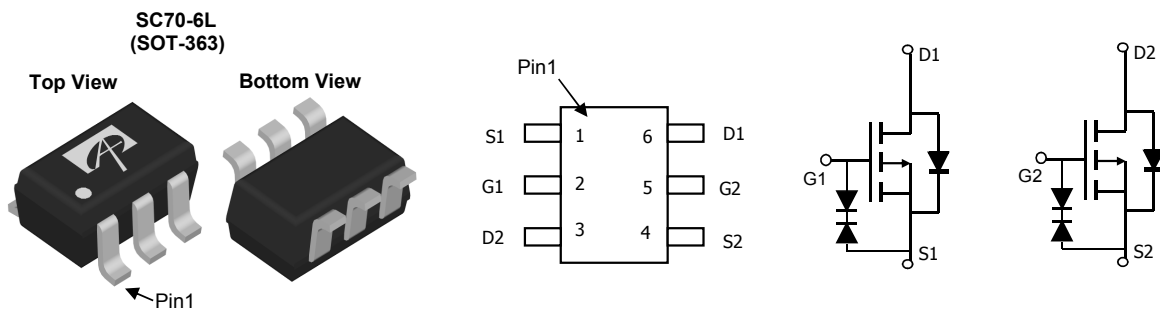
$$V_{DS} (V) = -20V$$

$$I_D = -0.6A (V_{GS} = -4.5V)$$

$$R_{DS(ON)} < 520m\Omega (V_{GS} = -4.5V)$$

$$R_{DS(ON)} < 700m\Omega (V_{GS} = -2.5V)$$

$$R_{DS(ON)} < 950m\Omega (V_{GS} = -1.8V)$$



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ^A	I_D	$T_A=25^\circ C$	-0.6
		$T_A=70^\circ C$	-0.48
Pulsed Drain Current ^B	I_{DM}	-3	A
Power Dissipation ^A	P_D	$T_A=25^\circ C$	0.3
		$T_A=70^\circ C$	0.19
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	360	415
Maximum Junction-to-Ambient ^A		Steady-State	400	460
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	300	350	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-16V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±8V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.5	-0.6	-0.9	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-3			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-0.6A T _J =125°C		400 542	520 700	mΩ
		V _{GS} =-2.5V, I _D =-0.5A		540	700	mΩ
		V _{GS} =-1.8V, I _D =-0.4A		700	950	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-0.6A		1.7		S
V _{SD}	Diode Forward Voltage	I _S =-0.5A, V _{GS} =0V		-0.86	-1	V
I _S	Maximum Body-Diode Continuous Current				-0.4	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-10V, f=1MHz		114	140	pF
C _{oss}	Output Capacitance			17		pF
C _{rss}	Reverse Transfer Capacitance			14		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		12	17	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-0.6A		1.44	1.8	nC
Q _{gs}	Gate Source Charge			0.14		nC
Q _{gd}	Gate Drain Charge			0.35		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-4.5V, V _{DS} =-10V, R _L =16.7Ω, R _{GEN} =3Ω		6.5		ns
t _r	Turn-On Rise Time			6.5		ns
t _{D(off)}	Turn-Off DelayTime			18.2		ns
t _f	Turn-Off Fall Time			5.5		ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =-0.6A, dI/dt=100A/μs		10	13
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-0.6A, dI/dt=100A/μs		3		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

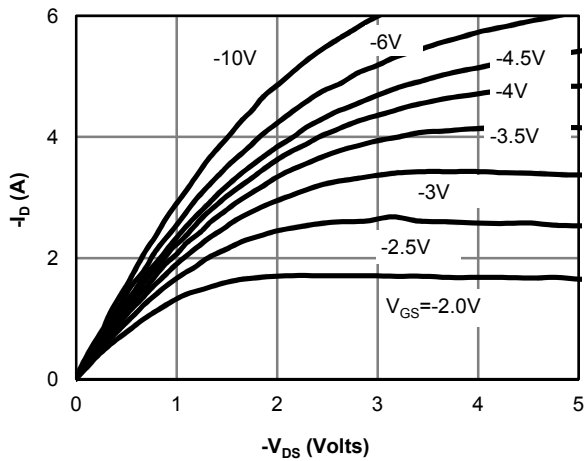


Fig 1: On-Region Characteristics

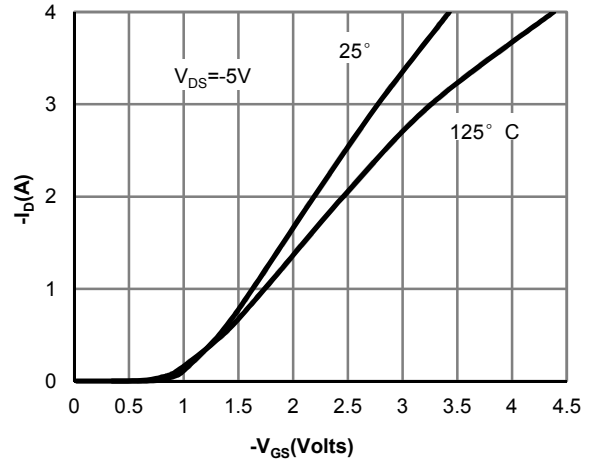


Figure 2: Transfer Characteristics

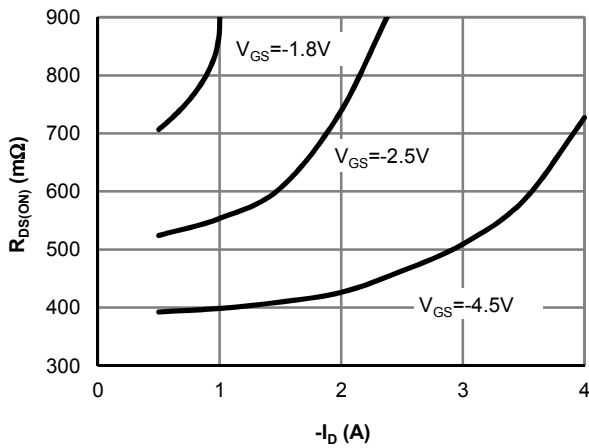


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

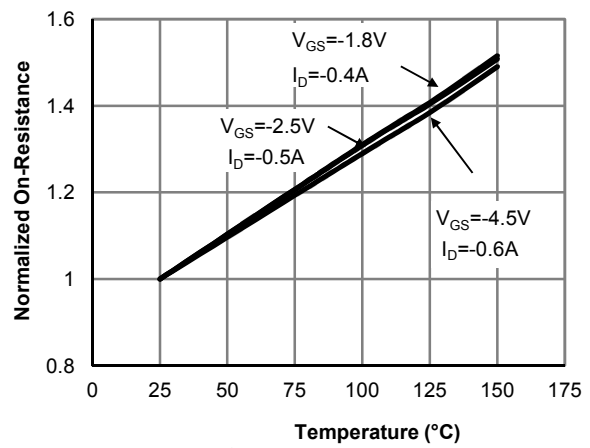


Figure 4: On-Resistance vs. Junction Temperature

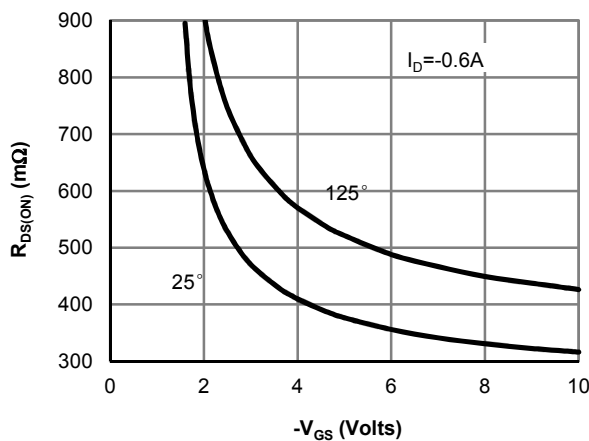


Figure 5: On-Resistance vs. Gate-Source Voltage

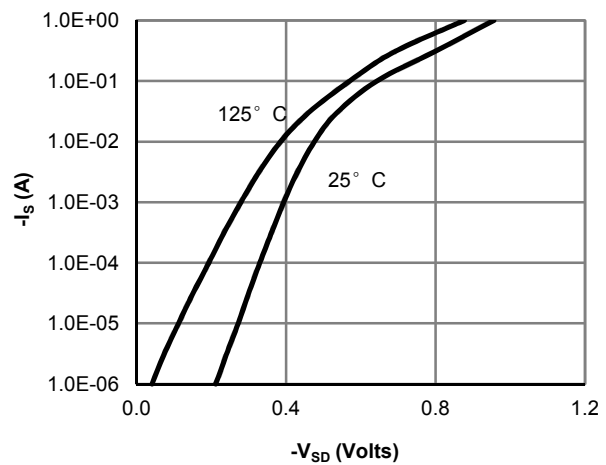


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

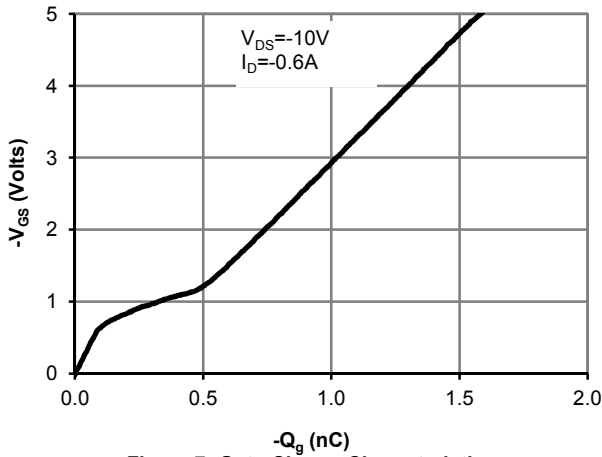


Figure 7: Gate-Charge Characteristics

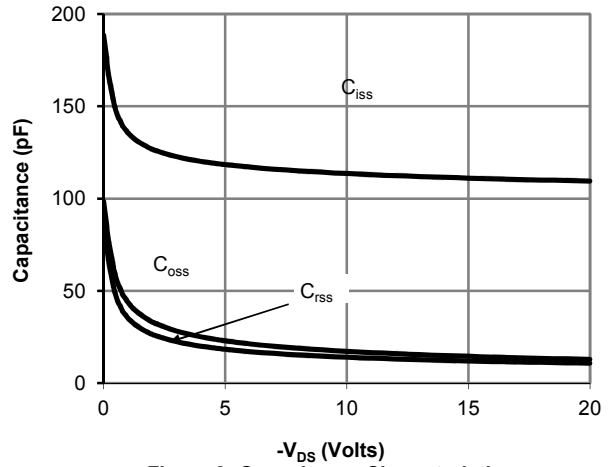


Figure 8: Capacitance Characteristics

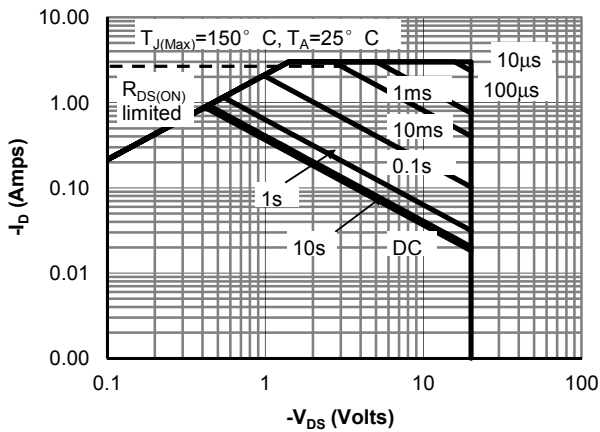


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

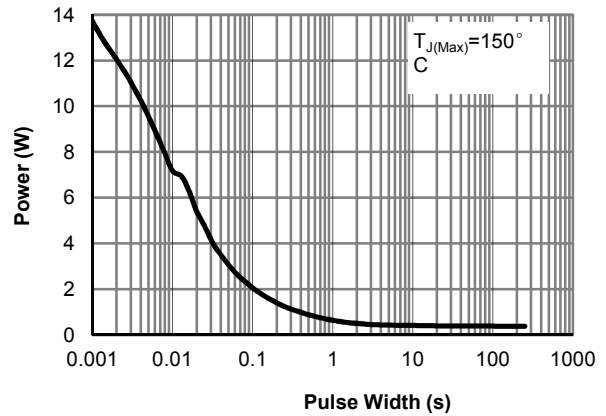


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

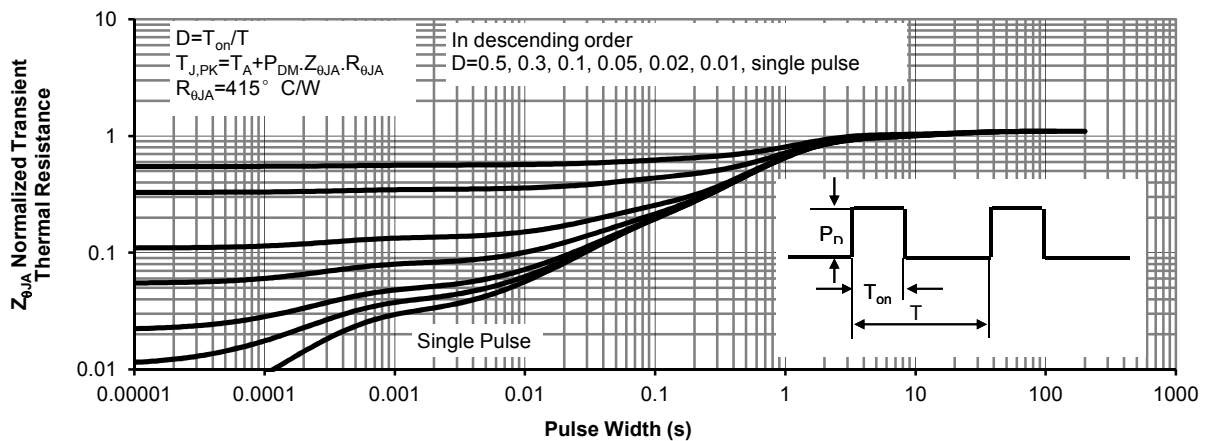
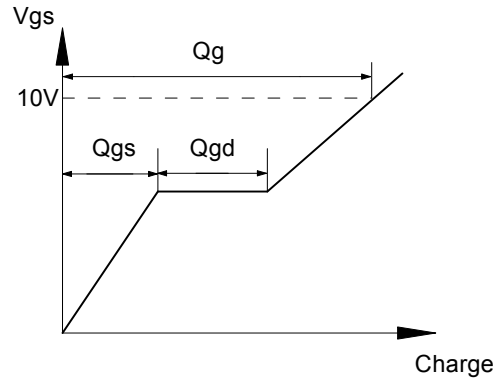
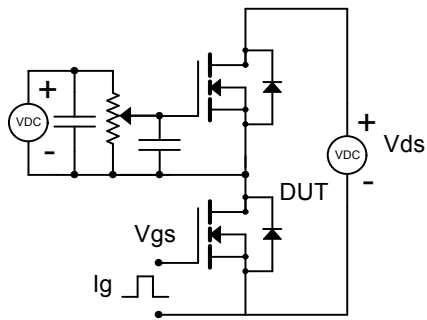
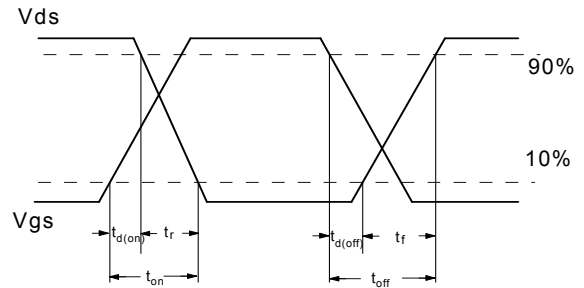
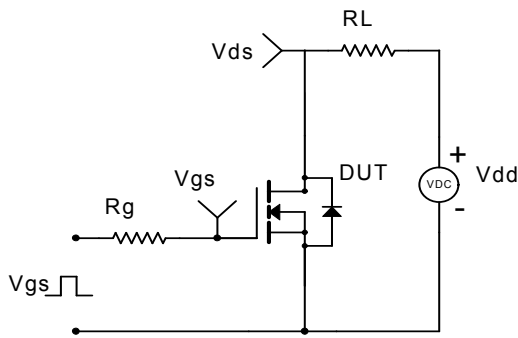


Figure 11: Normalized Maximum Transient Thermal Impedance

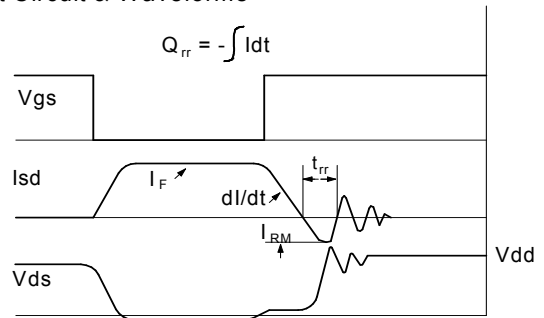
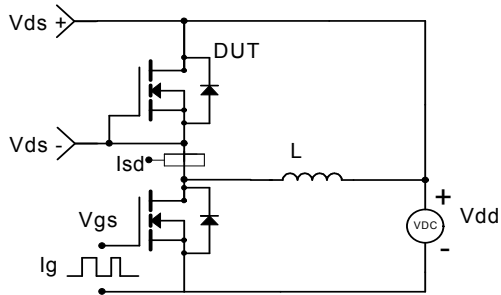
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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