AOCR36330

30V Common-Drain Dual N-Channel MOSFET

General Description

- Trench Power MOSFET technology
- Low $R_{SS(ON)}$
- Common drain configuration for design simplicity
- Advantage RigidCSP packge
- RoHS and Halogen-Free Compliant

Applications

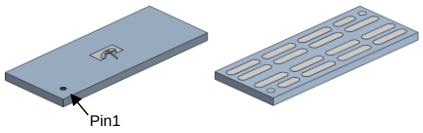
- Battery protection switch
- Mobile device battery charging and discharging

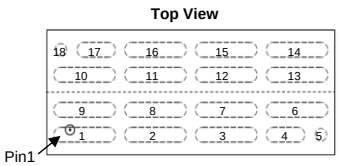
Product Summary

V_{SS}	30V
$R_{SS(ON)}$ (at V_{GS}=10V)	< 1.4mΩ
$R_{SS(ON)}$ (at V_{GS}=8V)	< 1.6mΩ
$R_{SS(ON)}$ (at V_{GS}=4.5V)	< 2.8mΩ

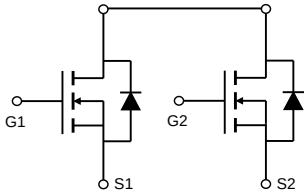
Green Product

RigidCSP™ 6.22x2.5_18





1~4,6~9. Source1(FET1) 5. Gate1 (FET1)
10~17. Source2(FET2) 18. Gate2 (FET2)



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOCR36330	RigidCSP™ 6.22x2.5_18	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Source-Source Voltage		V_{SS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Source Current(DC) Note1	T_A=25°C	I_S	40	A
Source Current(Pulse) Note2		I_{SM}	200	
Power Dissipation Note1	T_A=25°C	P_D	3.5	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typical	Units
Maximum Junction-to-Ambient	t ≤ 10s	$R_{\theta JA}$	25	°C/W
Maximum Junction-to-Ambient	Steady-State		35	°C/W

Note 1. I_S rated value is based on bare silicon.Mounted on 70mmx70mm FR-4 board.
Note 2. PW <10 µs pulses, duty cycle 1% max.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{SSS}	Source-Source Breakdown Voltage	I_S=250µA, V_{GS}=0V	Test Circuit 6	30			V
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}=30V, V_{GS}=0V	Test Circuit 1			1	µA
			T_J=55°C			5	
I_{GSS}	Gate leakage current	V_{SS}=0V, V_{GS}=±20V	Test Circuit 2			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{SS}=V_{GS}, I_S=250µA	Test Circuit 3	1	1.5	2	V
$R_{SS(ON)}$	Static Source to Source On-Resistance	V_{GS}=10V, I_S=6A	Test Circuit 4	0.7	1.05	1.4	mΩ
			T_J=125°C	1.0	1.5	2	
		V_{GS}=8V, I_S=6A	Test Circuit 4	0.8	1.2	1.6	mΩ
		V_{GS}=4.5V, I_S=6A	Test Circuit 4	1.3	1.95	2.8	mΩ
g_{FS}	Forward Transconductance	V_{SS}=5V, I_S=6A	Test Circuit 3		33		S
V_{FSS}	Forward Source to Source Voltage	I_S=1A,V_{GS}=0V	Test Circuit 5		0.66	1	V
DYNAMIC PARAMETERS							
R_g	Gate resistance	f=1MHz			1.4		Ω
SWITCHING PARAMETERS							
Q_g	Total Gate Charge	V_{G1S1}=10V, V_{SS}=15V, I_S=6A			128		nC
$t_{D(on)}$	Turn-On DelayTime	V_{G1S1}=10V, V_{SS}=15V, R_L=2.5Ω, R_{GEN}=3Ω	Test Circuit8		13.5		ns
t_r	Turn-On Rise Time				25		ns
$t_{D(off)}$	Turn-Off DelayTime				80		ns
t_f	Turn-Off Fall Time				65		ns

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

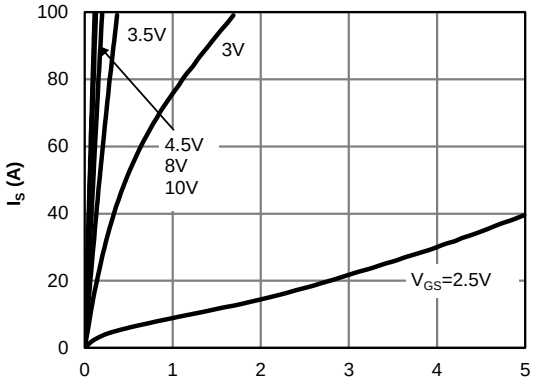


Figure 1: On-Region Characteristics

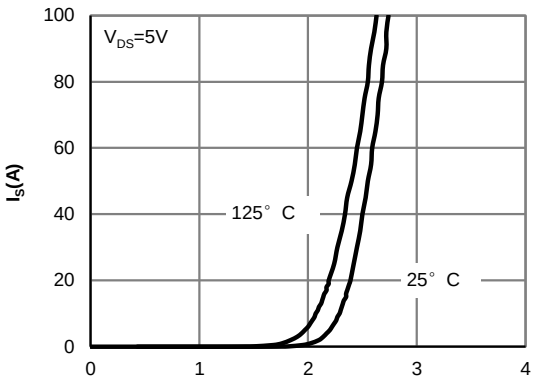


Figure 2: Transfer Characteristics

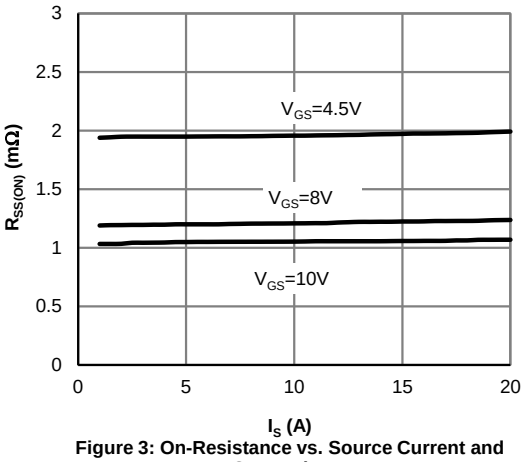


Figure 3: On-Resistance vs. Source Current and Gate Voltage

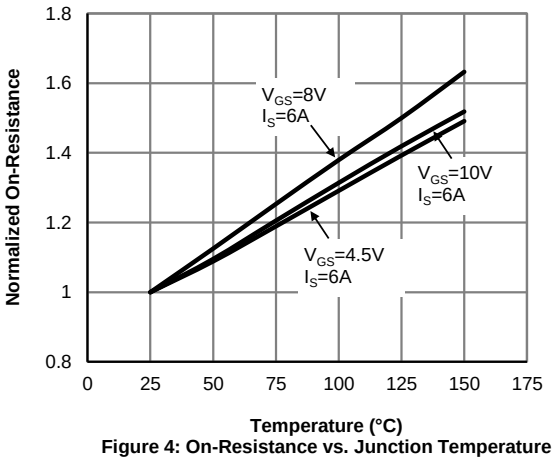


Figure 4: On-Resistance vs. Junction Temperature

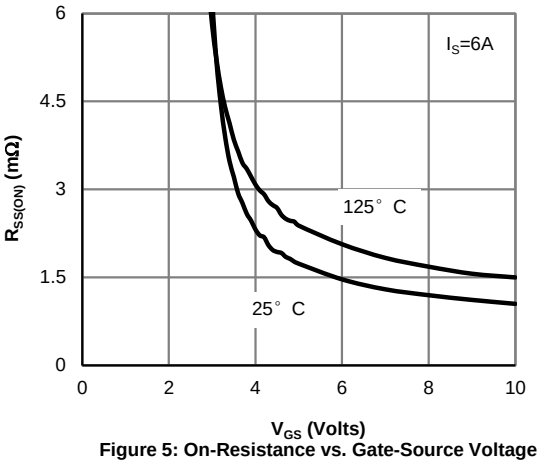


Figure 5: On-Resistance vs. Gate-Source Voltage

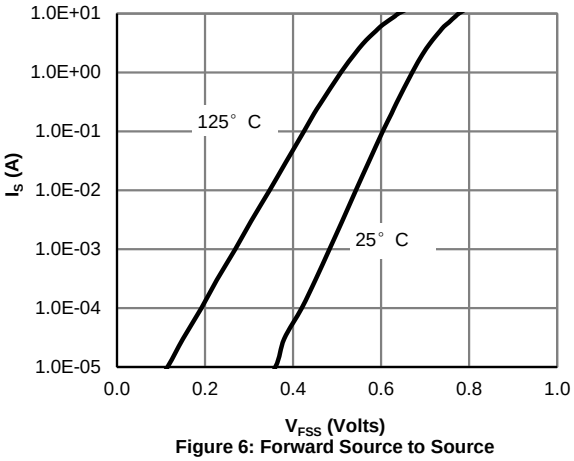


Figure 6: Forward Source to Source Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

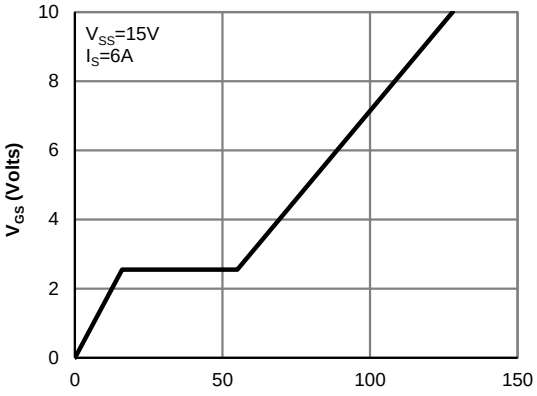


Figure 7: Gate-Charge Characteristics

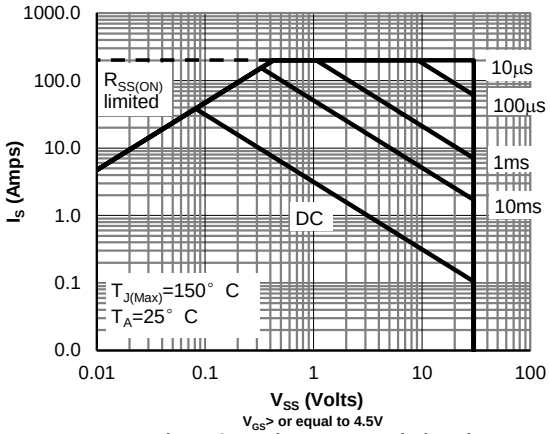


Figure 8: Maximum Forward Biased Safe Operating Area (Note1)

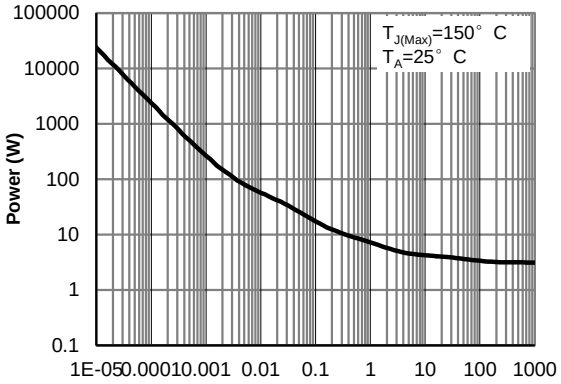


Figure 9: Single Pulse Power Rating Junction-to-Ambient (Note1)

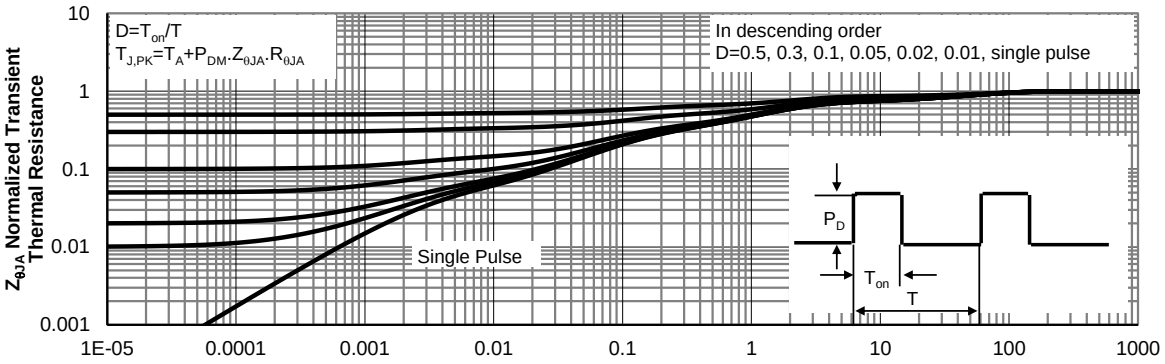
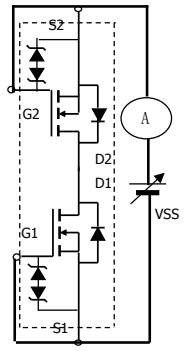


Figure 10: Normalized Maximum Transient Thermal Impedance (Note1)

TEST CIRCUIT 1 Isss

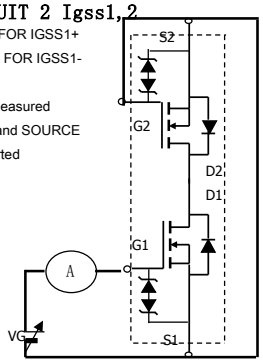
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 2 Igss1,2

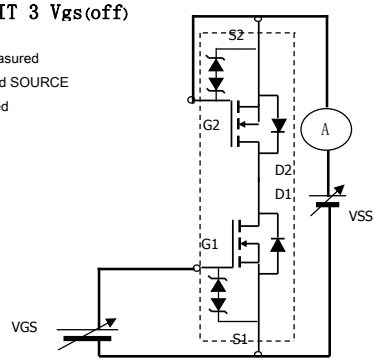
POSITIVE VGS FOR IGSS1+
NEGATIVE VGS FOR IGSS1-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



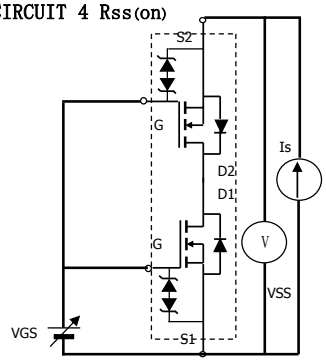
TEST CIRCUIT 3 Vgs(off)

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



TEST CIRCUIT 4 Rss(on)

Vss/Is

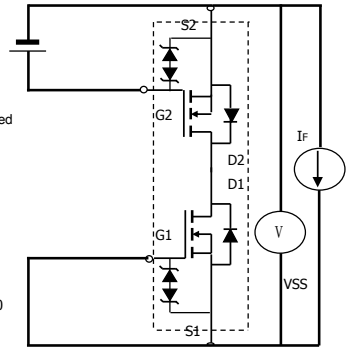


TEST CIRCUIT 5 $V_{F(SS)1,2}$

4.5V

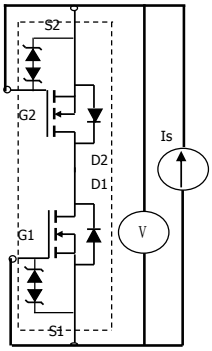
When FET1 measured
FET2 VGS=4.5V

VGS=0



TEST CIRCUIT 6 BV_{DSS}

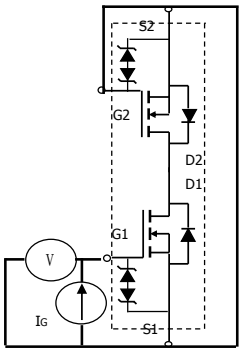
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



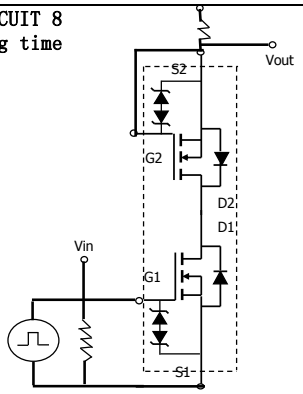
TEST CIRCUIT 7 $BV_{GSO1,2}$

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



TEST CIRCUIT 8 Switching time



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>>AOS(万代)