ALPHA & OMEGA SEMICONDUCTOR

AOD607
Complementary Enhancement Mode Field Effect Transistor

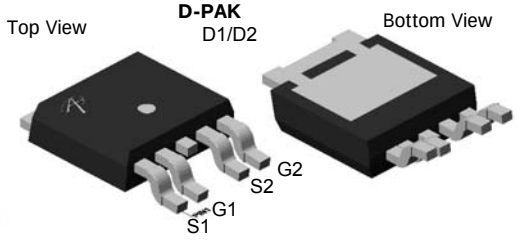
General Description
The AOD607 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

-RoHS Compliant
-Halogen Free*

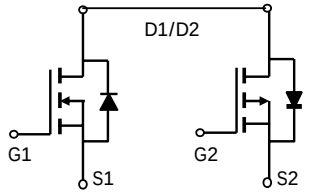
Features
n-channel	p-channel
V_{DS} (V) = 30V	-30V
I_D = 12A (V_{GS}=10V)	-12A (V_{GS} = -10V)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 25 mΩ (V_{GS}=10V)	< 37 mΩ (V_{GS} = -10V)
< 34 mΩ (V_{GS}=4.5V)	< 62 mΩ (V_{GS} = -4.5V)

100% UIS Tested!

TO-252-4L
D-PAK



Top View
Drain Connected
to Tab



n-channel **p-channel**

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	12	-12	A
	T_C=100°C		9.4	-9.4	
Pulsed Drain Current [C]		I_{DM}	40	-40	
Avalanche Current [C]		I_{AR}	18	-18	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	40	40	mJ
Power Dissipation [B]	T_C=25°C	P_D	25	25	W
	T_C=100°C		12.5	12.5	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.1	2.1	W
	T_A=70°C		1.3	1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	-55 to 175	°C

Thermal Characteristics: n-channel and p-channel

Parameter		Symbol	Device	Typ	Max	
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	n-ch	19	23	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		n-ch	47	60	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	n-ch	4.5	6	°C/W
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	p-ch	19	23	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		p-ch	47	60	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	p-ch	4.5	6	°C/W

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.5	1.7	2.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=12A		20	25	mΩ
		T_J=125°C		28	34	
		V_{GS}=4.5V, I_D=5A		27.5	34	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=12A		25		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				18	A
I_{SM}	Pulsed Body-Diode Current[C]				40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1040	1250	pF
C_{oss}	Output Capacitance			180		pF
C_{rss}	Reverse Transfer Capacitance			110		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.7	1.5	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=12A		19.8	25	nC
Q_g(4.5V)	Total Gate Charge			9.8	12.5	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			3.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.25Ω, R_{GEN}=3Ω		4.5		ns
t_r	Turn-On Rise Time			3.9		ns
$t_{D(off)}$	Turn-Off DelayTime			17.4		ns
t_f	Turn-Off Fall Time			3.2		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, dI/dt=100A/µs		19	25	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, dI/dt=100A/µs		8		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev3: Oct 2008

N-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

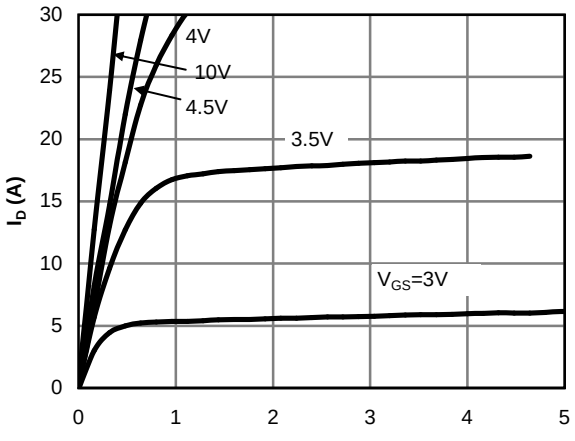


Fig 1: On-Region Characteristics

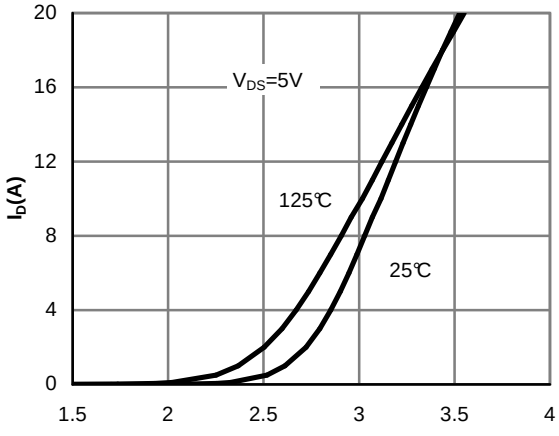


Figure 2: Transfer Characteristics

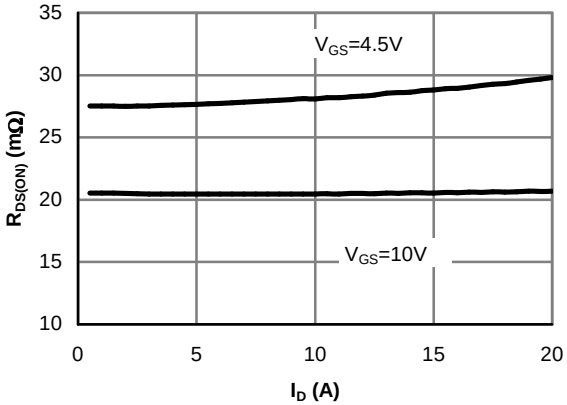


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

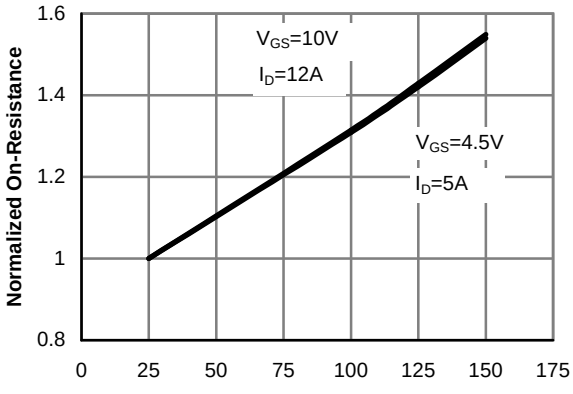


Figure 4: On-Resistance vs. Junction Temperature

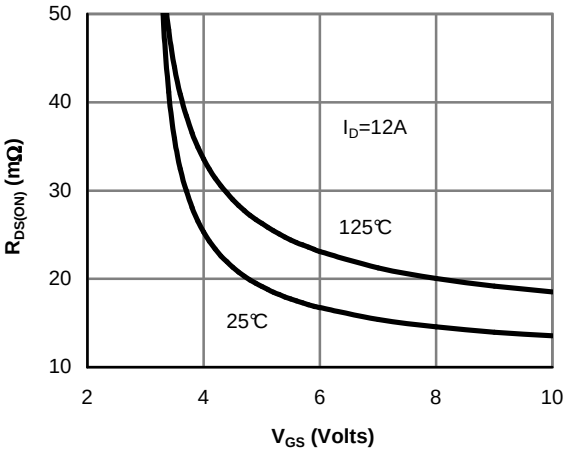


Figure 5: On-Resistance vs. Gate-Source Voltage

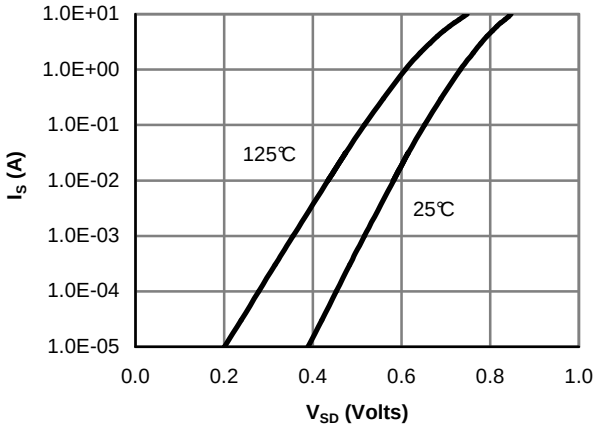


Figure 6: Body-Diode Characteristics

N-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

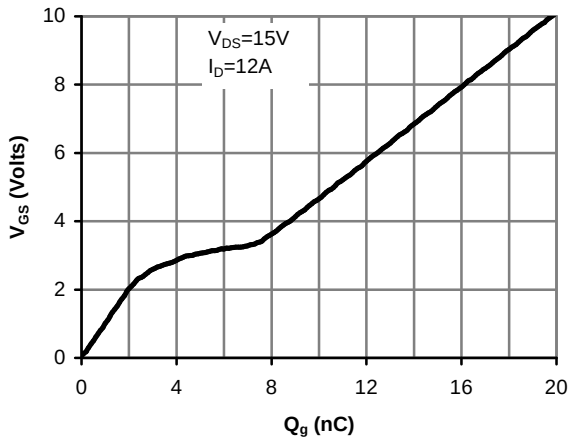


Figure 7: Gate-Charge Characteristics

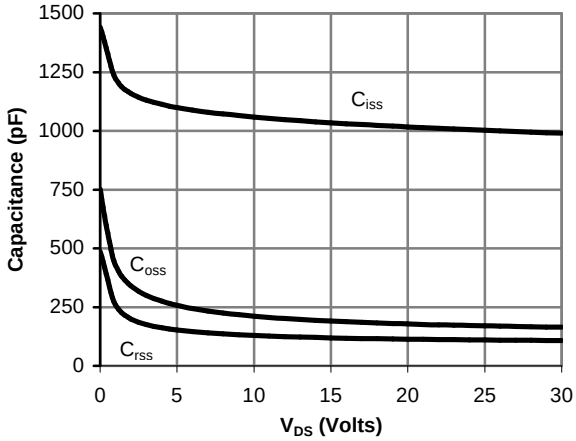


Figure 8: Capacitance Characteristics

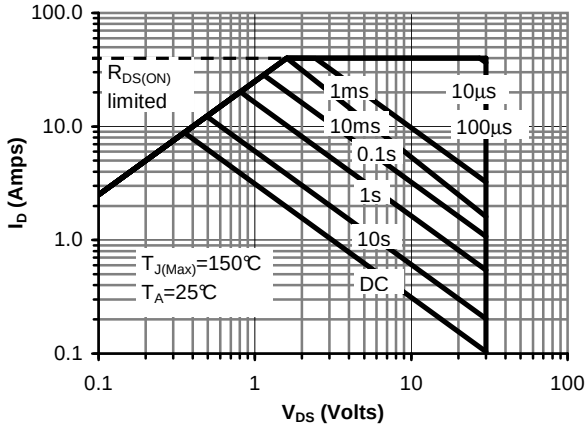


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

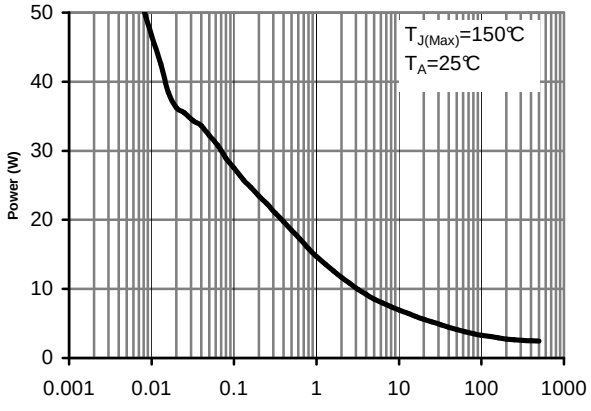


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

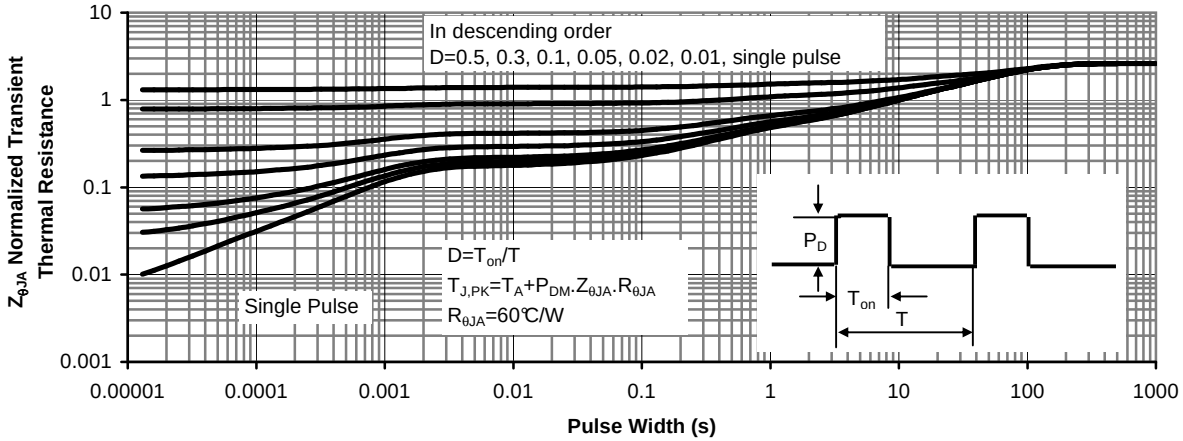


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V		-0.003	-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1.5	-2	-2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-12A		30	37	mΩ
		T_J=125°C		42	50	
		V_{GS}=-4.5V, I_D=-5A		50	62	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-12A		17		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.76	-1	V
I_S	Maximum Body-Diode Continuous Current				-18	A
I_{SM}	Pulsed Body-Diode Current[C]				-40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		920	1100	pF
C_{oss}	Output Capacitance			190		pF
C_{rss}	Reverse Transfer Capacitance			122		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		3.6	5	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge (10V)	V_{GS}=-10V, V_{DS}=-15V, I_D=-12A		18.7	23	nC
Q_g(4.5V)	Total Gate Charge (4.5V)			9.7	11.7	nC
Q_{gs}	Gate Source Charge			2.54		nC
Q_{gd}	Gate Drain Charge			5.4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=1.25Ω, R_{GEN}=3Ω		9	13	ns
t_r	Turn-On Rise Time			25	35	ns
$t_{D(off)}$	Turn-Off DelayTime			20	30	ns
t_f	Turn-Off Fall Time			12	18	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-12A, dI/dt=100A/µs		21.4	26	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-12A, dI/dt=100A/µs		13	16	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on steady-state $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature fo 175°C may be u sed if the PCB or heatsink allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by the package current capability.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev3: Oct. 2008

P-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

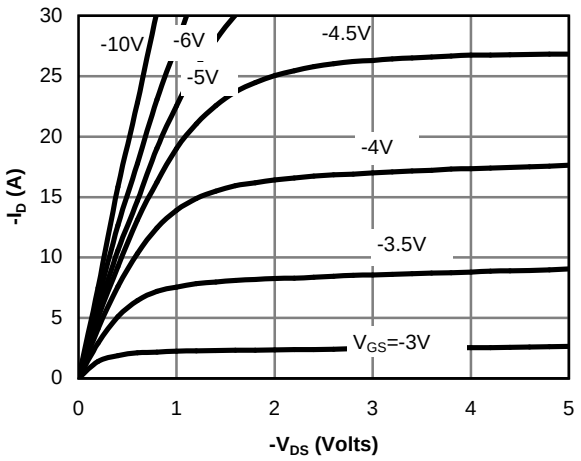


Fig 1: On-Region Characteristics

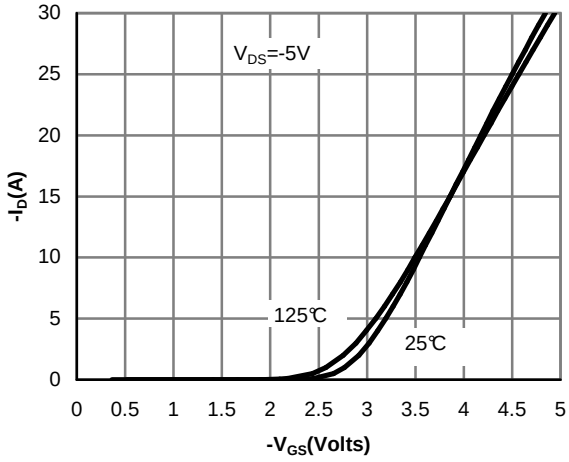


Figure 2: Transfer Characteristics

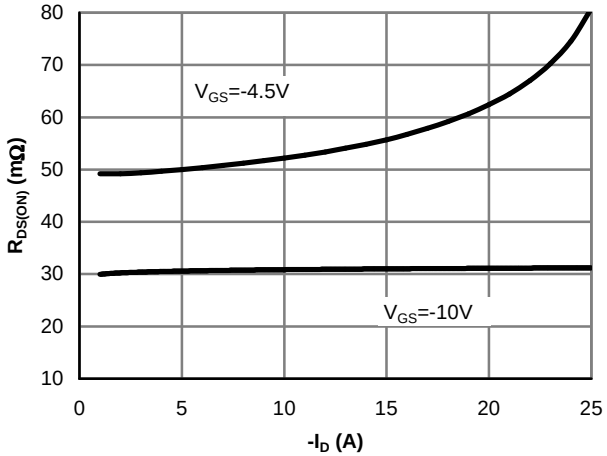


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

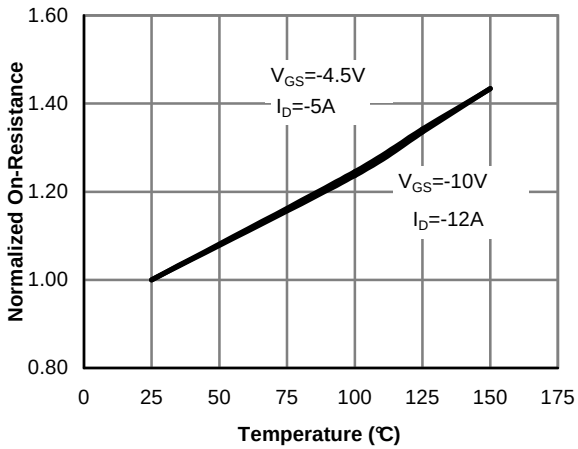


Figure 4: On-Resistance vs. Junction Temperature

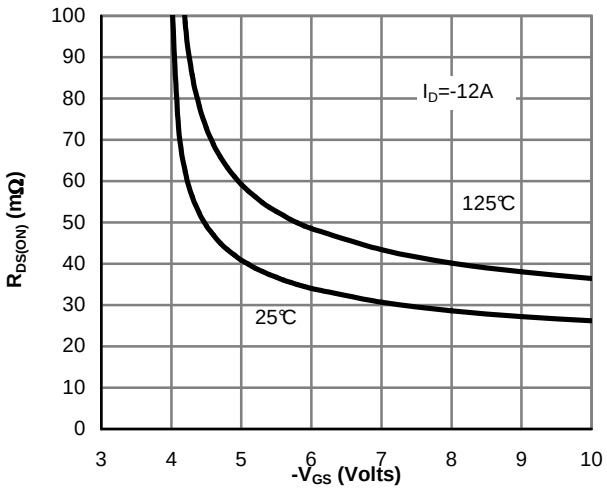


Figure 5: On-Resistance vs. Gate-Source Voltage

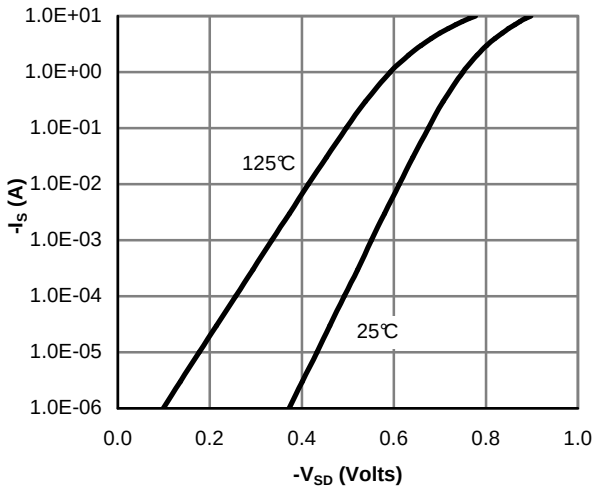


Figure 6: Body-Diode Characteristics

P-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

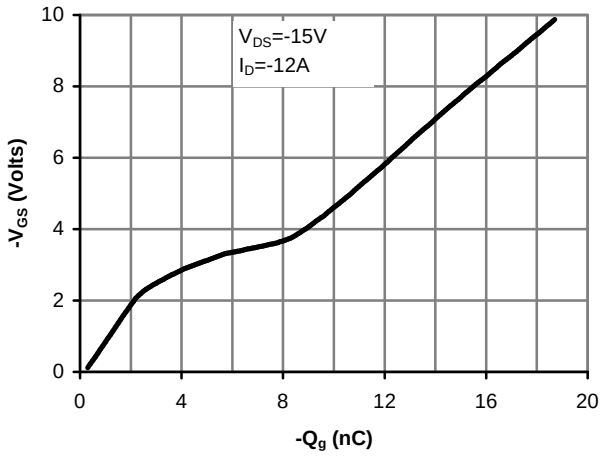


Figure 7: Gate-Charge Characteristics

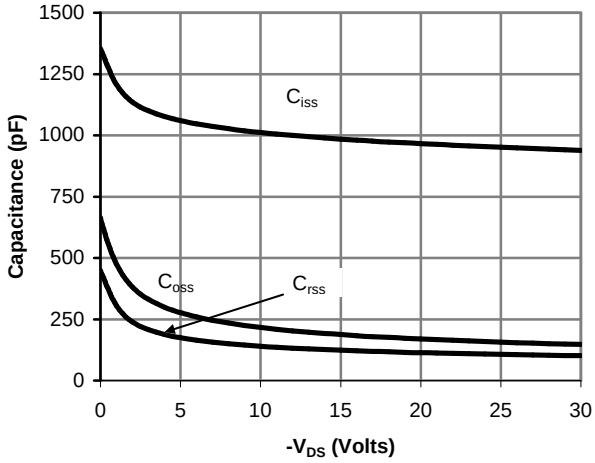


Figure 8: Capacitance Characteristics

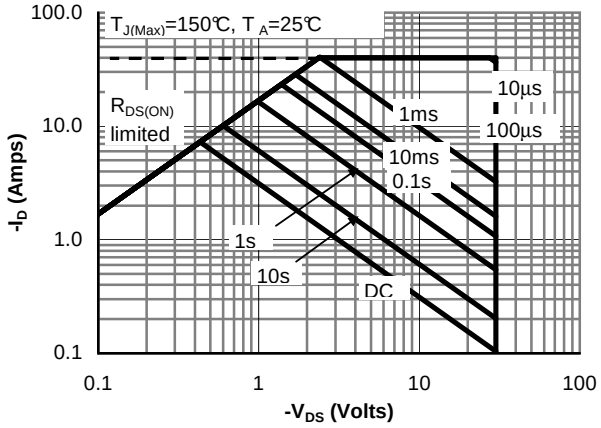


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

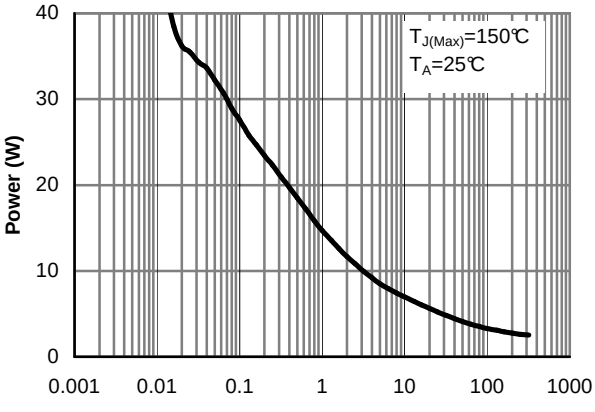


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

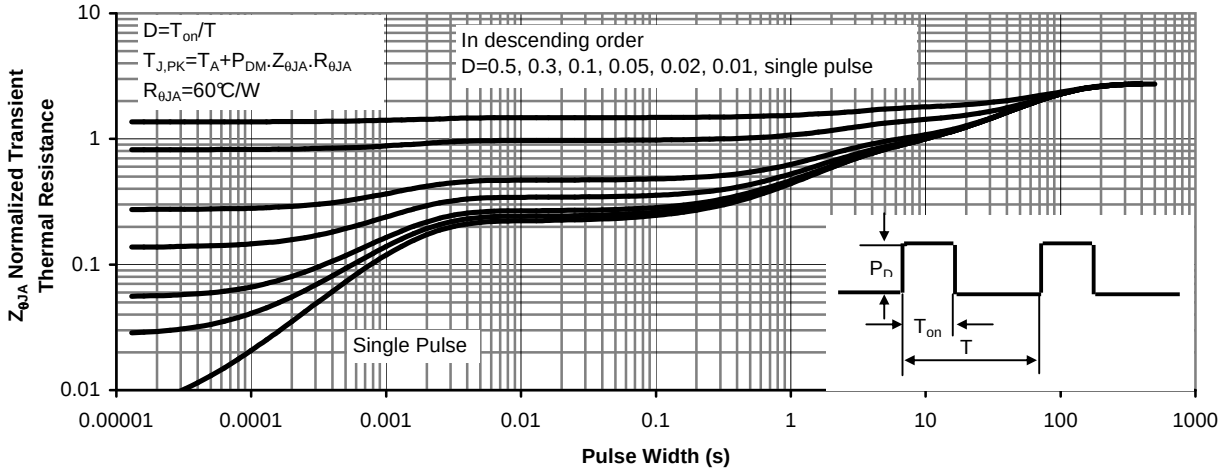
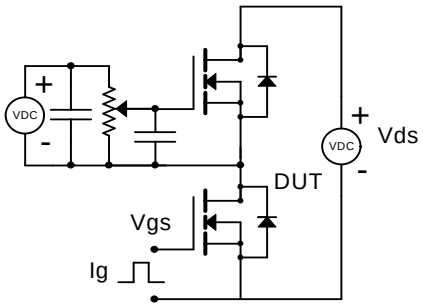
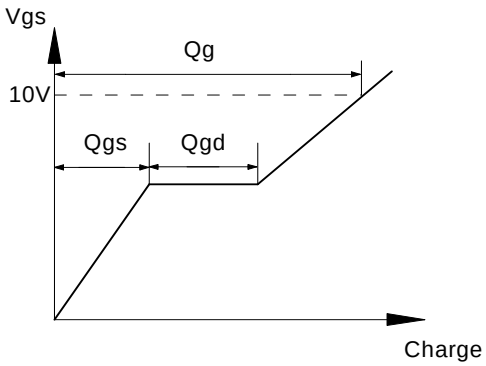


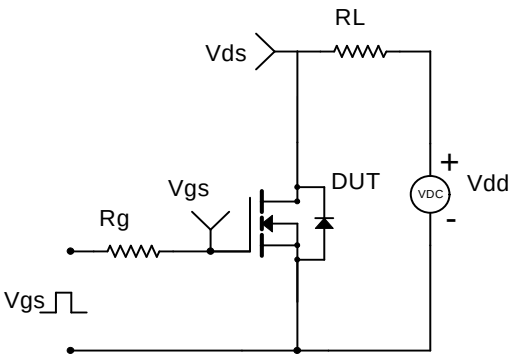
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

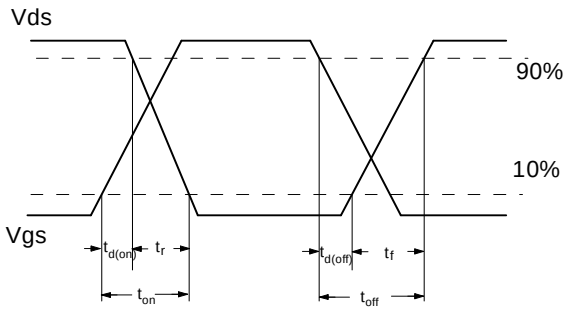
Gate Charge Test Circuit & Waveform



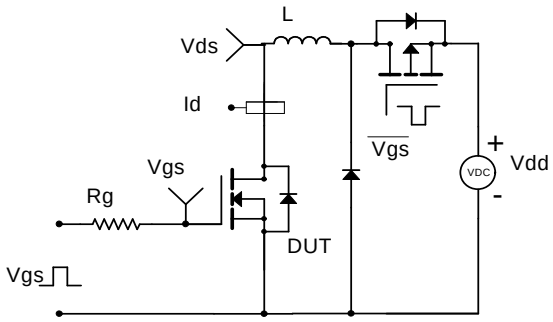


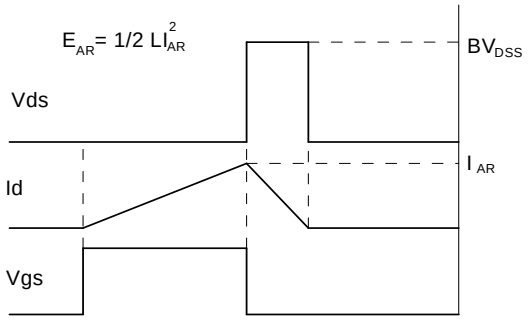
Resistive Switching Test Circuit & Waveforms



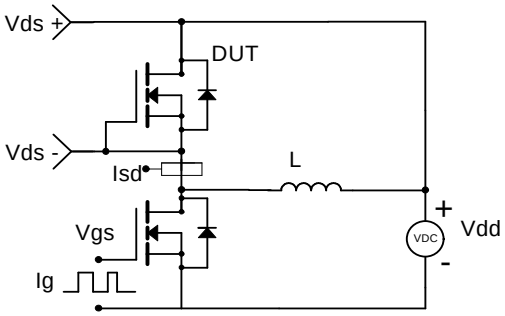


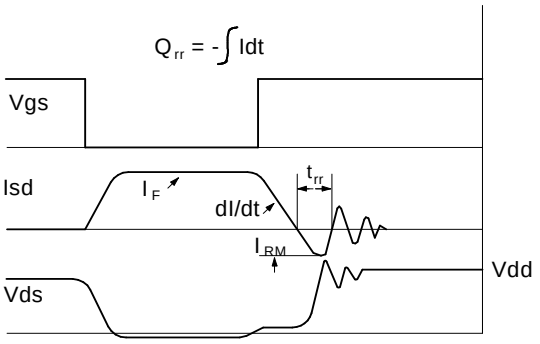
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



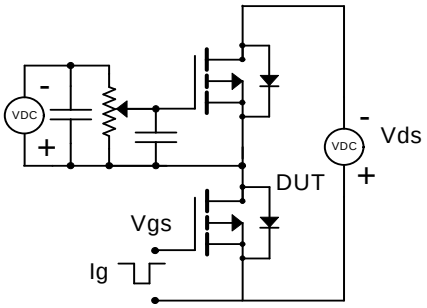


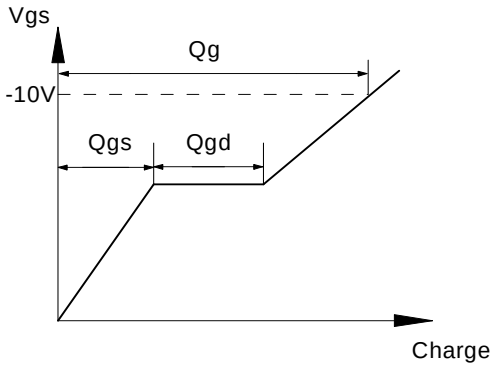
Diode Recovery Test Circuit & Waveforms



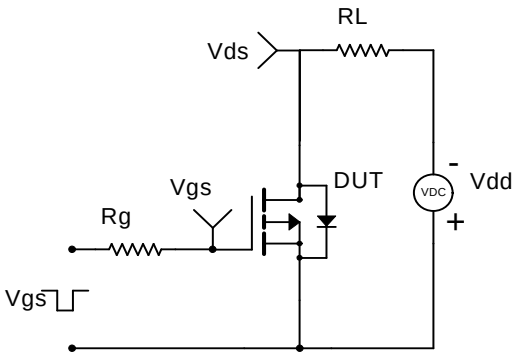


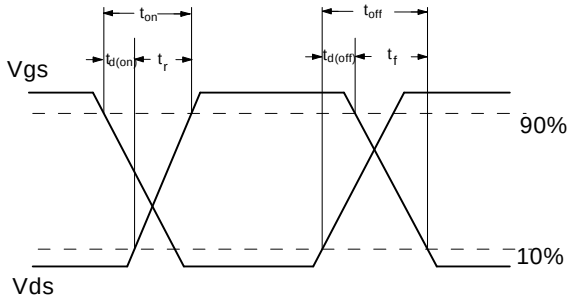
Gate Charge Test Circuit & Waveform



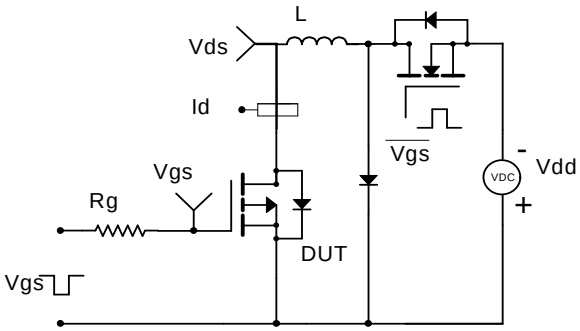


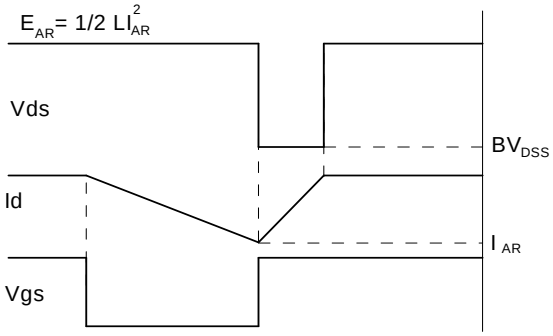
Resistive Switching Test Circuit & Waveforms



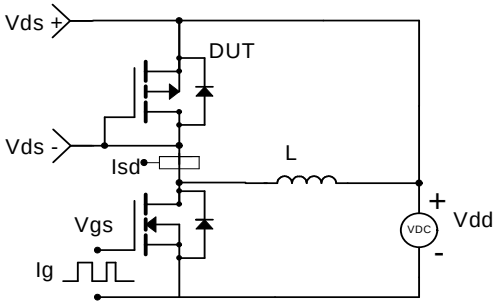


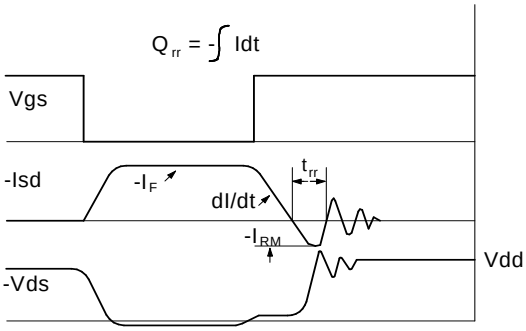
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





单击下面可查看定价，库存，交付和生命周期等信息

>>AOS(万代)