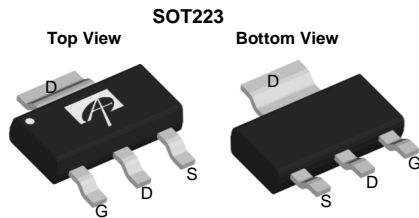


General Description

The AOH3110 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

Product Summary

V_{DS}	100V
I_D (at $V_{GS}=10V$)	1.0A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 700m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 820m Ω



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	4	A
Avalanche Current ^C	I_{AS}	3.5	A
Avalanche energy $L=50\mu\text{H}$ ^C	E_{AS}	0.3	mJ
Power Dissipation ^B	P_D	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	33	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}				
Maximum Junction-to-Lead	$R_{\theta JL}$	30	40	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.7	2.3	2.9	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	4			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =0.9A T _J =125°C		585	700	mΩ
		V _{GS} =4.5V, I _D =0.75A		635	820	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =0.9A		2.8		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.9	1.2	V
I _S	Maximum Body-Diode Continuous Current ^G				1	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, f=1MHz		100		pF
C _{oss}	Output Capacitance			13		pF
C _{riss}	Reverse Transfer Capacitance			5		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	2.5	5	7.5	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =50V, I _D =0.9A		2.8	6	nC
Q _{g(4.5V)}	Total Gate Charge			1.5	3	nC
Q _{gs}	Gate Source Charge			0.4		nC
Q _{gd}	Gate Drain Charge			0.8		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =50V, R _L =50Ω, R _{GEN} =3Ω		5		ns
t _r	Turn-On Rise Time			4		ns
t _{D(off)}	Turn-Off DelayTime			12		ns
t _f	Turn-Off Fall Time			5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =5.6A, di/dt=100A/μs		52		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =5.6A, di/dt=100A/μs		60		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating. G. The maximum current rating is package limited.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

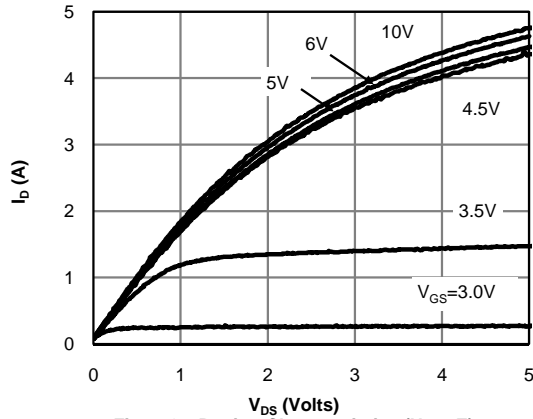


Figure 1: On-Region Characteristics (Note E)

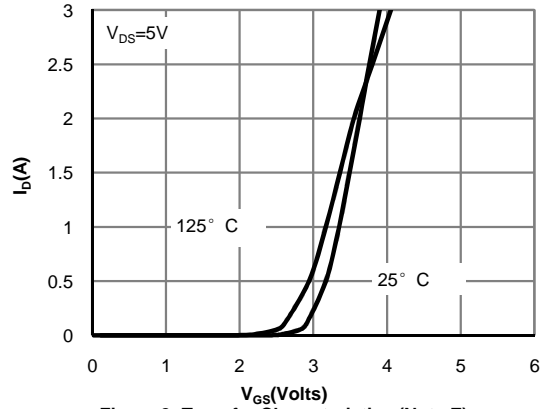


Figure 2: Transfer Characteristics (Note E)

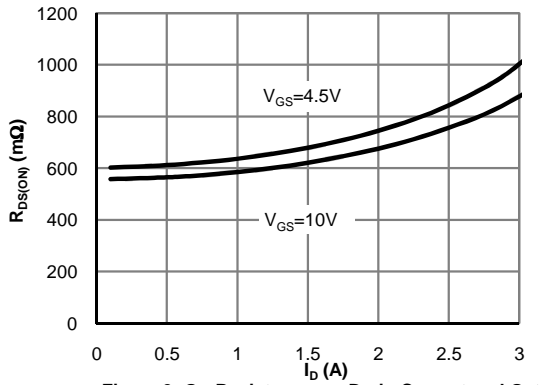


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

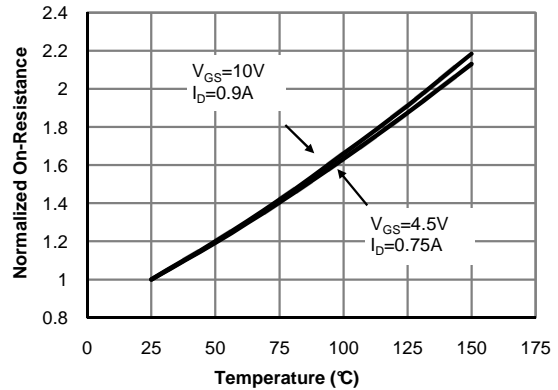


Figure 4: On-Resistance vs. Junction Temperature (Note E)

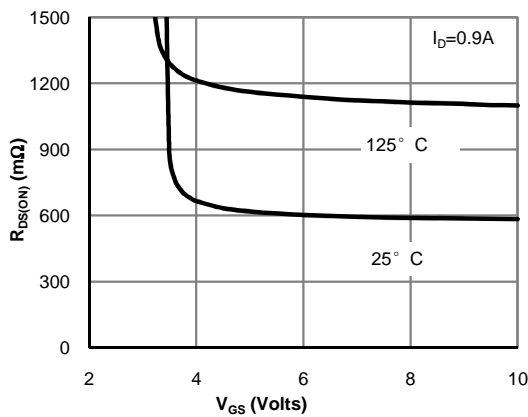


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

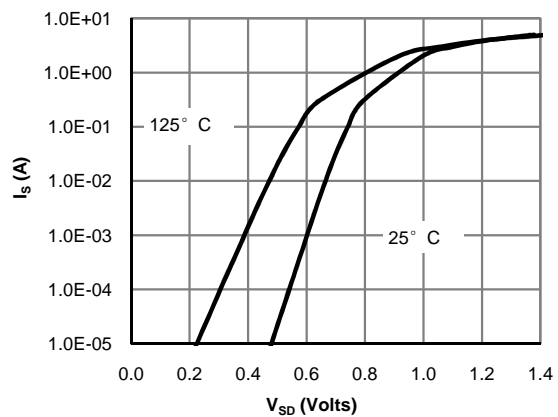


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

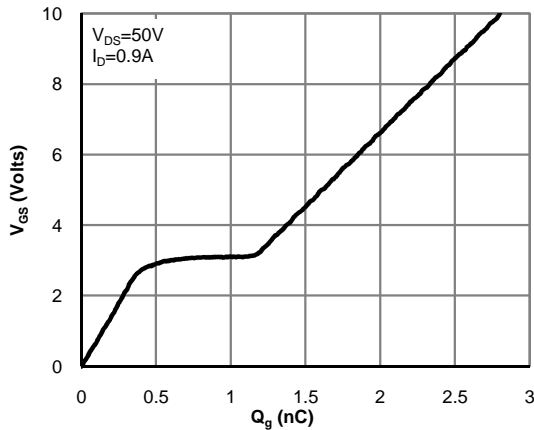


Figure 7: Gate-Charge Characteristics

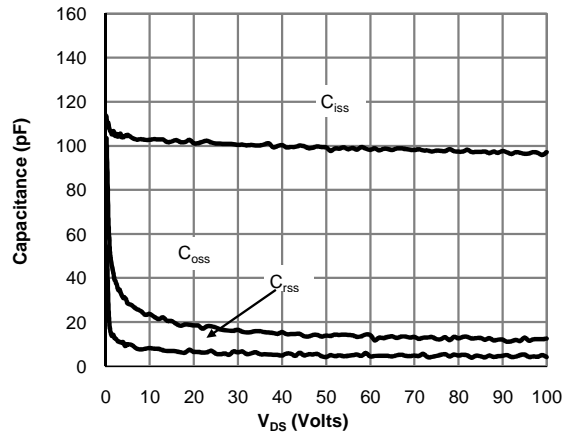


Figure 8: Capacitance Characteristics

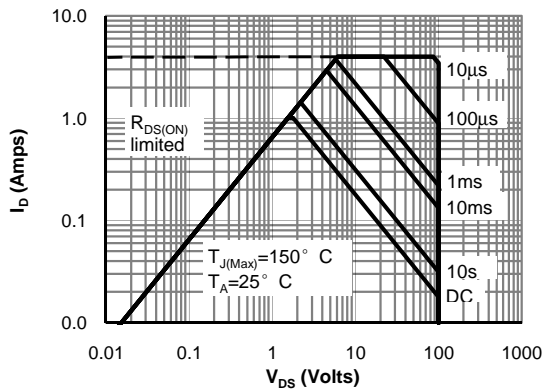


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

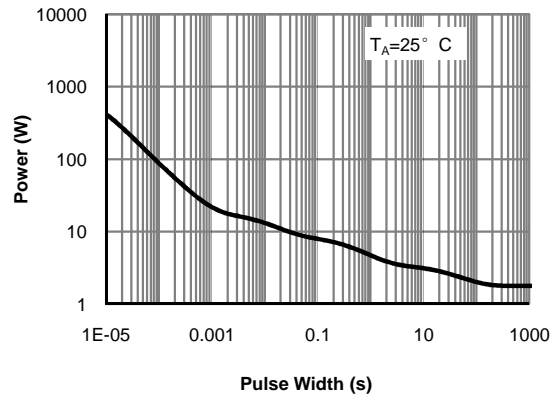


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

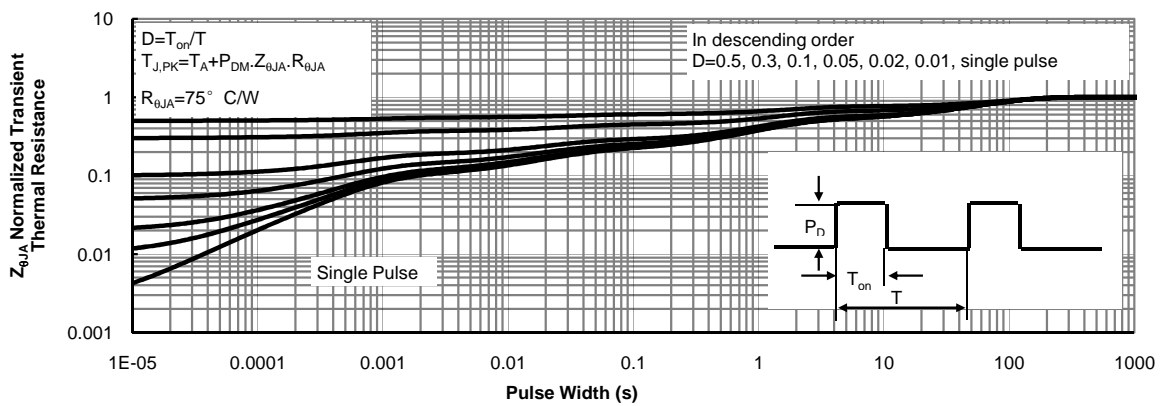
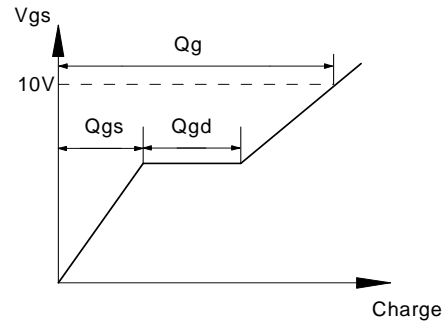
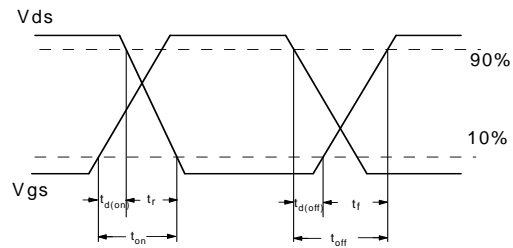
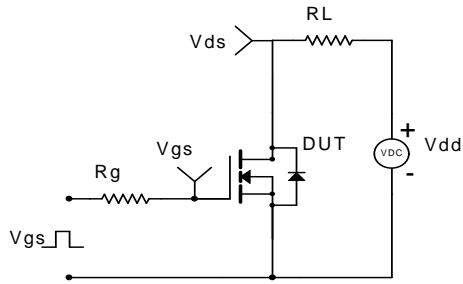


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

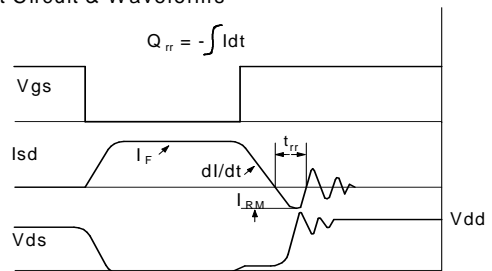
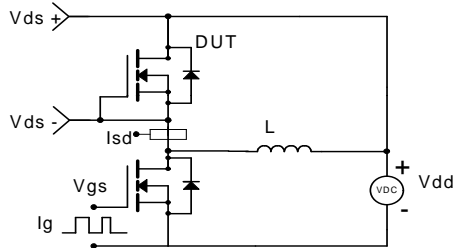
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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