

AOL1454
N-Channel Enhancement Mode Field Effect Transistor
General Description

The AOL1454 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It is ESD protected. This device is suitable for use as a low side switch in SMPS and general purpose applications.

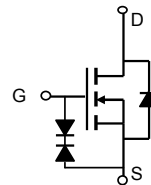
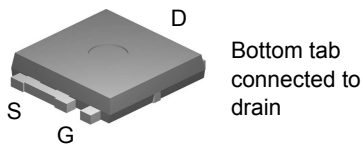
- RoHS Compliant
- Halogen and Antimony Free Green Device*

Features

V_{DS} (V) = 40V
 I_D = 50A (V_{GS} = 10V)
 $R_{DS(ON)} < 9m\Omega$ (V_{GS} = 10V)
 $R_{DS(ON)} < 13m\Omega$ (V_{GS} = 4.5V)

ESD Protected
 UIS Tested
 Rg,Ciss,Coss,Crss Tested

Ultra SO-8™ Top View


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^B	I_D	$T_C=25^\circ\text{C}$ ^H	50
		$T_C=100^\circ\text{C}$	48
Pulsed Drain Current ^C	I_{DM}	100	A
Continuous Drain Current ^A	I_{DSM}	$T_A=25^\circ\text{C}$	12
		$T_A=70^\circ\text{C}$	10
Avalanche Current ^C	I_{AR}	30	A
Repetitive avalanche energy $L=0.3\text{mH}$ ^C	E_{AR}	135	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	60
		$T_C=100^\circ\text{C}$	30
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	2.1
		$T_A=70^\circ\text{C}$	1.3
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	50	$^\circ\text{C/W}$
Maximum Junction-to-Case ^D	$R_{\theta JC}$	1.8	2.5	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1	2	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	100			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		7.5 10	9.0	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		47		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				50	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz		1600	1920	pF
C _{oss}	Output Capacitance			320		pF
C _{rss}	Reverse Transfer Capacitance			100		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		3.4		Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A		22		nC
Q _g (4.5V)	Total Gate Charge			10.5		nC
Q _{gs}	Gate Source Charge			4.2		nC
Q _{gd}	Gate Drain Charge			4.8		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =1Ω, R _{GEN} =3Ω		6.5		ns
t _r	Turn-On Rise Time			12.5		ns
t _{D(off)}	Turn-Off DelayTime			33		ns
t _f	Turn-Off Fall Time			16		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=100A/μs		31		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=100A/μs		33		nC

A: The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C. The power dissipation P_{DSM} and current rating I_{DSM} are based on T_{J(MAX)}=150°C, using steady state junction-to-ambient thermal resistance.

B. The power dissipation PD is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

H. The maximum current rating is limited by bond-wires.

* This device is guaranteed green after date code 8P11 (June 1ST 2008)

Rev1: June 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

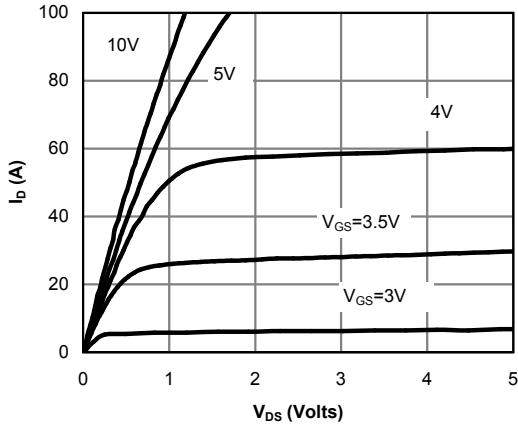


Figure 1: On-Region Characteristics

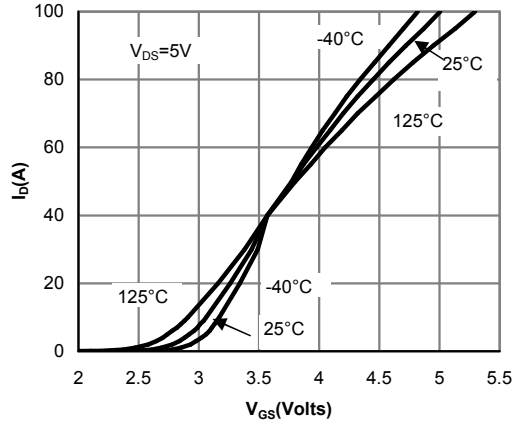


Figure 2: Transfer Characteristics

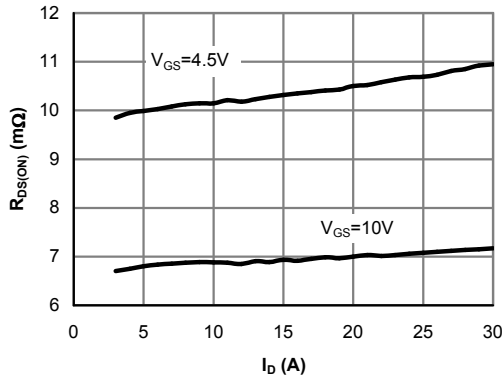


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

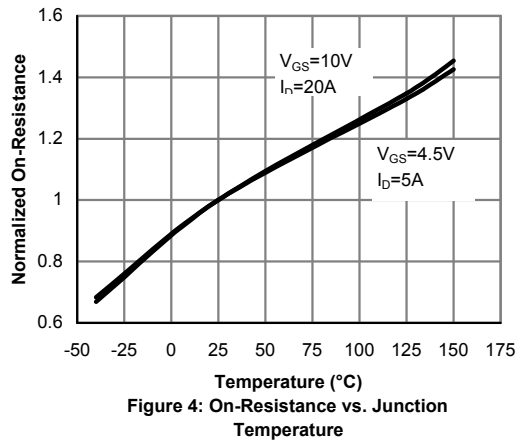


Figure 4: On-Resistance vs. Junction Temperature

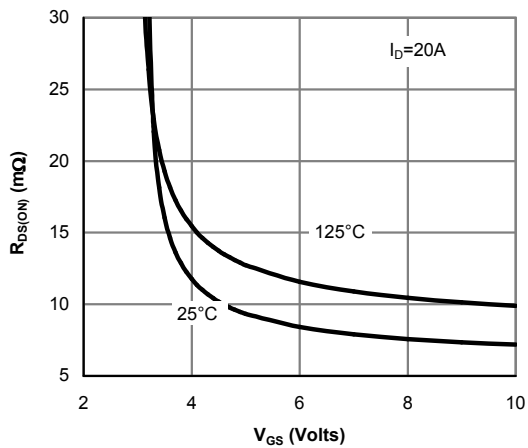


Figure 5: On-Resistance vs. Gate-Source Voltage

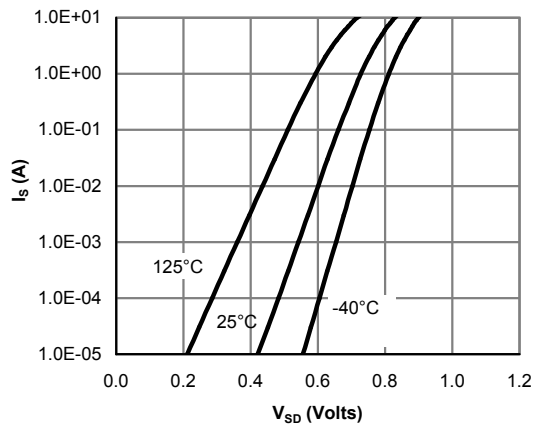


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

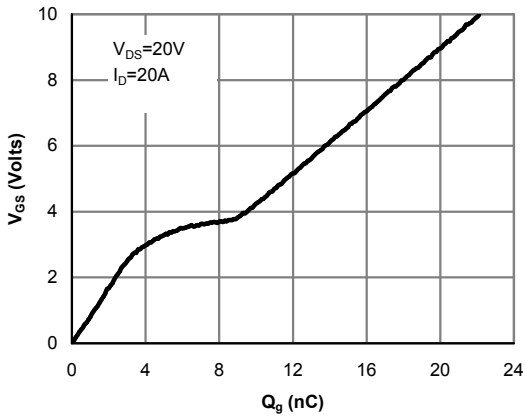


Figure 7: Gate-Charge Characteristics

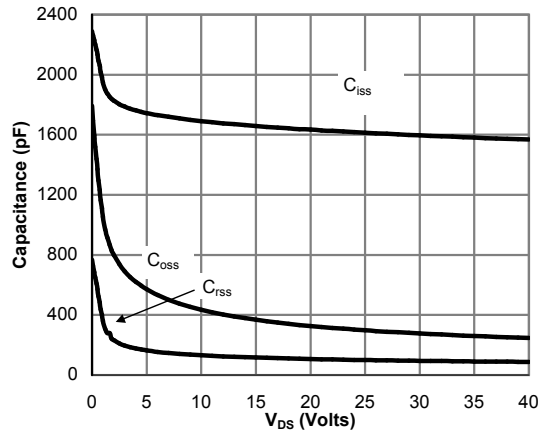


Figure 8: Capacitance Characteristics

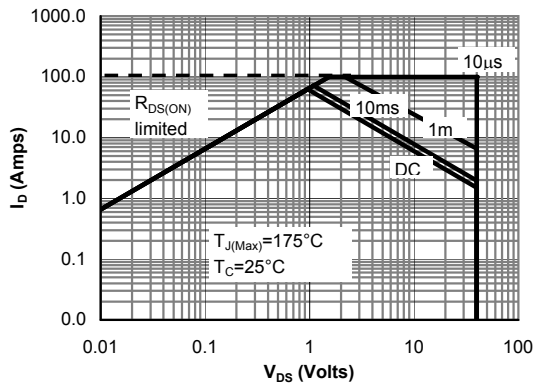


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

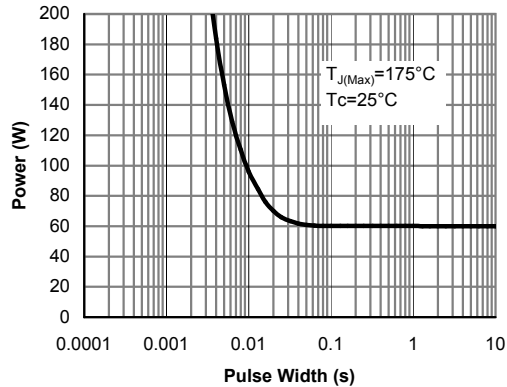


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

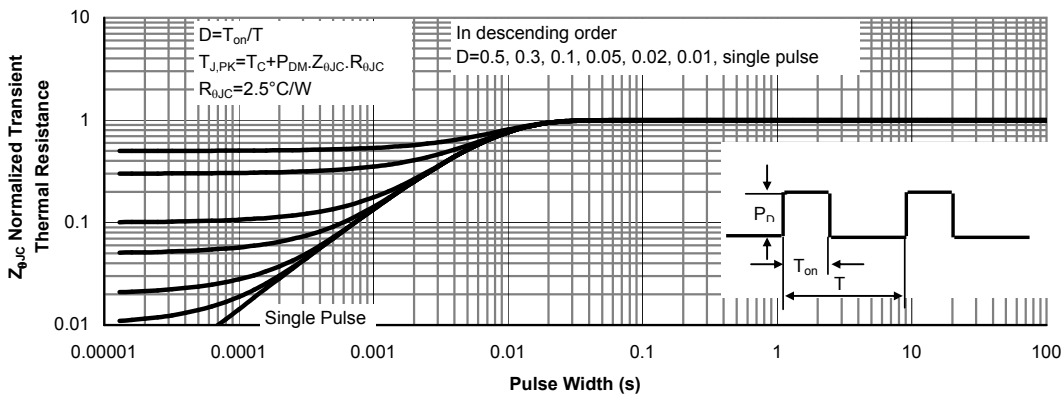


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

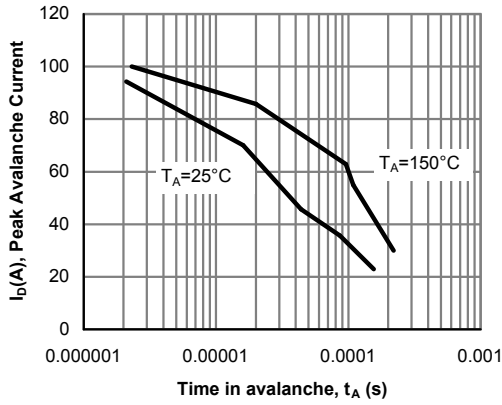


Figure 12: Single Pulse Avalanche capability

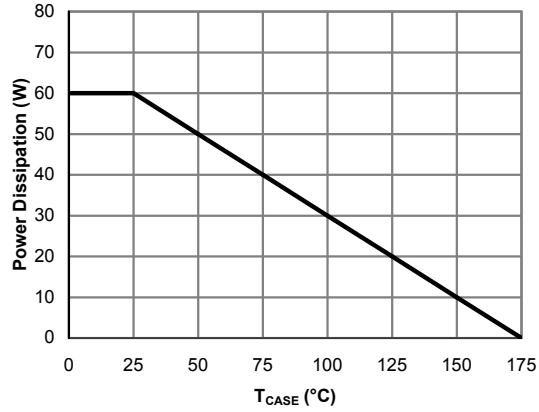


Figure 13: Power De-rating (Note B)

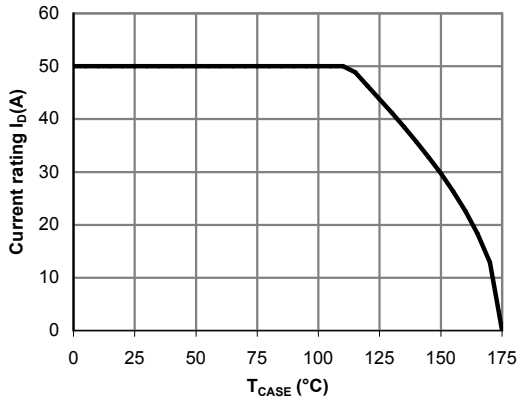


Figure 14: Current De-rating (Note B)

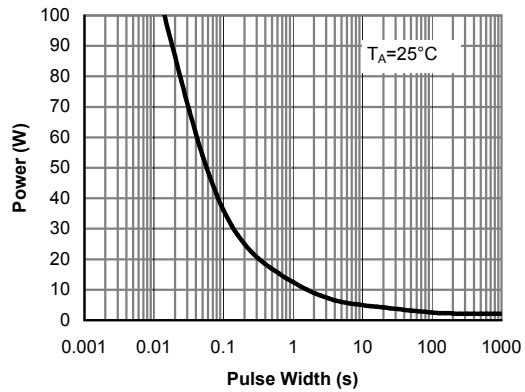


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

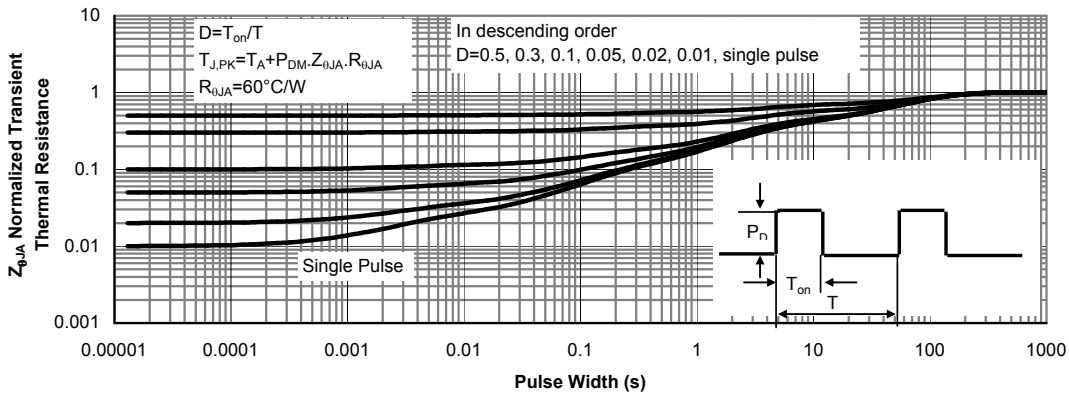
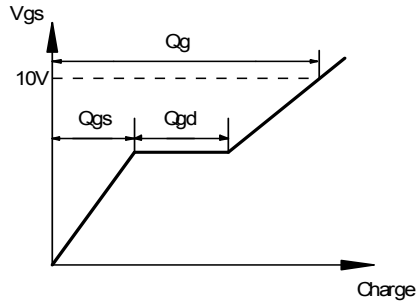
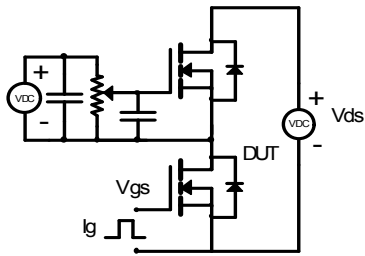
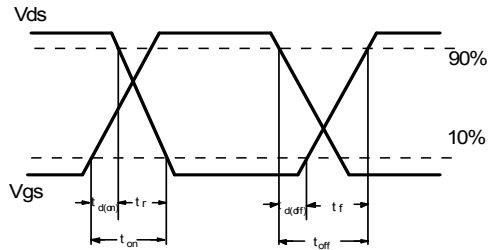
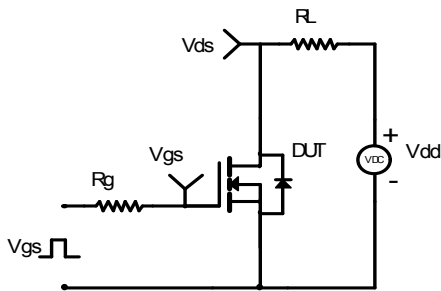


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

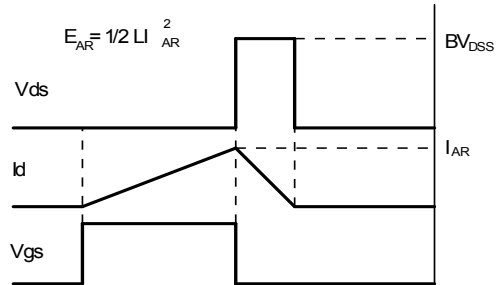
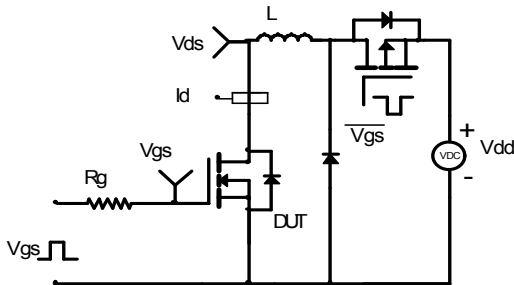
Gate Charge Test Circuit & Waveform



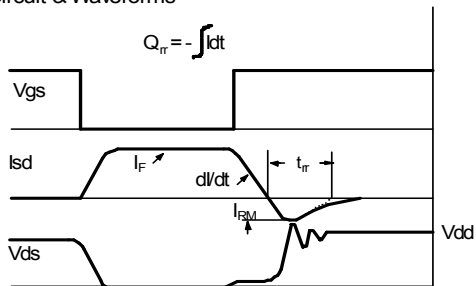
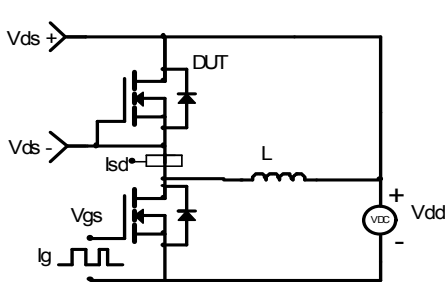
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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