

AON4805L

Dual P-Channel Enhancement Mode Field Effect Transistor

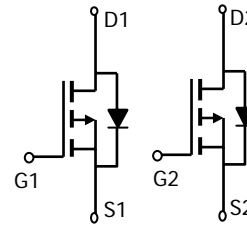
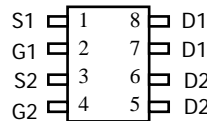
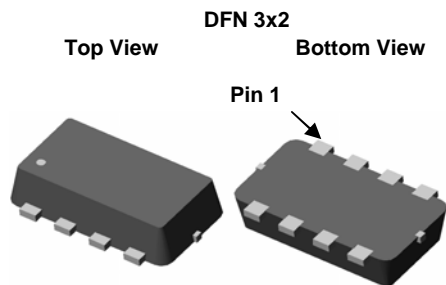
General Description

The AON4805L uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.

- RoHS Compliant
- Halogen Free

Features

- V_{DS} (V) = -20V
- I_D = -4.5A (V_{GS} = -4.5V)
- $R_{DS(ON)} < 65m\Omega$ (V_{GS} = -4.5V)
- $R_{DS(ON)} < 85m\Omega$ (V_{GS} = -2.5V)
- $R_{DS(ON)} < 115m\Omega$ (V_{GS} = -1.8V)



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	MOSFET	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	-4.5
		$T_A=70^\circ\text{C}$	-3.5
Pulsed Drain Current ^C	I_{DM}	-25	A
Power Dissipation ^B	P_D	$T_A=25^\circ\text{C}$	2
		$T_A=70^\circ\text{C}$	1.3
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	50	60	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{AD}		Steady-State	84	100
Maximum Junction-to-Lead	$R_{\theta JL}$	28	34	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±8V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.5	-0.67	-1	V
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-25			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-4.5A T _J =125°C		53 72	65 90	mΩ
		V _{GS} =-2.5V, I _D =-3A		66	85	mΩ
		V _{GS} =-1.8V, I _D =-2A		88	115	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-4.5A		15		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1	V
I _S	Maximum Body-Diode Continuous Current				-1.7	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =-10V, f=1MHz		560	670	pF
C _{OSS}	Output Capacitance			80		pF
C _{ISS}	Reverse Transfer Capacitance			70		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		15	23	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-4.5A		8.5	10	nC
Q _{gs}	Gate Source Charge			1.2		nC
Q _{gd}	Gate Drain Charge			2.1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-4.5V, V _{DS} =-10V, R _L =2.2Ω, R _{GEN} =6Ω		7.2		ns
t _r	Turn-On Rise Time			36		ns
t _{D(off)}	Turn-Off DelayTime			53		ns
t _f	Turn-Off Fall Time			56		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-4.5A, dI/dt=100A/μs		37	45	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-4.5A, dI/dt=100A/μs		27		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B: The power dissipation P_D is based on T_{J(MAX)}=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C: Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

Rev0 : July 2008

COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

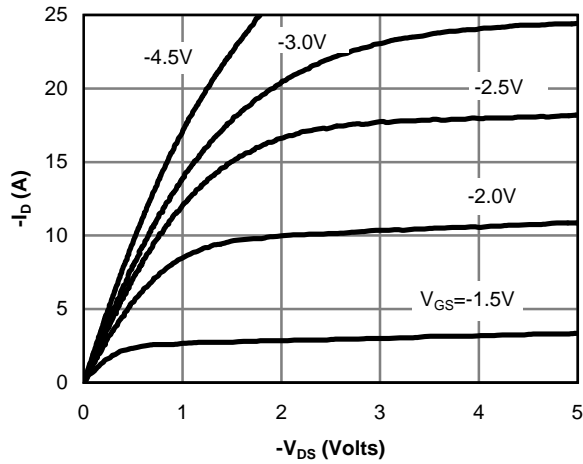


Figure 1: On-Region Characteristics(Note E)

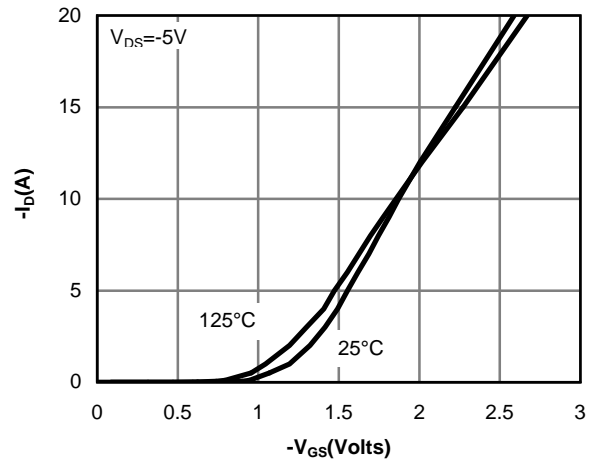


Figure 2: Transfer Characteristics(Note E)

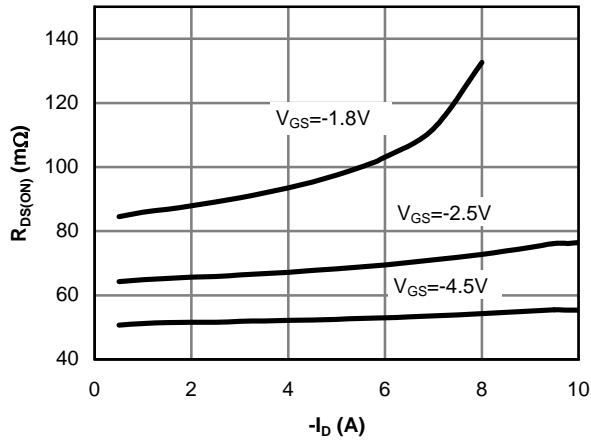


Figure 3: On-Resistance vs. Drain Current and Gate Voltage(Note E)

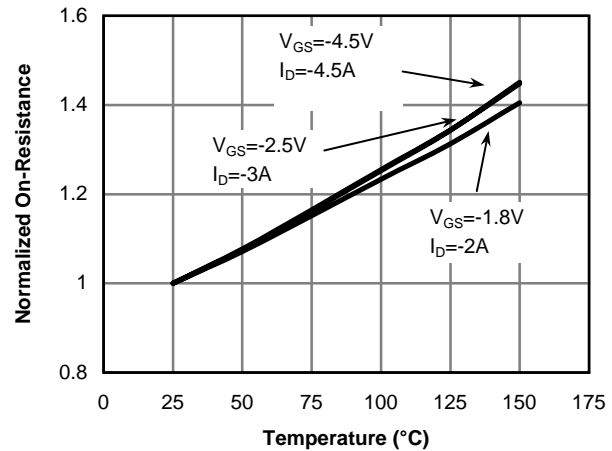


Figure 4: On-Resistance vs. Junction Temperature(Note E)

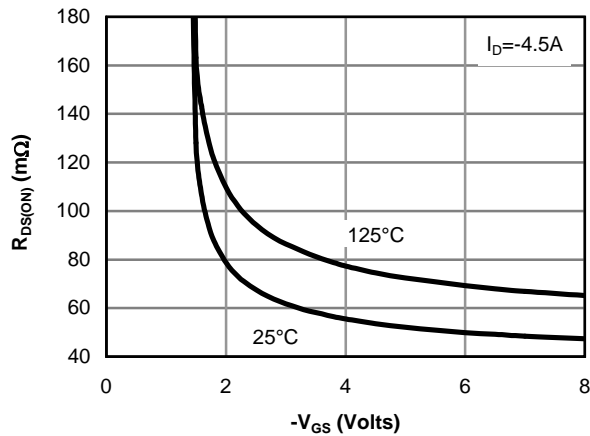


Figure 5: On-Resistance vs. Gate-Source Voltage(Note E)

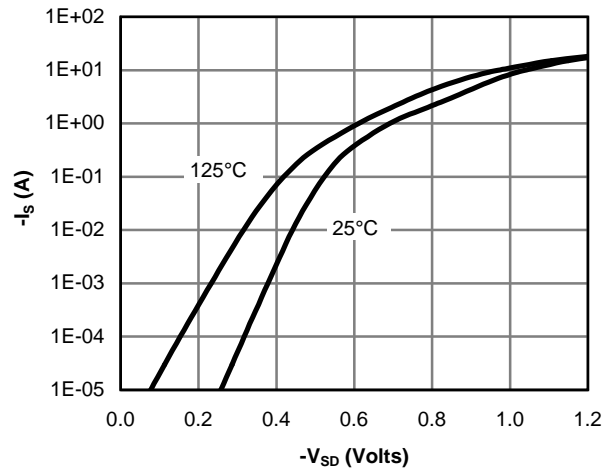


Figure 6: Body-Diode Characteristics(Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

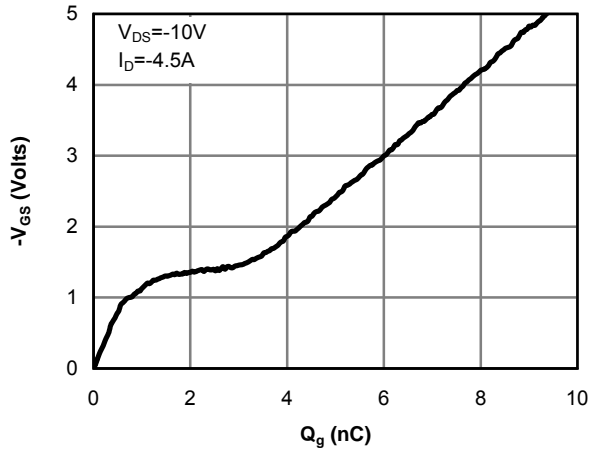


Figure 7: Gate-Charge Characteristics

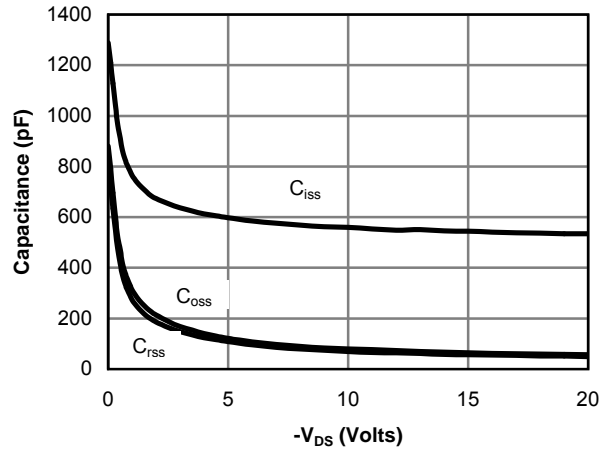


Figure 8: Capacitance Characteristics

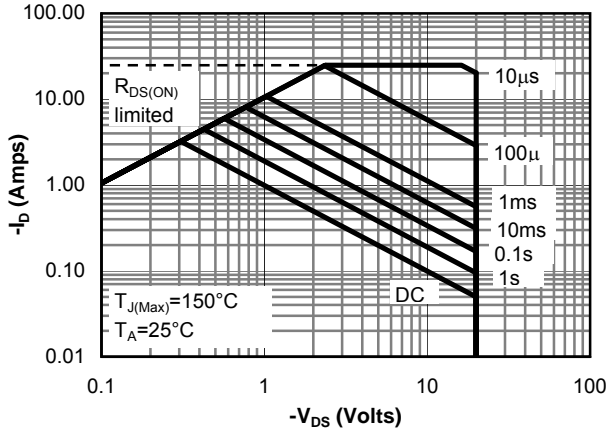


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

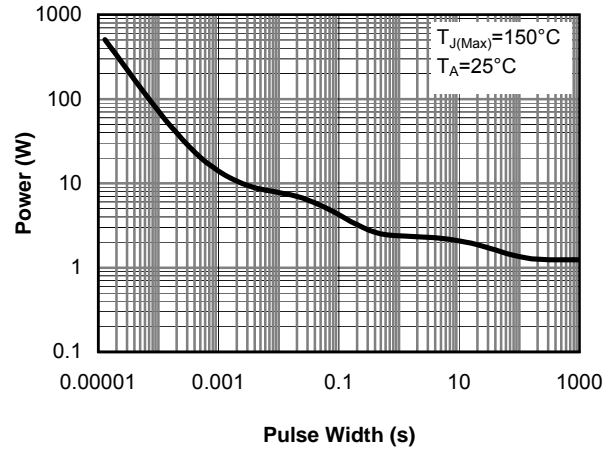


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

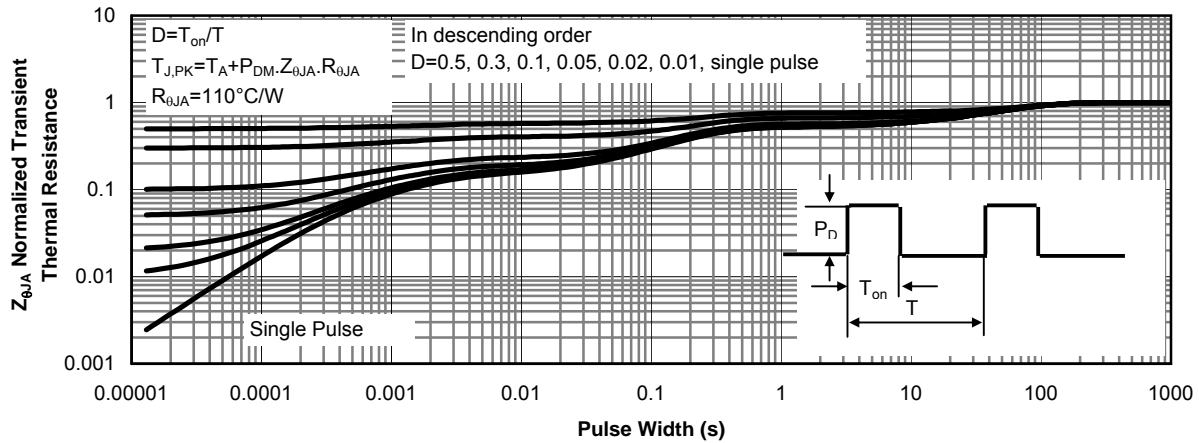
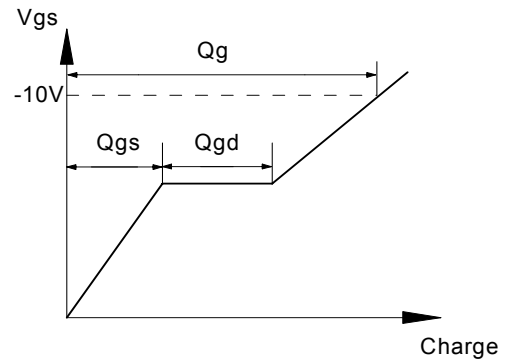
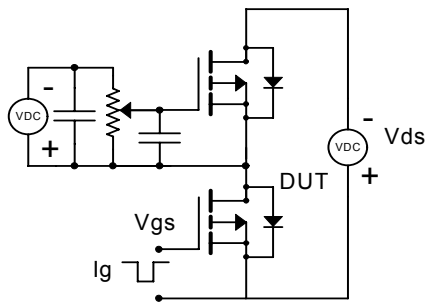
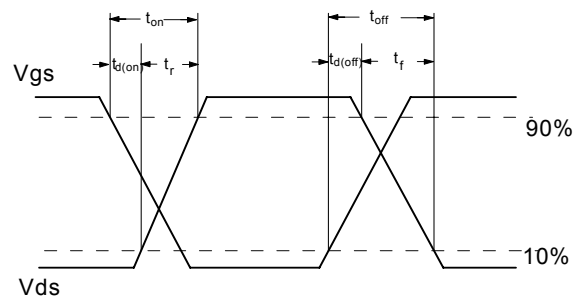
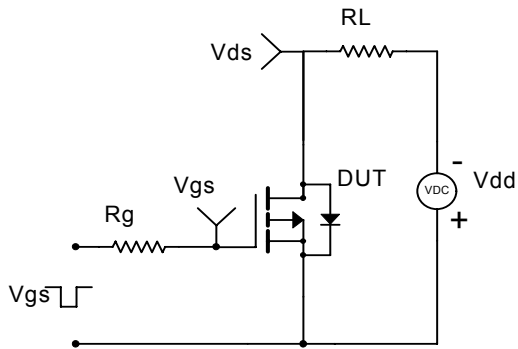


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

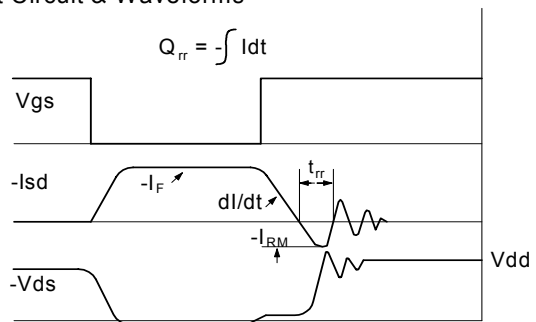
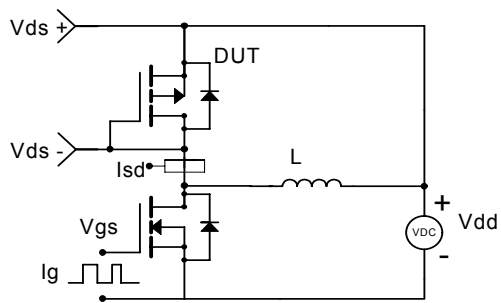
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



单击下面可查看定价，库存，交付和生命周期等信息

[>>AOS\(万国半导体\)](#)