
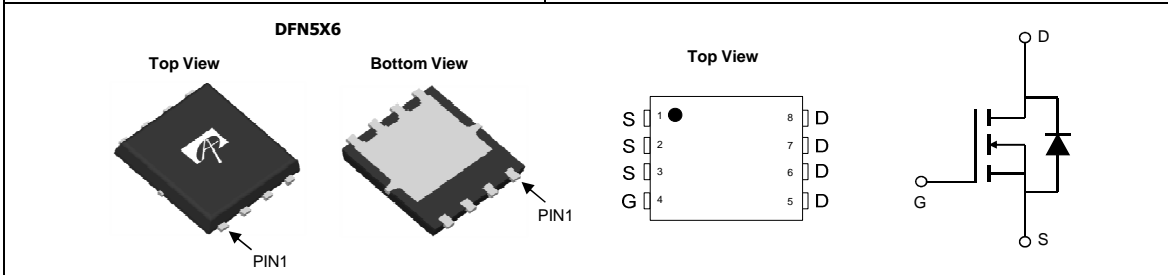


General Description	Product Summary
<ul style="list-style-type: none"> <li>Trench Power AlphaMOS (αMOS LV) technology</li> <li>Low <math>R_{DS(ON)}</math></li> <li>Low Gate Charge</li> <li>High Current Capability</li> <li>RoHS and Halogen-Free Compliant</li> </ul>	$V_{DS}$ 30V $I_D$ (at $V_{GS}=10V$ ) 32A $R_{DS(ON)}$ (at $V_{GS}=10V$ ) < 4.4mΩ $R_{DS(ON)}$ (at $V_{GS}=4.5V$ ) < 5.9mΩ
<b>Application</b> <ul style="list-style-type: none"> <li>DC/DC Converters in Computing, Servers, and POL</li> <li>Isolated DC/DC Converters in Telecom and Industrial</li> </ul>	100% UIS Tested 100% Rg Tested 



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON6510	DFN 5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$	32
		$T_C=100^\circ\text{C}$	25
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	128	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	28
		$T_A=70^\circ\text{C}$	22
Avalanche Current <sup>C</sup>	$I_{AS}$	46	A
Avalanche energy	$E_{AS}$	53	mJ
$V_{DS}$ Spike	$V_{SPIKE}$	36	V
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	46
		$T_C=100^\circ\text{C}$	18.5
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	5
		$T_A=70^\circ\text{C}$	3.2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

Thermal Characteristics				
Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	20	25	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A D</sup>				
Maximum Junction-to-Case	$R_{\theta JC}$	2.2	2.7	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.4	1.8	2.2	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		3.6	4.4	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		4.9	6	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		91		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				32	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		2160		pF
C <sub>oss</sub>	Output Capacitance			915		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			115		pF
R <sub>g</sub>	Gate resistance	f=1MHz	0.9	1.8	2.7	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		30	42	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			14	20	nC
Q <sub>gs</sub>	Gate Source Charge			5.1		nC
Q <sub>gd</sub>	Gate Drain Charge			6.3		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		8		ns
t <sub>r</sub>	Turn-On Rise Time			4		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			29		ns
t <sub>f</sub>	Turn-Off Fall Time			5.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs		16.5		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs		34.2		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

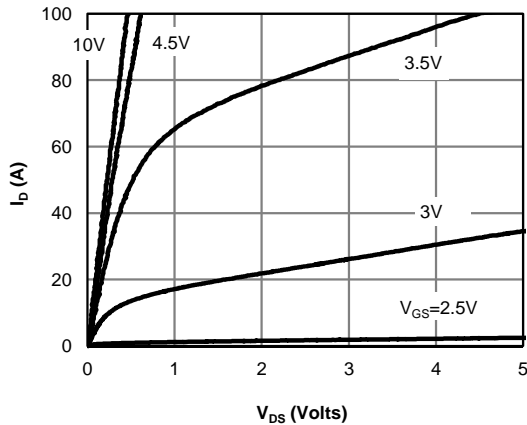


Figure 1: On-Region Characteristics (Note E)

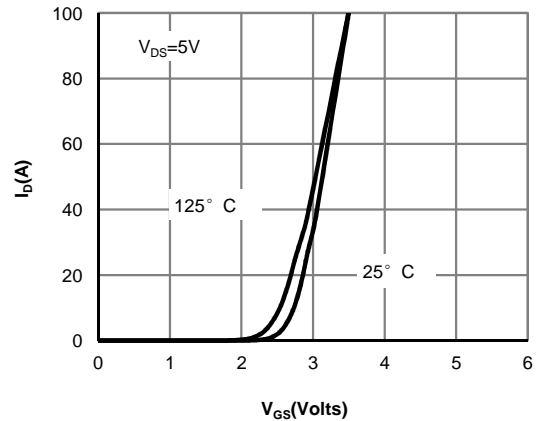


Figure 2: Transfer Characteristics (Note E)

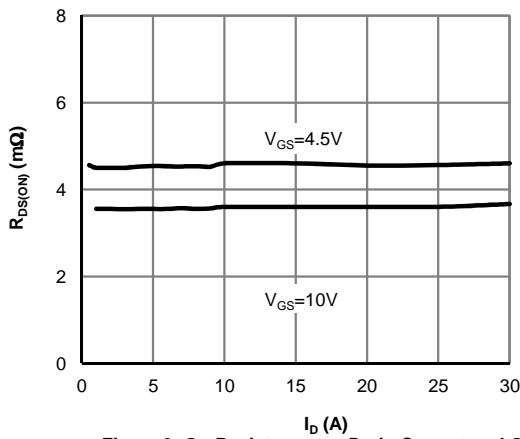


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

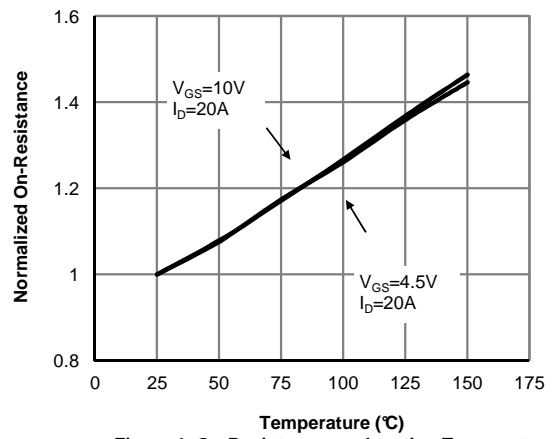


Figure 4: On-Resistance vs. Junction Temperature (Note E)

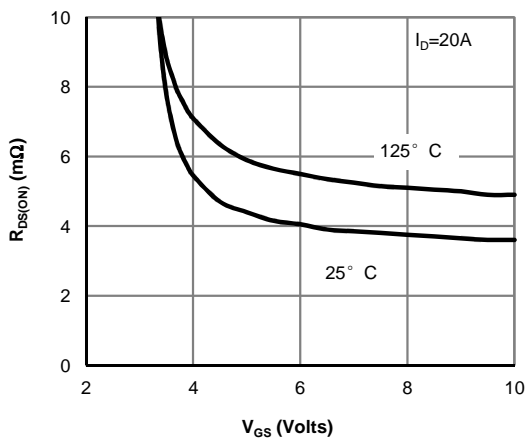


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

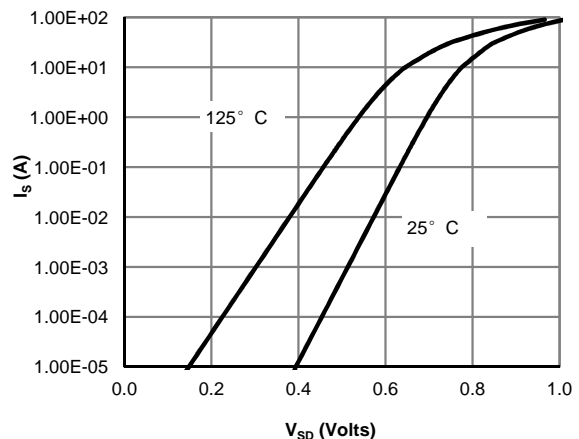


Figure 6: Body-Diode Characteristics (Note E)

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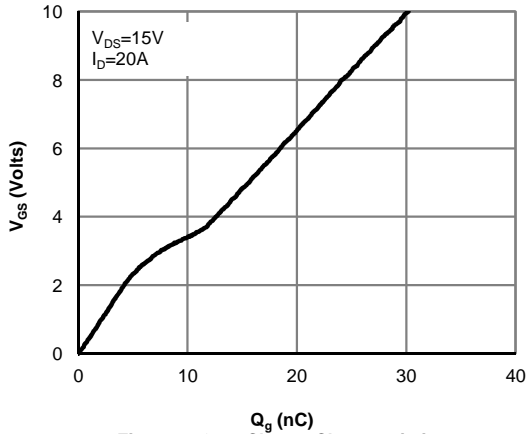


Figure 7: Gate-Charge Characteristics

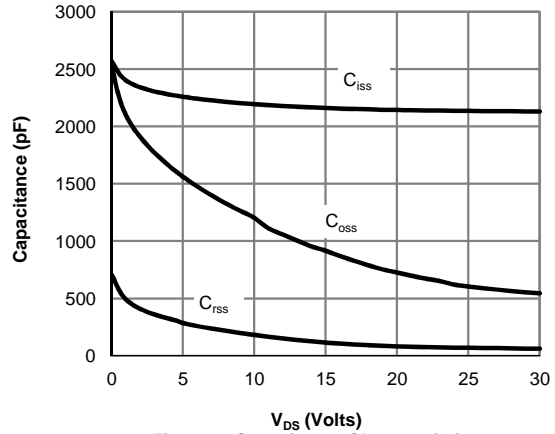


Figure 8: Capacitance Characteristics

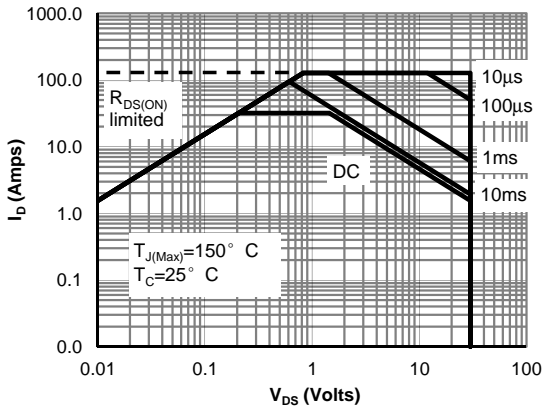


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

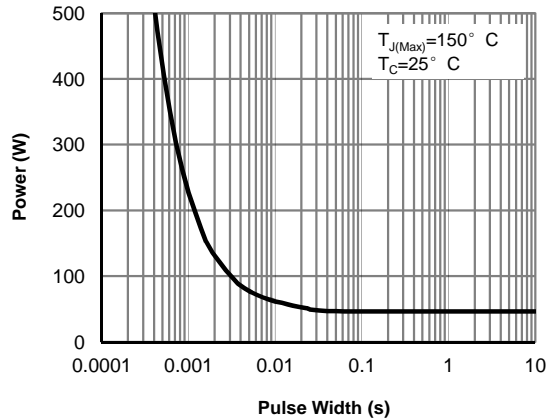


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

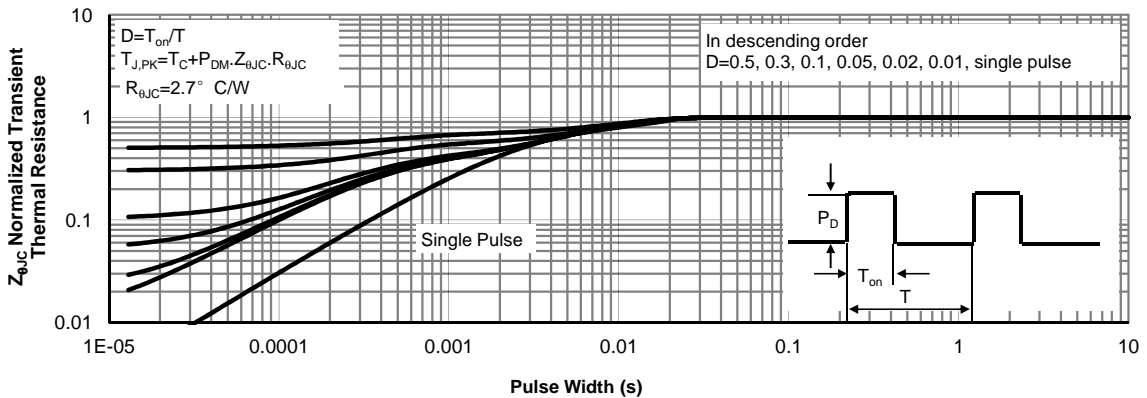


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

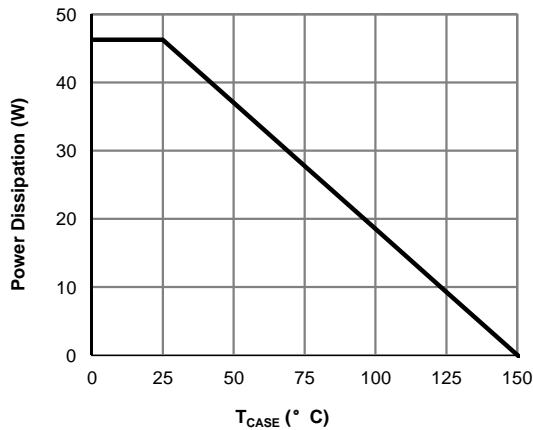


Figure 12: Power De-rating (Note F)

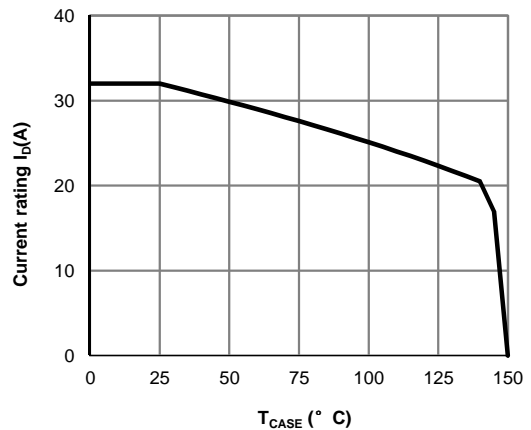


Figure 13: Current De-rating (Note F)

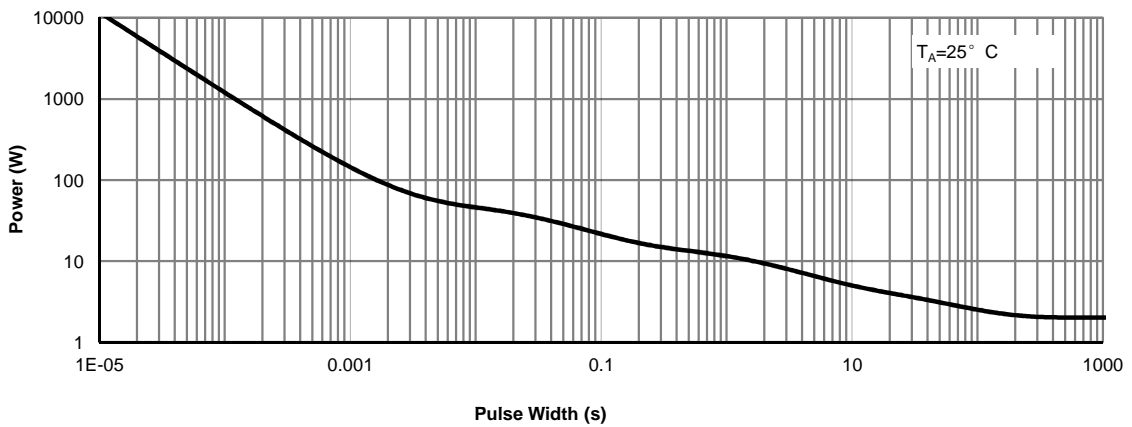


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

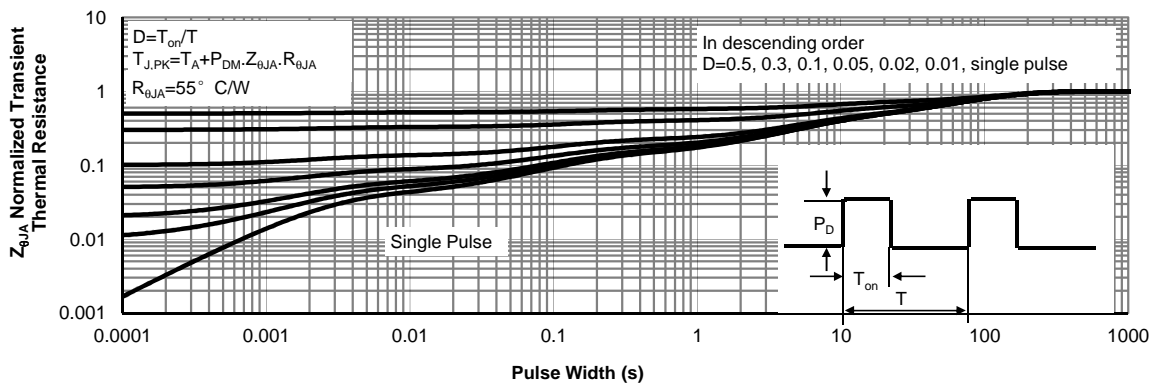
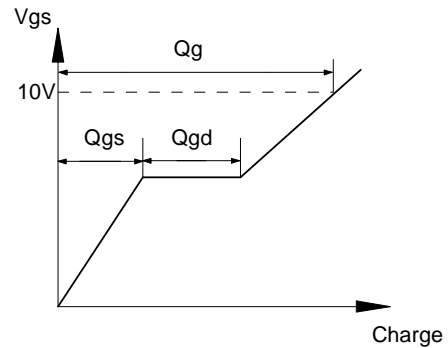
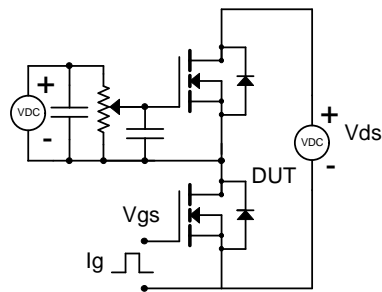
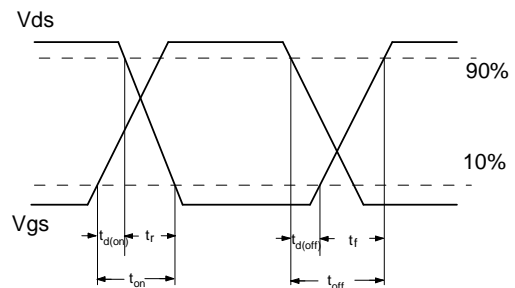
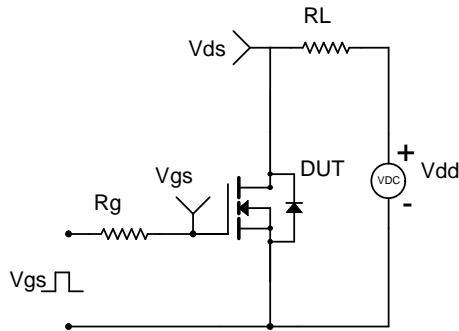


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

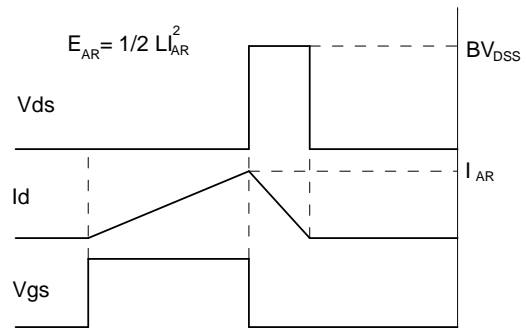
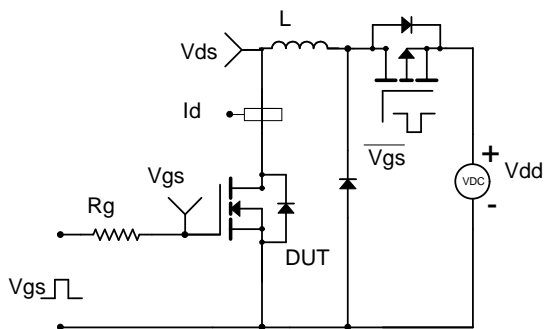
Gate Charge Test Circuit & Waveform



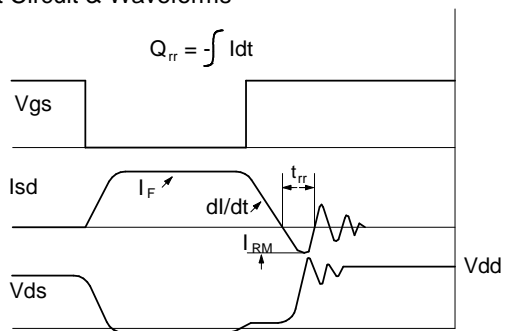
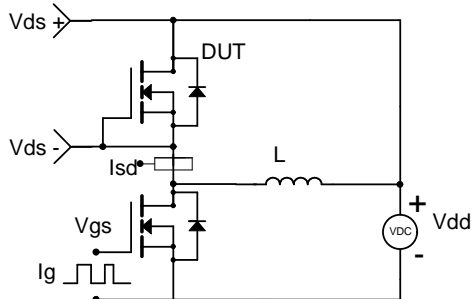
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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