

General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Very Low $R_{DS(on)}$ at $4.5V_{GS}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Application

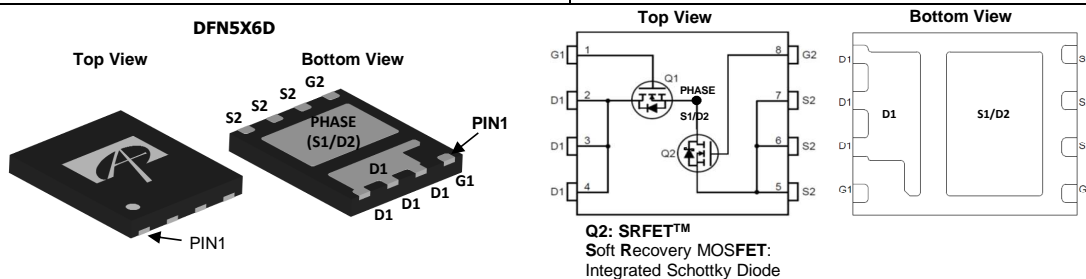
- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

Product Summary

	Q1	Q2
V_{DS}	30V	30V
I_D (at $V_{GS}=10V$)	56A	85A
$R_{DS(on)}$ (at $V_{GS}=10V$)	<5.7mΩ	<1.7mΩ
$R_{DS(on)}$ (at $V_{GS}=4.5V$)	<9.0mΩ	<2.2mΩ

100% UIS Tested

100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units	
Drain-Source Voltage	V_{DS}	30		V	
Gate-Source Voltage	V_{GS}	± 20	± 12	V	
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	56	85	A
		$T_C=100^\circ\text{C}$	35	66	
Pulsed Drain Current ^C	I_{DM}	132	340		
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	23	40	A
		$T_A=70^\circ\text{C}$	18	32	
Avalanche Current ^C	I_{AS}	30	64	A	
Avalanche Energy $L=0.05\text{mH}$ ^C	E_{AS}	23	102	mJ	
V_{DS} Spike	V_{SPIKE}	36	36	V	
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	31	78	W
		$T_C=100^\circ\text{C}$	12	31	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	5	4.1	W
		$T_A=70^\circ\text{C}$	3.2	2.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$	

Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	20	25	25	30	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient ^{A,D}		50	56	60	67	
Maximum Junction-to-Case	$R_{\theta JC}$	3.3	1.2	4	1.6	$^\circ\text{C}/\text{W}$

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.4	1.8	2.2	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		4.7	5.7	mΩ
		V _{GS} =4.5V, I _D =20A		7.1	9.0	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		80		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.67	1	V
I _S	Maximum Body-Diode Continuous Current				35	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance			1186		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		292		pF
C _{rss}	Reverse Transfer Capacitance			53		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.2	0.5	0.8	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		17	23	nC
Q _{g(4.5V)}	Total Gate Charge			7.8	11	nC
Q _{gs}	Gate Source Charge			3.1		nC
Q _{gd}	Gate Drain Charge			3.1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		5.5		ns
t _r	Turn-On Rise Time			16		ns
t _{D(off)}	Turn-Off DelayTime			19		ns
t _f	Turn-Off Fall Time			3		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		12.8		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		22.7		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

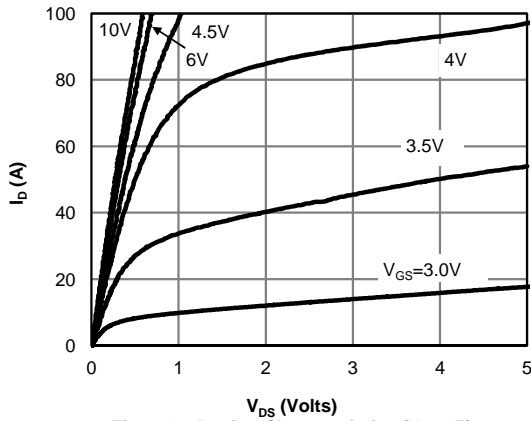


Figure 1: On-Region Characteristics (Note E)

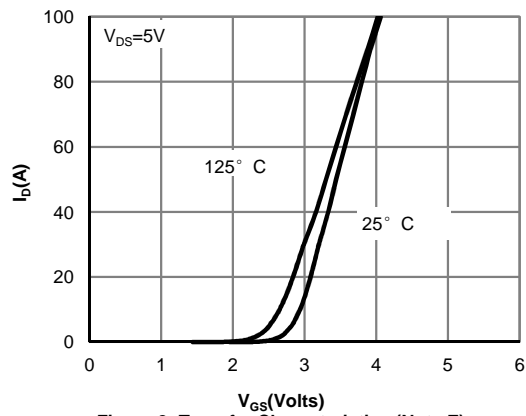


Figure 2: Transfer Characteristics (Note E)

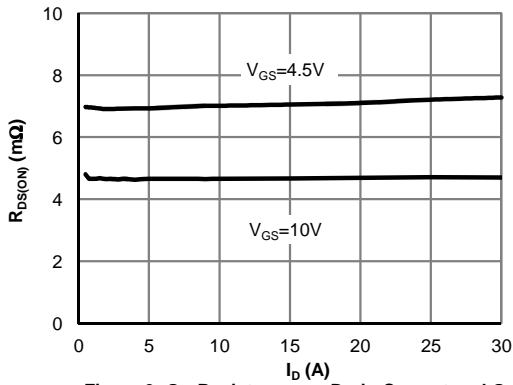


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

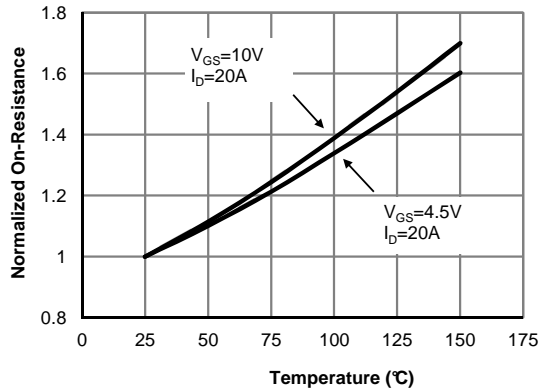


Figure 4: On-Resistance vs. Junction Temperature (Note E)

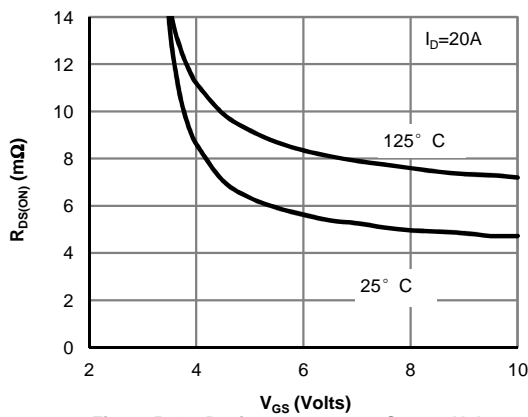


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

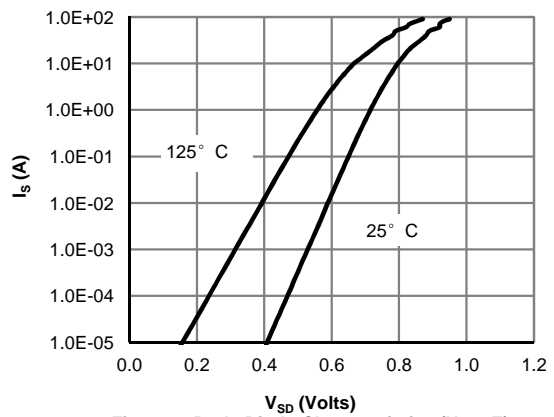


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

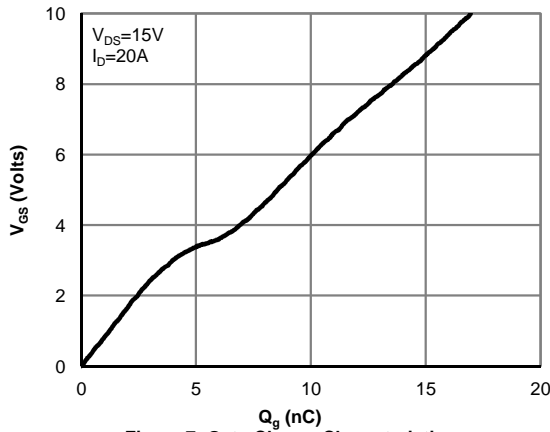


Figure 7: Gate-Charge Characteristics

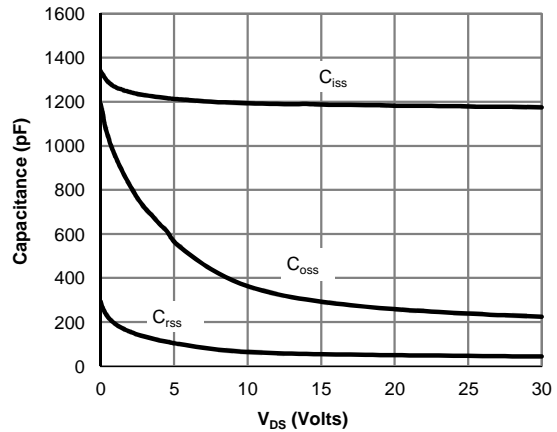


Figure 8: Capacitance Characteristics

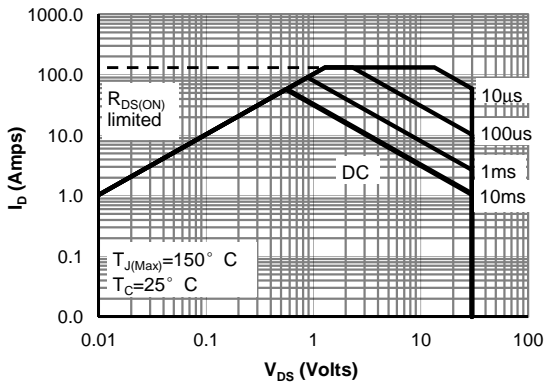


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

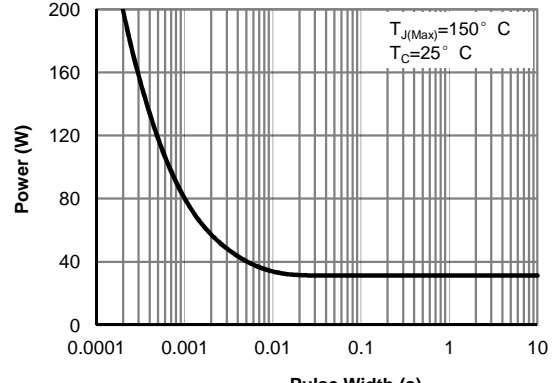


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

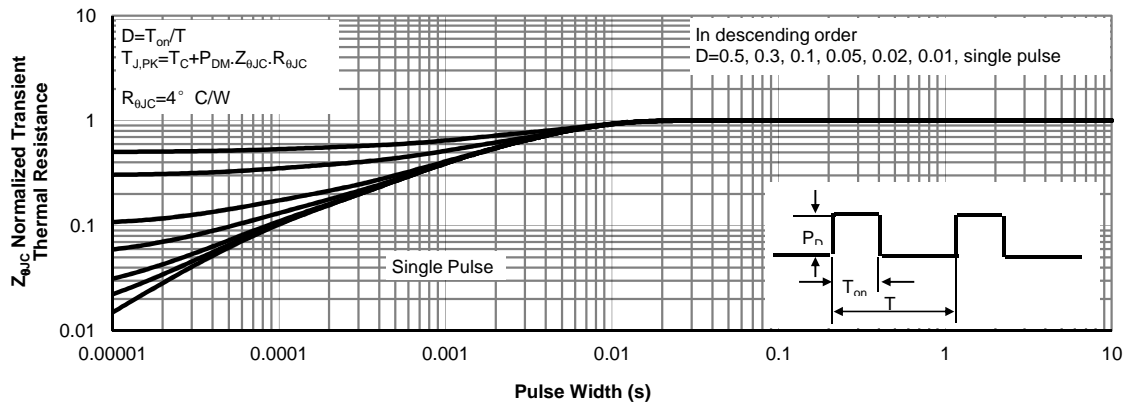


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

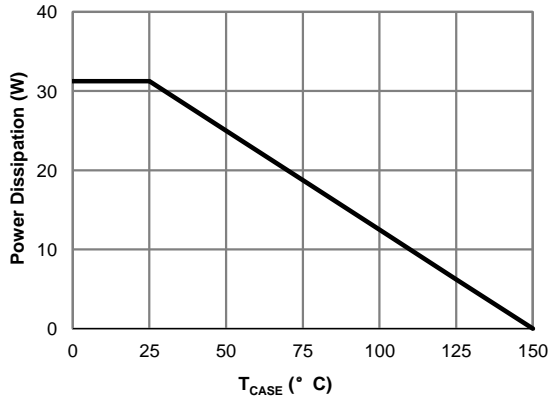


Figure 12: Power De-rating (Note F)

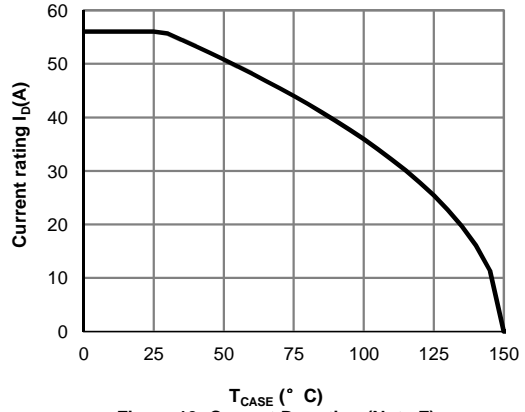


Figure 13: Current De-rating (Note F)

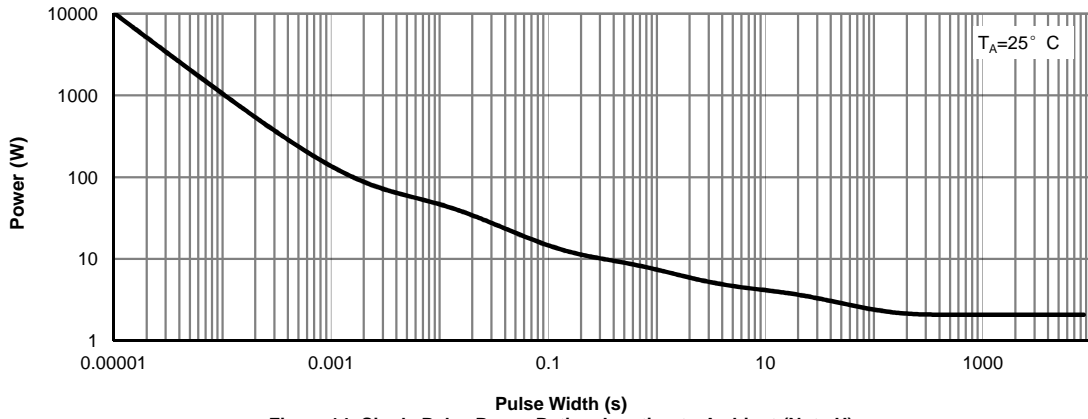


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

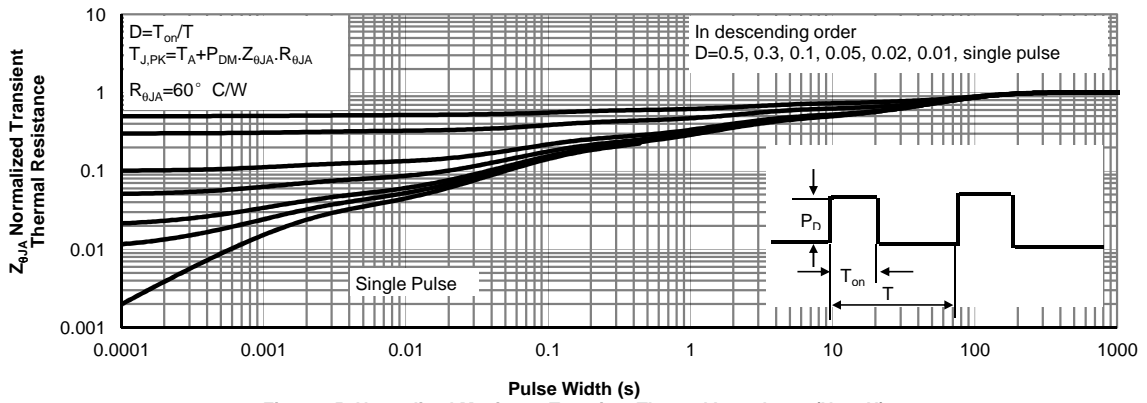


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			0.5 100	mA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.6	2	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		1.4	1.7	mΩ
		V _{GS} =4.5V, I _D =20A		2	2.4	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		180		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.44	0.6	V
I _S	Maximum Body-Diode Continuous Current ^G				85	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance			6221		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		1126		pF
C _{rss}	Reverse Transfer Capacitance			99		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.3	0.66	1	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge			88.4	120	nC
Q _{g(4.5V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		37.0	50	nC
Q _{gs}	Gate Source Charge			15.6		nC
Q _{gd}	Gate Drain Charge			7.4		nC
t _{D(on)}	Turn-On DelayTime			12		ns
t _r	Turn-On Rise Time	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω,		16		ns
t _{D(off)}	Turn-Off DelayTime	R _{GEN} =3Ω		53		ns
t _f	Turn-Off Fall Time			6.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		20		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		55.4		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

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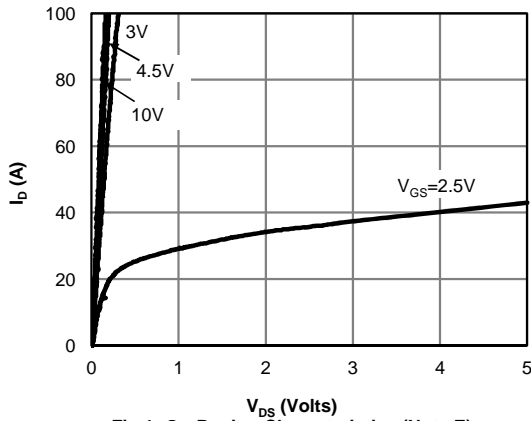


Fig 1: On-Region Characteristics (Note E)

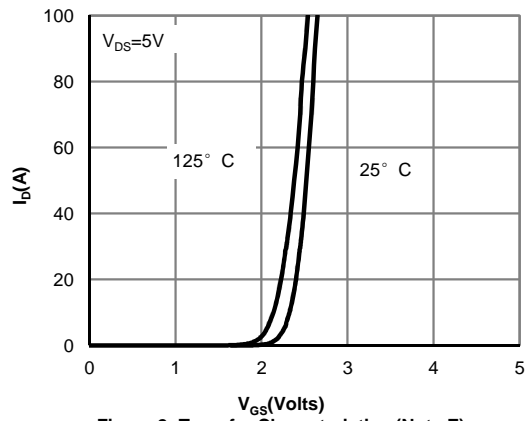


Figure 2: Transfer Characteristics (Note E)

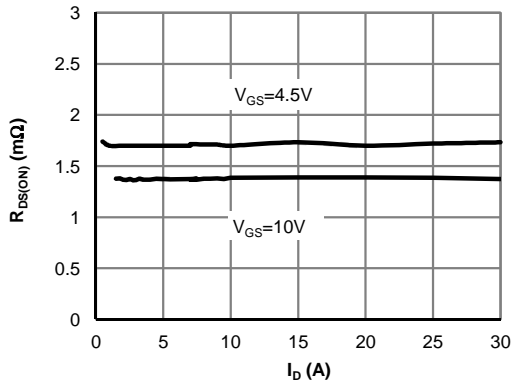


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

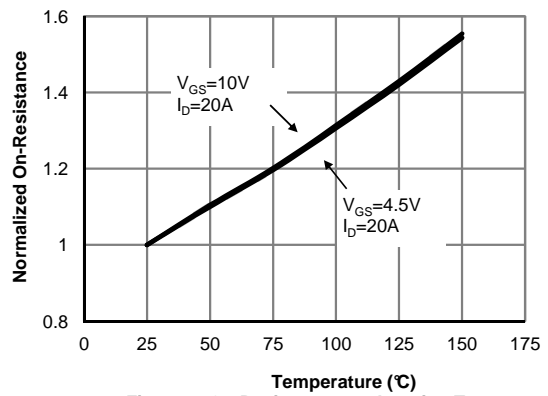


Figure 4: On-Resistance vs. Junction Temperature (Note E)

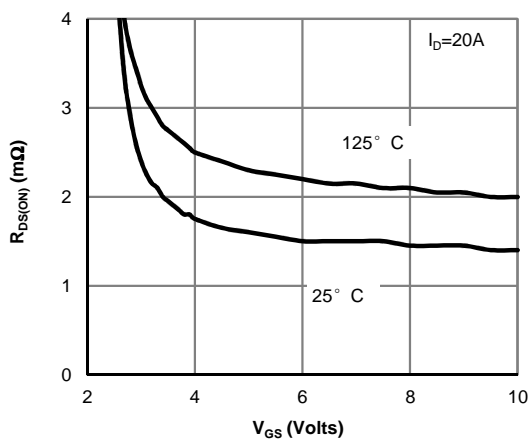


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

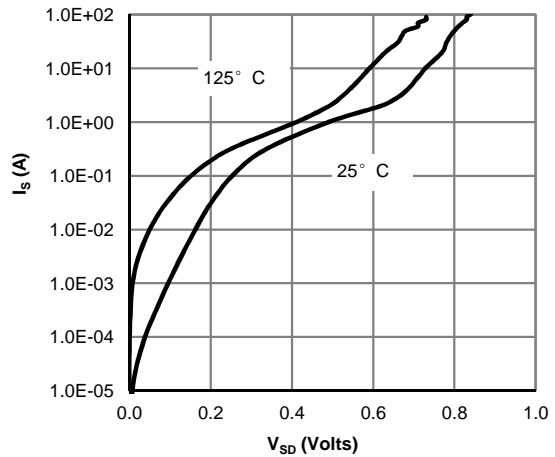


Figure 6: Body-Diode Characteristics (Note E)

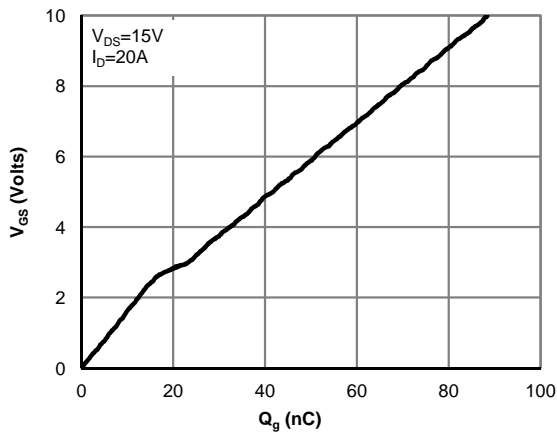


Figure 7: Gate-Charge Characteristics

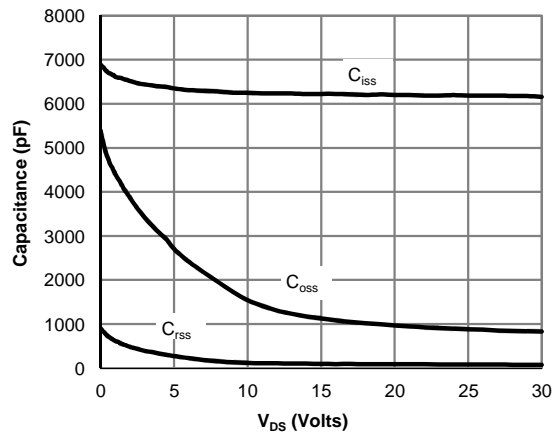


Figure 8: Capacitance Characteristics

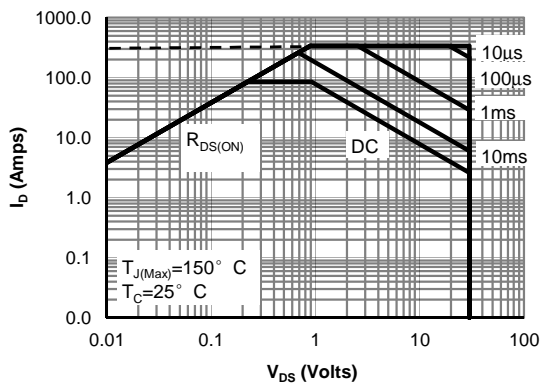


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

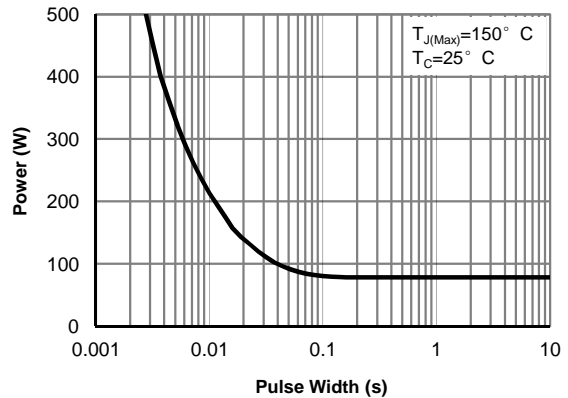


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

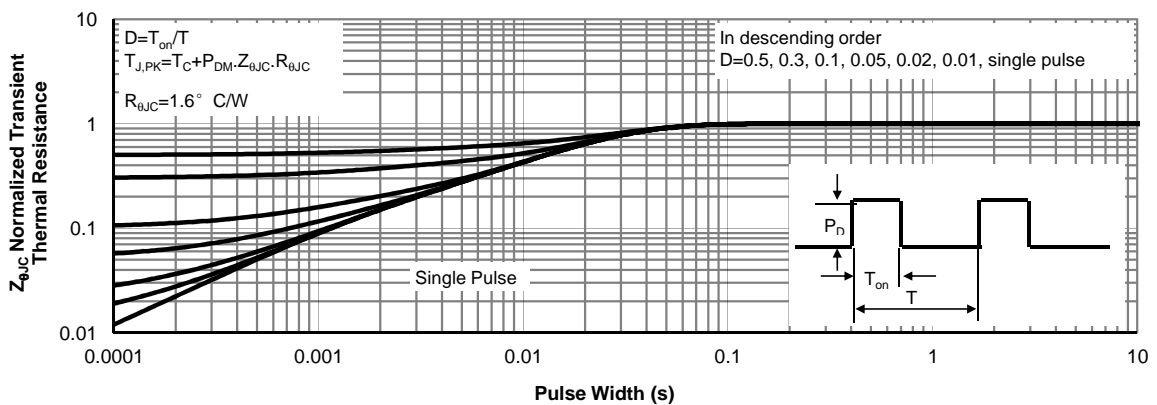


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

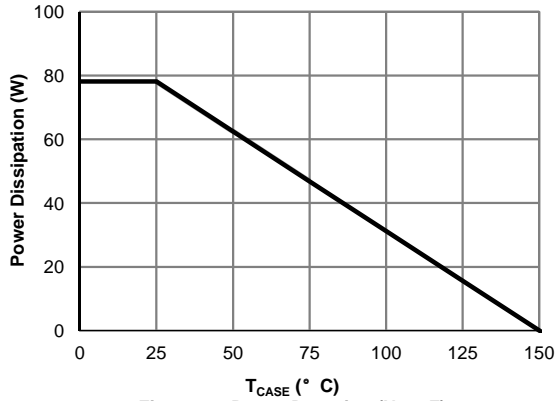


Figure 12: Power De-rating (Note F)

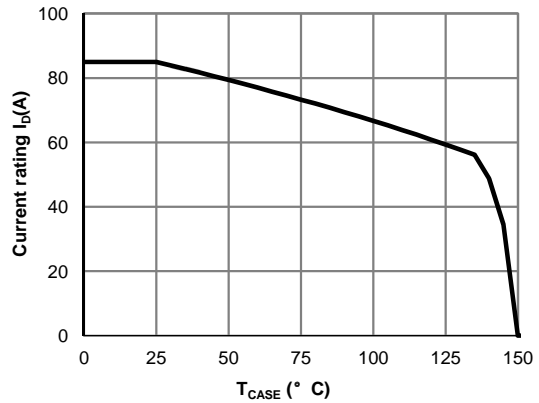


Figure 13: Current De-rating (Note F)



Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

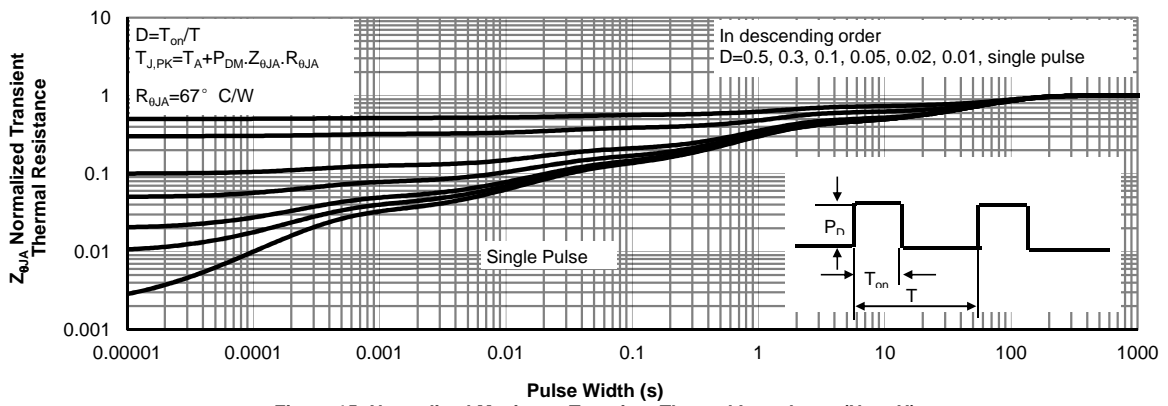
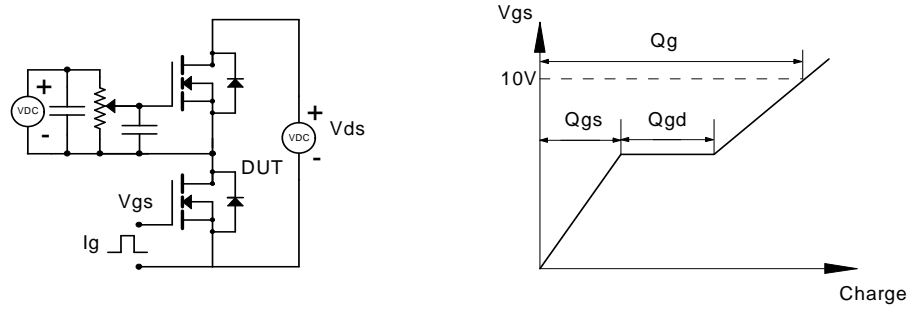
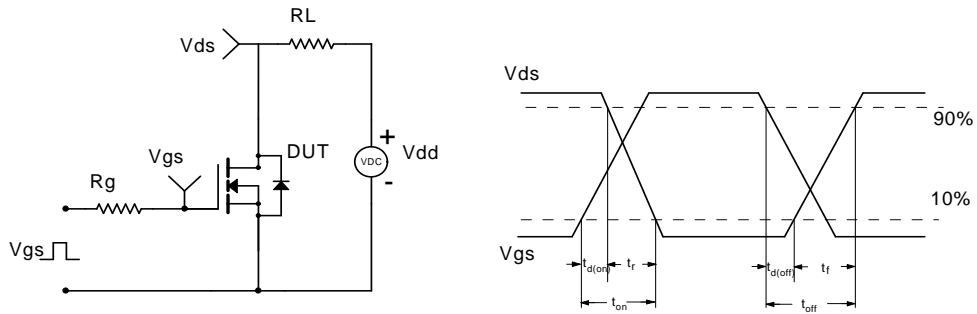


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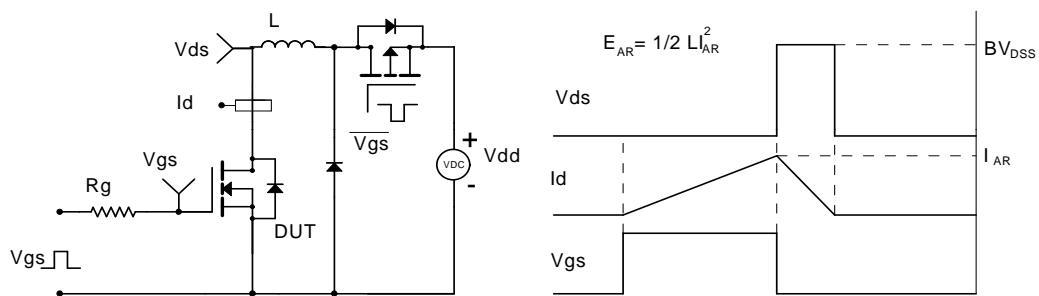
Gate Charge Test Circuit & Waveform



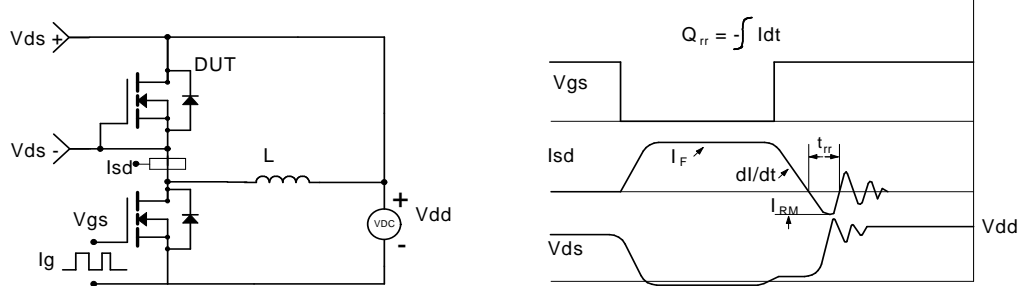
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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