

Inermal Characteristics										
Parameter	Symbol	Тур	Max	Units						
Maximum Junction-to-Ambient ^A	t ≤ 10s	P	30	40	°C/W					
Maximum Junction-to-Ambient AD	Steady-State	κ _{θJA}	60	75	°C/W					
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	3.5	4.2	°C/W					



Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Тур	Max	Units
STATIC F	PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V		-30			V
1	Zero Gate Voltage Drain Current	V_{DS} =-30V, V_{GS} =0V				-1	μA
I _{DSS}	Zero Gale Voltage Drain Current		T _J =55°C			-5	μA
I _{GSS}	Gate-Body leakage current	V_{DS} =0V, V_{GS} = ±25V				±100	nA
V _{GS(th)}	Gate Threshold Voltage	$V_{DS}=V_{GS}$ $I_{D}=-250\mu A$		-1.7	-2.2	-3	V
I _{D(ON)}	On state drain current	V_{GS} =-10V, V_{DS} =-5V		-80			А
		V _{GS} =-10V, I _D =-9A			11	14	mΩ
R _{DS(ON)}	Static Drain-Source On-Resistance		T _J =125°C		16	19	1115.2
		V_{GS} =-6V, I_{D} =-7A			12.9	17	mΩ
g fs	Forward Transconductance	V _{DS} =-5V, I _D =-9A			27		S
V_{SD}	Diode Forward Voltage	I _S =-1A,V _{GS} =0V			-0.7	-1	V
ls			-25	А			
DYNAMI	PARAMETERS						
C _{iss}	Input Capacitance				2060	2600	pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz			370		pF
C _{rss}	Reverse Transfer Capacitance				295		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1	MHz		2.4	3.6	Ω
SWITCHI	NG PARAMETERS						
Q _g (10V)	Total Gate Charge				30	39	nC
Q _{gs}	Gate Source Charge	V _{GS} =-10V, V _{DS} =-15V,	I _D =-9A		4.6		nC
Q_{gd}	Gate Drain Charge				10		nC
t _{D(on)}	Turn-On DelayTime				11		ns
t _r	Turn-On Rise Time	V _{GS} =-10V, V _{DS} =-15V,	$R_L=1.6\Omega$,		9.4		ns
t _{D(off)}	Turn-Off DelayTime	$R_{GEN}=3\Omega$			24		ns
t _f	Turn-Off Fall Time				12		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-9A, dI/dt=500A/μs	6		14	18	ns
Q _{rr}	Body Diode Reverse Recovery Charge	e I _F =-9A, dI/dt=500A/με	3		35		nC

A. The value of R_{0JA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}$ C. The Power dissipation P_{DSM} is based on R_{0JA} t \leq 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.

B. The power dissipation P_{D} is based on $T_{J(MAX)=}150^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)=}150^{\circ}$ C. Ratings are based on low frequency and duty cycles to keep initial $T_{J}=25^{\circ}$ C.

D. The R_{0JA} is the sum of the thermal impedence from junction to case R_{0JC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)=}150^{\circ}$ C. The SOA curve provides a single pulse rating.

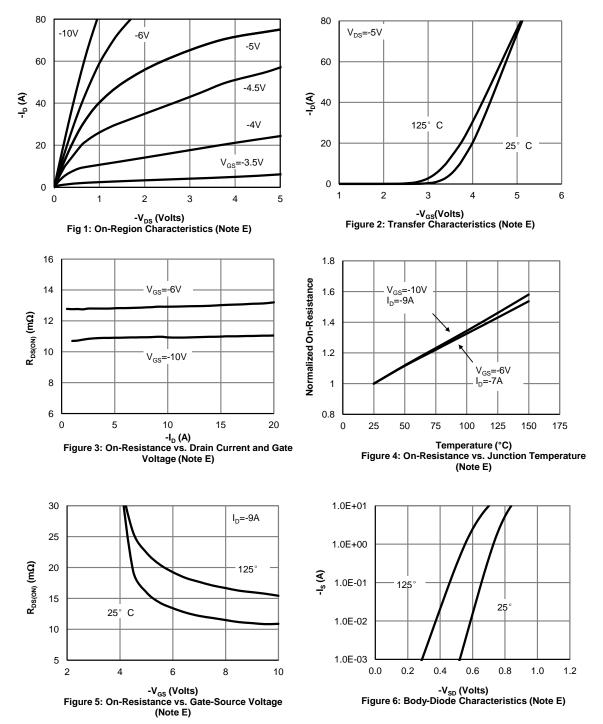
G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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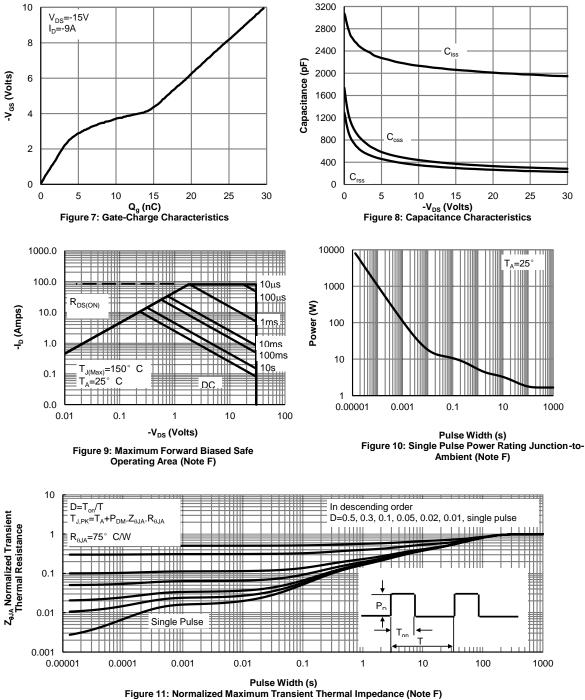


TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS





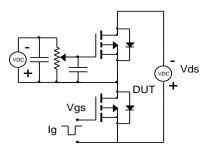
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

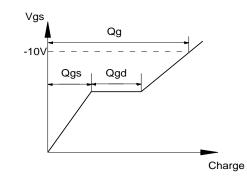




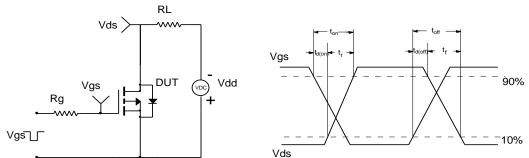


Gate Charge Test Circuit & Waveform

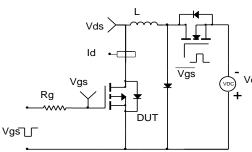


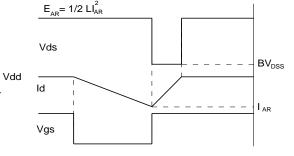


Resistive Switching Test Circuit & Waveforms

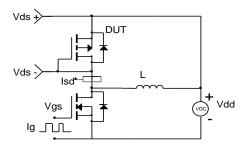


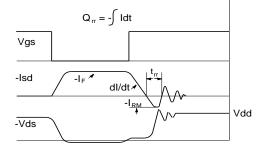
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms

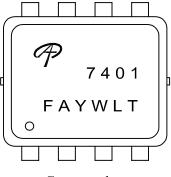






Document No.	PD-00873				
Version	В				
Title	AON7401 Marking Description				

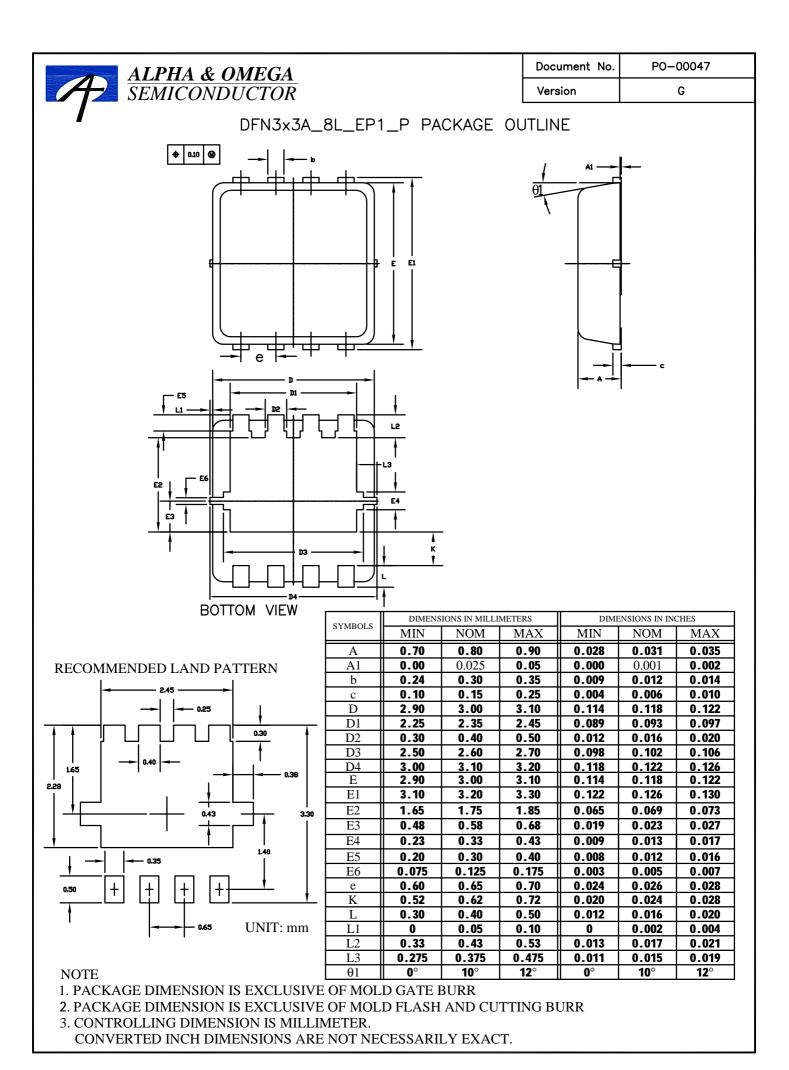
DFN3X3 PACKAGE MARKING DESCRIPTION



Green product

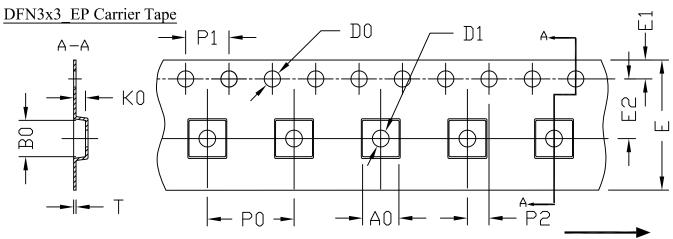
NOTE:	
LOGO	- AOS Logo
7401	- Part number code
F	- Fab code
A	 Assembly location code
Y	- Year code
W	- Week code
L&T	- Assembly lot code

PART NO.	DESCRIPTION	CODE
AON7401	Green product	7401
AON7401L	Green product	7401



DFN3x3_EP Tape and Reel Data

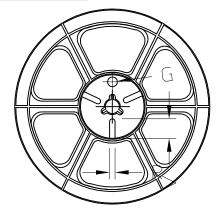


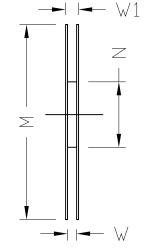


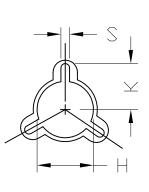
UNII: MM	UNIT:	MM
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UNIT: MM											FEEDING D	IRECTION
PACKAGE	A0	BO	K0	DO	D1	E	E1	E2	PO	P1	P2	Т
DFN3×3_EP	3.40 ±0.10	3.35 ±0.10	1.10 ±0.10	1.50 +0.10 -0	1.50 +0.10 -0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

DFN3x3_EP REEL

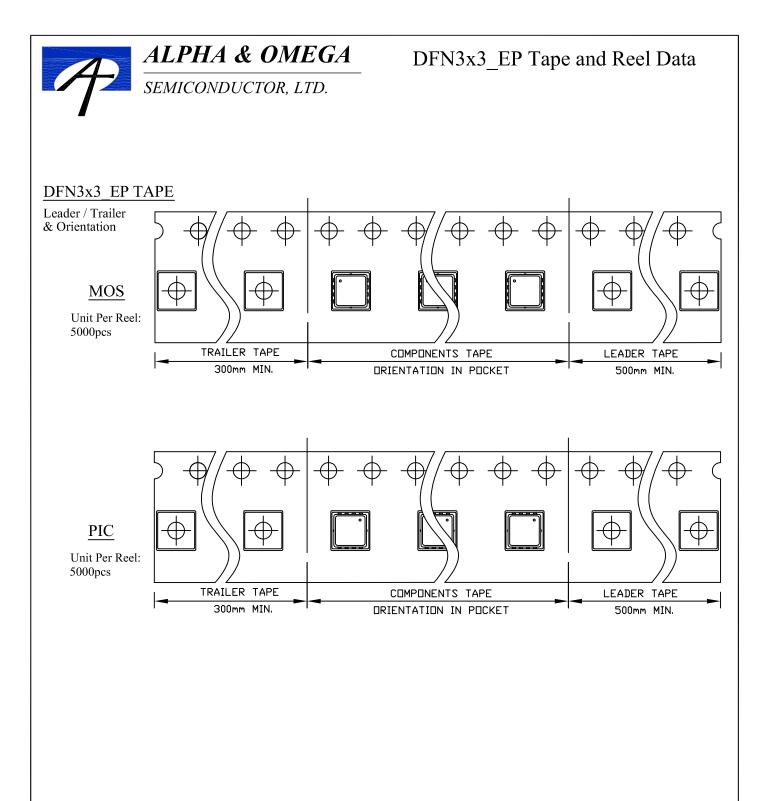






UNIT: MM

TAPE SIZE	reel size	М	Ν	W	W1	Н	К	S	G	R	V
12 mm	ø330	Ø330.00 ±0.50	Ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	Ø13.00 +0.50 -0.20	10.60	2.00 ±0.50			





AOS Semiconductor Product Reliability Report

AON7401, rev C

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com



This AOS product reliability report summarizes the qualification result for AON7401. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AON7401 passes AOS quality and reliability requirements.

Table of Contents:

- I. Product Description
- II. Package and Die information
- III. Environmental Stress Test Summary and Result
- IV. Reliability Evaluation

I. Product Description:

The AON7401 uses advanced trench technology to provide excellent $R_{DS(ON)}$, and ultra-low low gate charge with a 25V gate rating. This device is suitable for use as a load switch or in PWM applications.

-RoHS Compliant -Halogen-Free

Detailed information refers to datasheet.

II. Die / Package Information:

	AON7401
Process	Standard sub-micron
	Low voltage P channel
Package Type	DFN 3x3A
Lead Frame	Cu
Die Attach	Ag epoxy
Bonding	Cu wire
Mold Material	Epoxy resin with silica filler
MSL (moisture sensitive level)	Level 1 based on J-STD-020

Note * based on information provided by assembler and mold compound supplier



III. Result of Reliability Stress for AON7401

Test Item	Test Condition	Time Point	Lot Attribution	Total Sample size	Number of Failures	Standard
MSL Precondition	168hr 85℃ /85%RH +3 cycle reflow@260℃	-	11 lots	2299pcs	0	JESD22- A113
HTGB	Temp = 150 °c, Vgs=100% of Vgsmax	168hrs 500hrs 1000 hrs	1 lot 3 lots (Note A*)	308pcs 77pcs / lot	0	JESD22- A108
HTRB	Temp = 150 °c, Vds=80% of Vdsmax	168hrs 500hrs 1000 hrs	1 lot 3 lots (Note A*)	308pcs 77pcs / lot	0	JESD22- A108
HAST	130°c, 85%RH, 33.3 psi, Vgs = 100% of Vgs max	100 hrs	(Note A*)	605pcs 55pcs / lot	0	JESD22- A110
Pressure Pot	121°c, 29.7psi, RH=100%	96 hrs	11 lots (Note A*)	847pcs 77pcs / lot	0	JESD22- A102
Temperature Cycle	-65°c to 150°c, air to air	250 / 500 cycles	(Note A*)	847pcs 77pcs / lot	0	JESD22- A104

Note A: The reliability data presents total of available generic data up to the published date.

IV. Reliability Evaluation

FIT rate (per billion): 7 MTTF = 15704 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the selected product (AON7401). Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 x \ 10^9 / [2 (N) (H) (Af)]$ = 1.83 x 10⁹ / [2x (2x77x168+ 6x77x1000) x258] = 7 MTTF = 10⁹ / FIT = 1.38 x 10⁸hrs = 15704 years

 Chi^2 = Chi Squared Distribution, determined by the number of failures and confidence interval N = Total Number of units from HTRB and HTGB tests

H = Duration of HTRB/HTGB testing

Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C) Acceleration Factor [Af] = **Exp** [Ea / k (1/Tj u - 1/Tj s)]

Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	258	87	32	13	5.64	2.59	1

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16

Tj u = The use junction temperature in degree (Kelvin), K = C+273.16

 $\mathbf{K} = \text{Boltzmann's constant}, 8.617164 \text{ X } 10^{-5} \text{eV} / \text{K}$

单击下面可查看定价,库存,交付和生命周期等信息

>>AOS(万代)