

General Description

- Trench Power MOSFET technology
- Low $R_{DS(ON)}$
- RoHS and Halogen-Free Compliant

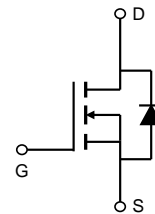
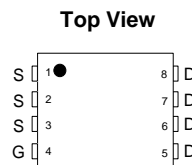
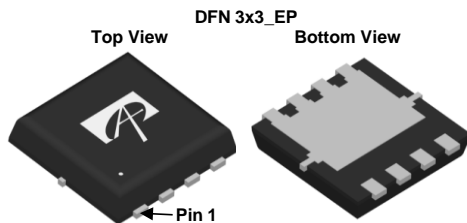
Applications

- DC/DC Converters in Computing, Servers, and POL
- Battery protection switch

Product Summary

V_{DS}	20V
I_D (at $V_{GS}=4.5V$)	20A
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 5.3m Ω
$R_{DS(ON)}$ (at $V_{GS}=2.5V$)	< 6.8m Ω

100% UIS Tested
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON7404G	DFN 3x3 EP	Tape & Reel	5000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	20
		$T_C=100^\circ\text{C}$	20
Pulsed Drain Current ^C	I_{DM}	80	A
Continuous Drain Current ^G	I_{DSM}	$T_A=25^\circ\text{C}$	20
		$T_A=70^\circ\text{C}$	20
Avalanche Current ^C	I_{AS}	40	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}	80	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	28
		$T_C=100^\circ\text{C}$	11
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	5
		$T_A=70^\circ\text{C}$	3.2
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	20	25	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	45	55
Maximum Junction-to-Case	$R_{\theta JC}$	3.7	4.5	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.45	0.85	1.25	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$ $T_J=125^\circ\text{C}$		4.4	5.3	m Ω
		$V_{GS}=2.5\text{V}$, $I_D=18\text{A}$		5.9	7.2	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		100		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.6	1	V
I_S	Maximum Body-Diode Continuous Current ^G				20	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=10\text{V}$, $f=1\text{MHz}$		3300		pF
C_{oss}	Output Capacitance			485		pF
C_{rfs}	Reverse Transfer Capacitance			370		pF
R_g	Gate resistance	$f=1\text{MHz}$	1.2	2.4	3.6	Ω
SWITCHING PARAMETERS						
$Q_g(4.5\text{V})$	Total Gate Charge	$V_{GS}=4.5\text{V}$, $V_{DS}=10\text{V}$, $I_D=20\text{A}$		31	45	nC
Q_{gs}	Gate Source Charge			5.2		nC
Q_{gd}	Gate Drain Charge			8		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=10\text{V}$, $R_L=0.5\Omega$, $R_{GEN}=3\Omega$		7.5		ns
t_r	Turn-On Rise Time			15		ns
$t_{D(off)}$	Turn-Off DelayTime			72		ns
t_f	Turn-Off Fall Time			21		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $di/dt=500\text{A}/\mu\text{s}$		17		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $di/dt=500\text{A}/\mu\text{s}$		30		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA} \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

APPLICATIONS OR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN,FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

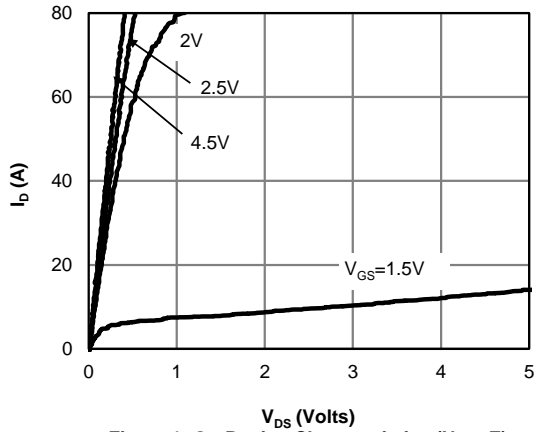


Figure 1: On-Region Characteristics (Note E)

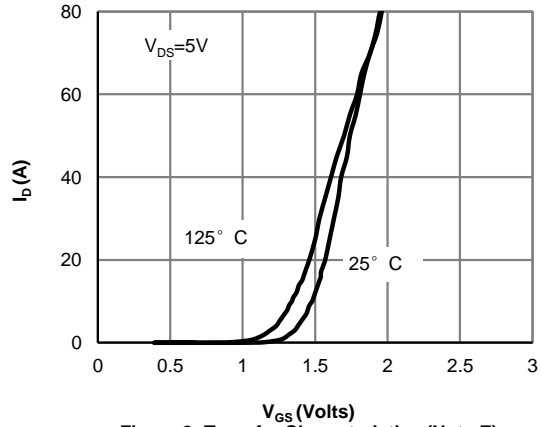


Figure 2: Transfer Characteristics (Note E)

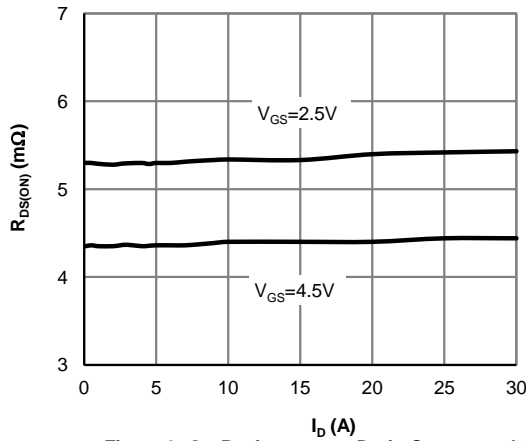


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

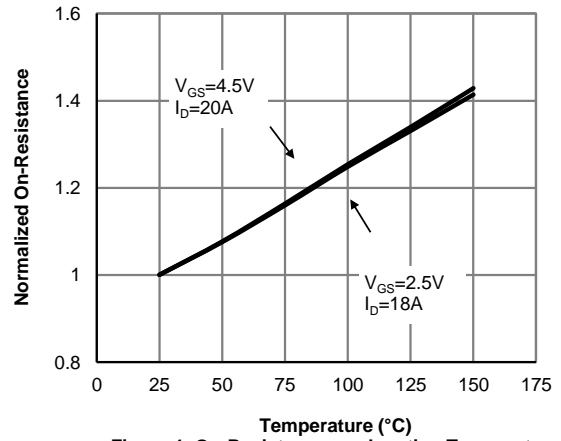


Figure 4: On-Resistance vs. Junction Temperature (Note E)

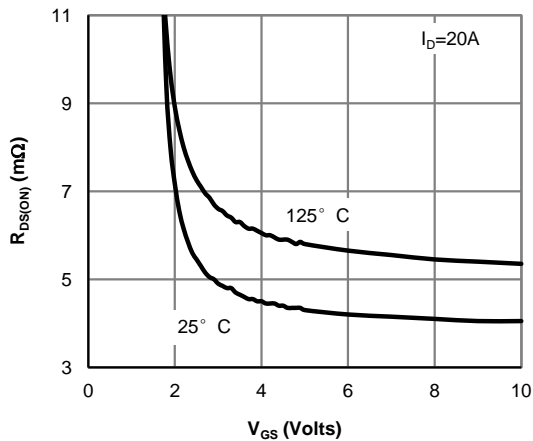


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

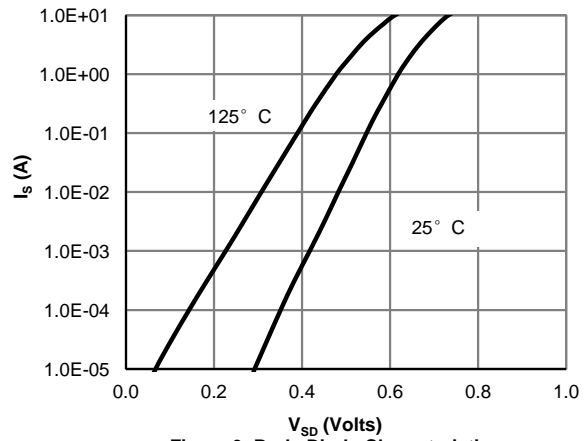


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

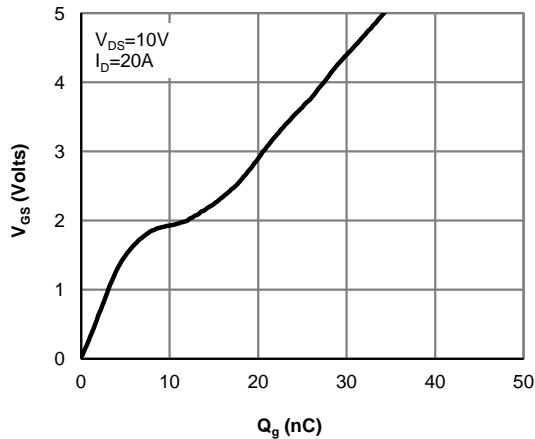


Figure 7: Gate-Charge Characteristics

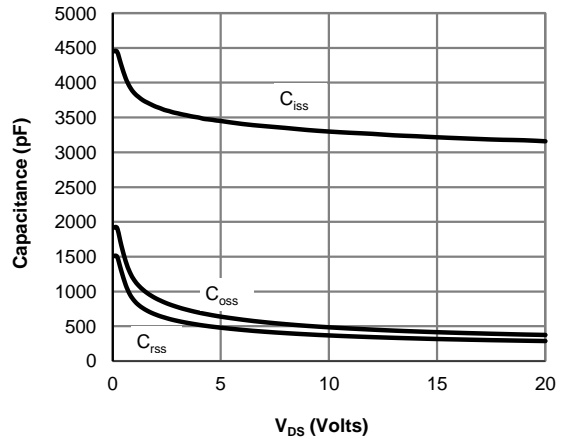


Figure 8: Capacitance Characteristics

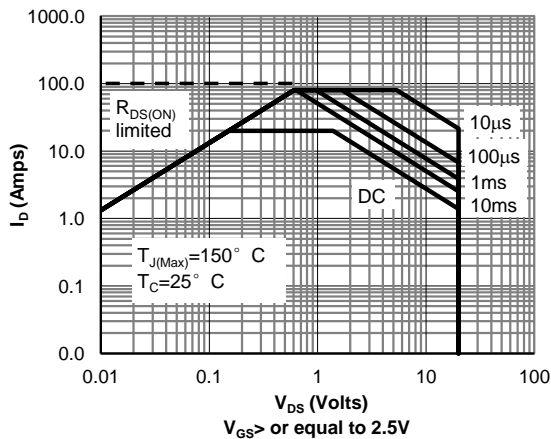


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

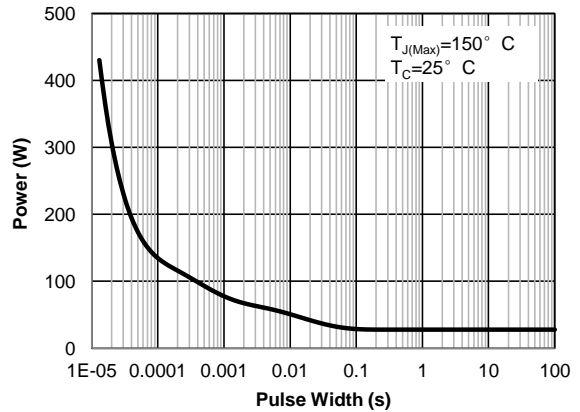


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

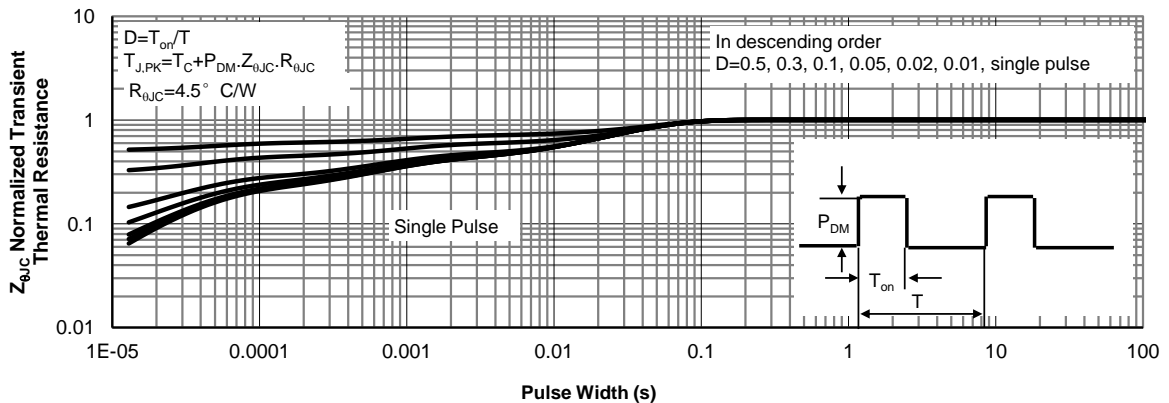


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

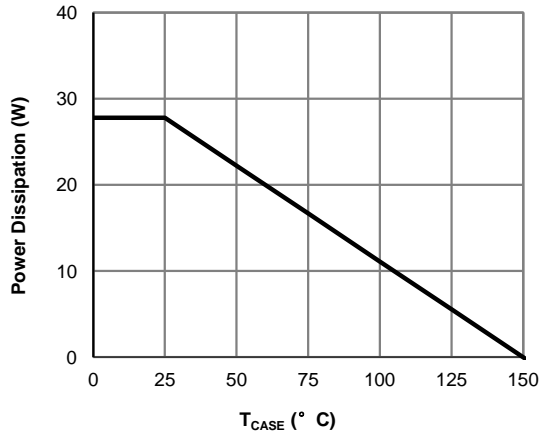


Figure 12: Power De-rating (Note F)

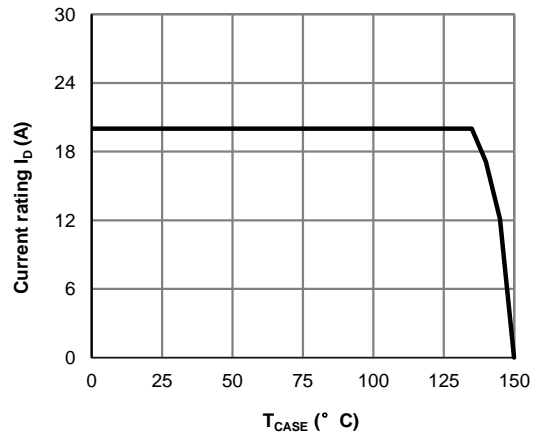


Figure 13: Current De-rating (Note F)

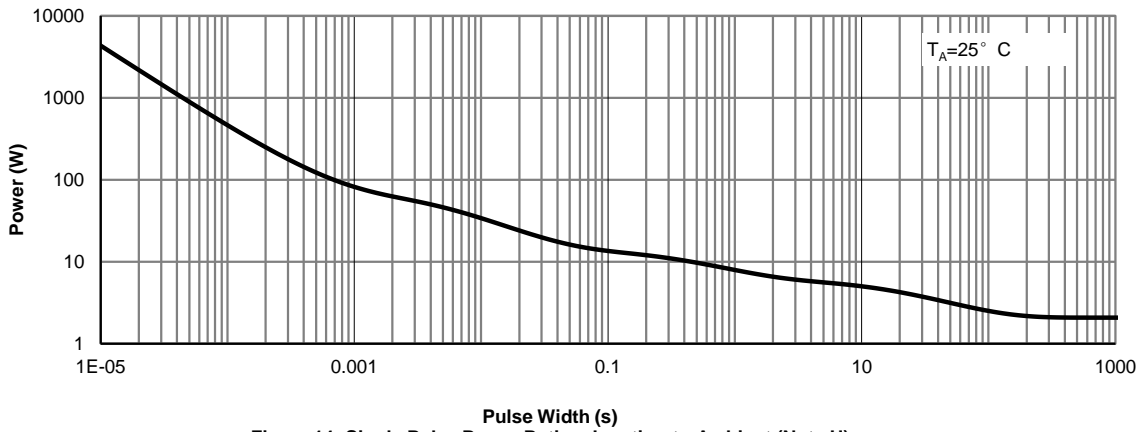


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

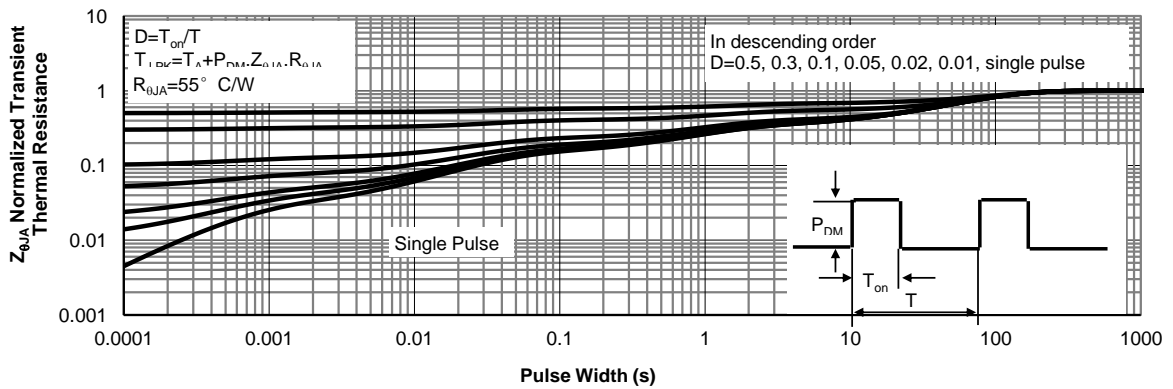


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

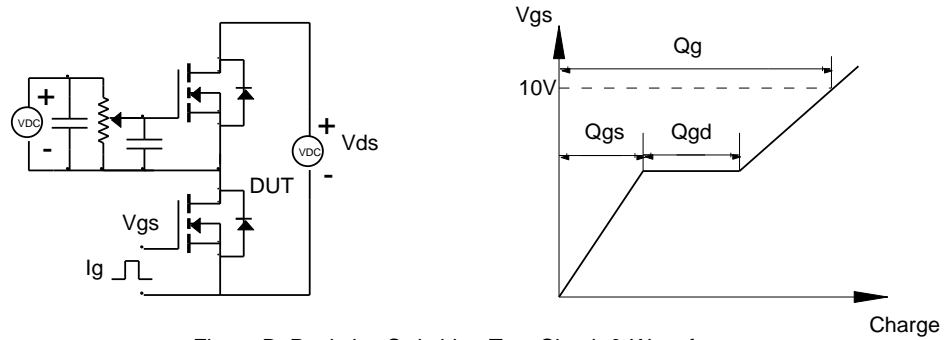


Figure B: Resistive Switching Test Circuit & Waveforms

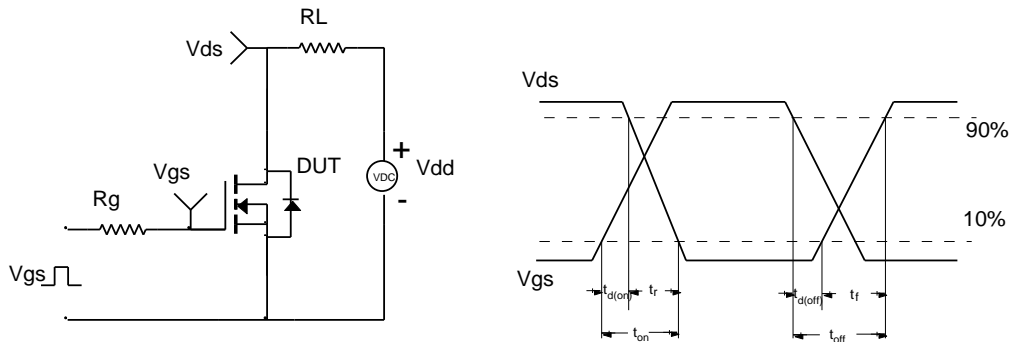


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

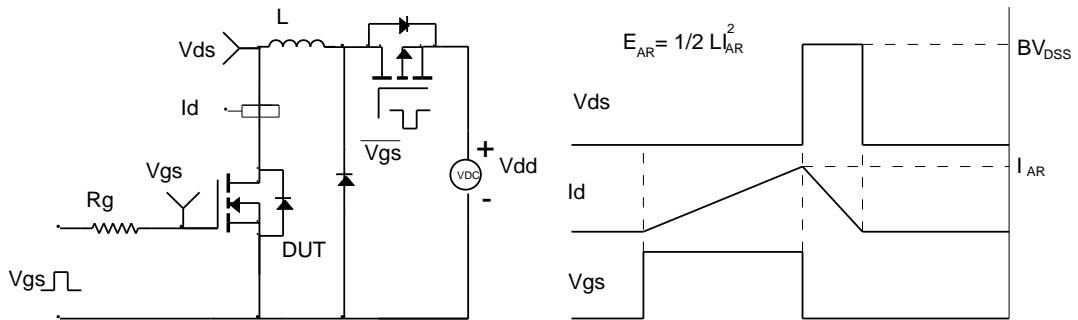
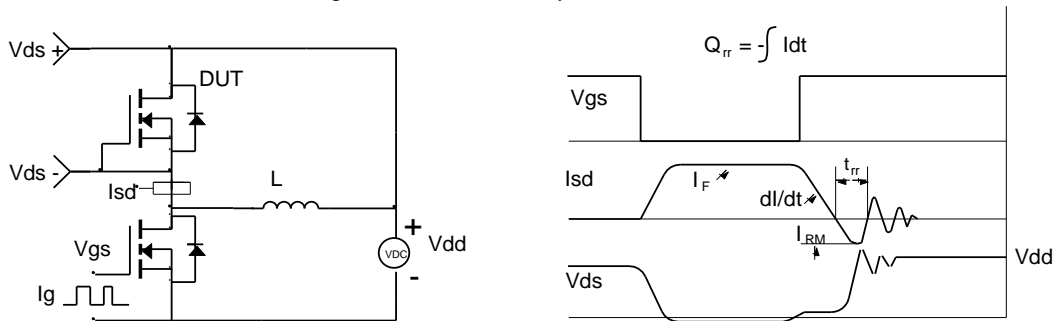


Figure D: Diode Recovery Test Circuit & Waveforms



单击下面可查看定价，库存，交付和生命周期等信息

[>>AOS\(万国半导体\)](#)