

General Description

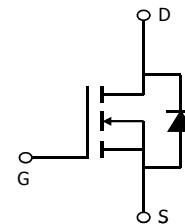
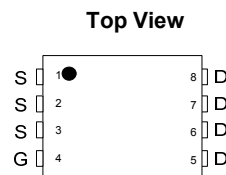
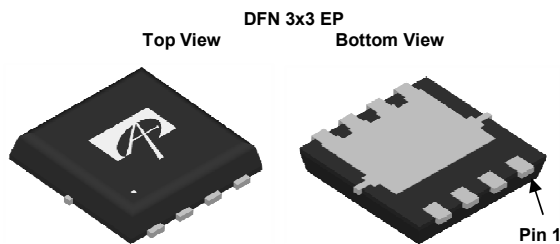
The AON7410 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC - DC converters and Load Switch applications.

RoHS and Halogen-Free Compliant

Features

V_{DS} (V) = 30V
 I_D = 24A ($V_{GS} = 10V$)
 $R_{DS(ON)} < 20m\Omega$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 26m\Omega$ ($V_{GS} = 4.5V$)

100% UIS Tested
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON7410	DFN 3x3 EP	Tape & Reel	5000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^B	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	50	A
Continuous Drain Current ^A	I_{DSM}	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Avalanche Current ^C	I_{AS}, I_{AR}	17	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	14	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$	30	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	60	$^\circ\text{C/W}$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	5	6	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.4	1.8	2.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	50			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =8A T _J =125°C		16 24	20 29	mΩ
		V _{GS} =4.5V, I _D =7A		21	26	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =8A		30		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				20	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	440	550	660	pF
C _{oss}	Output Capacitance		77	110	143	pF
C _{rss}	Reverse Transfer Capacitance		33	55	77	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	3	4	4.9	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =8A	7.8	9.8	12	nC
Q _g (4.5V)	Total Gate Charge		3.6	4.6	5.5	nC
Q _{gs}	Gate Source Charge		1.4	1.8	2.2	nC
Q _{gd}	Gate Drain Charge		1.3	2.2	3	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =2Ω, R _{GEN} =3Ω		5		ns
t _r	Turn-On Rise Time			3.2		ns
t _{D(off)}	Turn-Off DelayTime			24		ns
t _f	Turn-Off Fall Time			6		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =8A, di/dt=500A/μs	7	9	11	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =8A, di/dt=500A/μs	12	15	18	nC

- A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.
- B: The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C.
- D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.
- E: The static characteristics in Figures 1 to 6 are obtained using <300ms pulses, duty cycle 0.5% max.
- F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C.
- G: The maximum current rating is limited by bond-wires.
- H: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.
- Rev12: Jul-2011

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

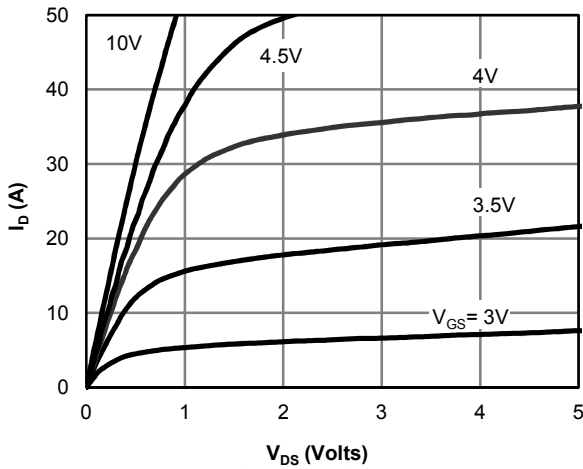


Figure 1: On-Region Characteristics

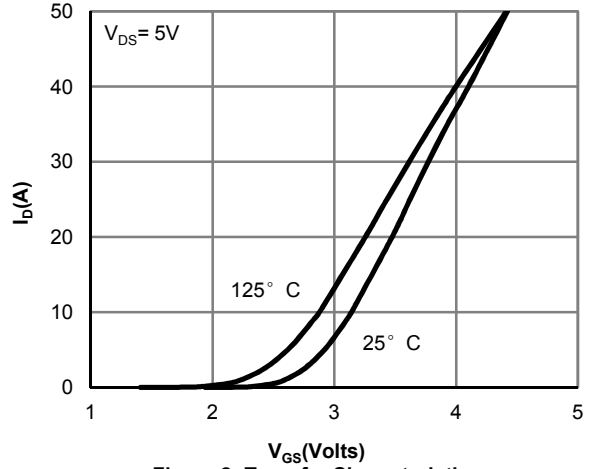


Figure 2: Transfer Characteristics

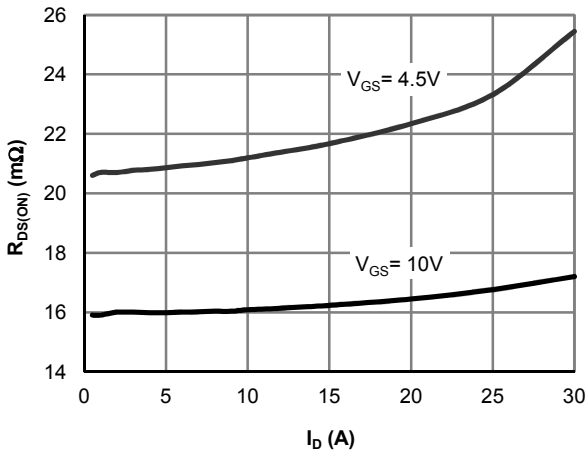


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

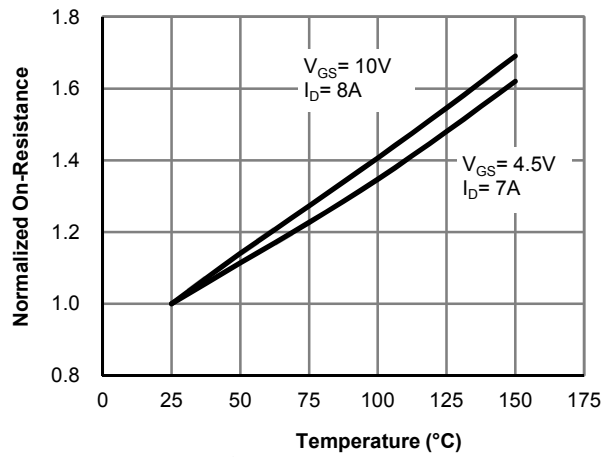


Figure 4: On-Resistance vs. Junction Temperature

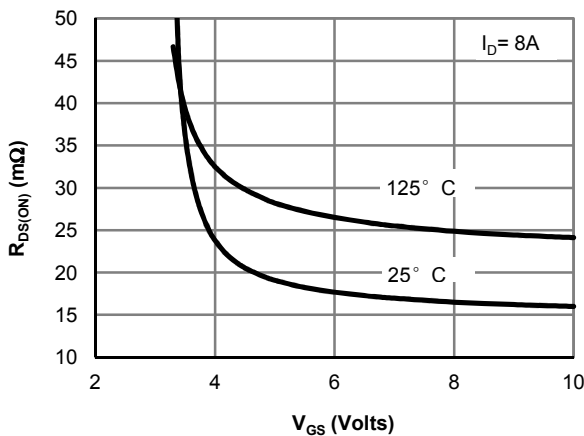


Figure 5: On-Resistance vs. Gate-Source Voltage

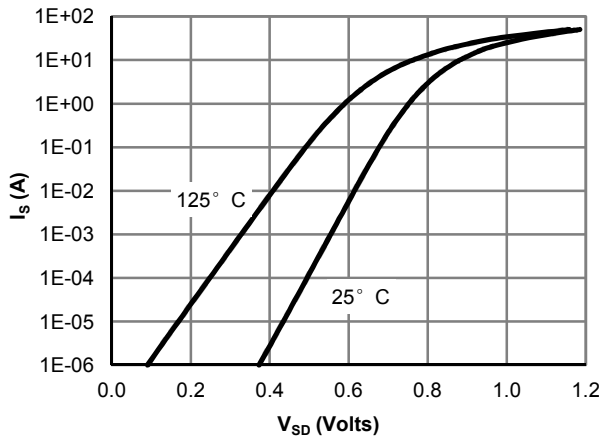


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTER

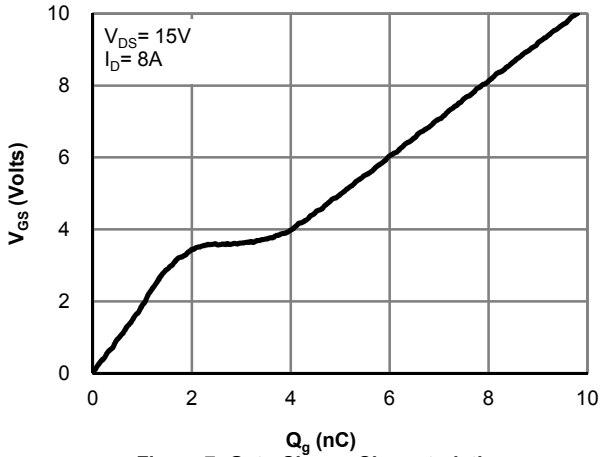


Figure 7: Gate-Charge Characteristics

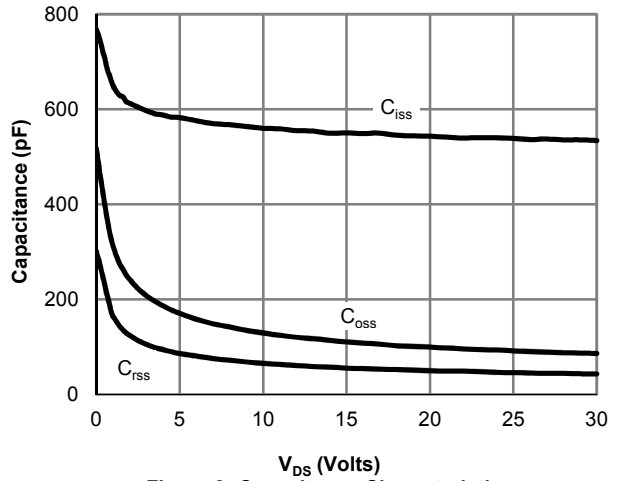


Figure 8: Capacitance Characteristics

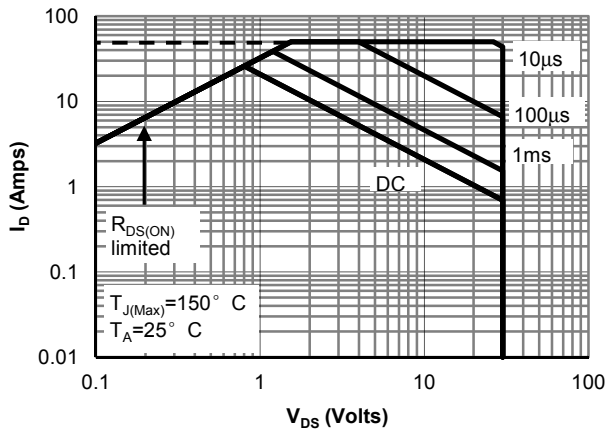


Figure 9: Maximum Forward Biased Safe Operating Area (Note H)

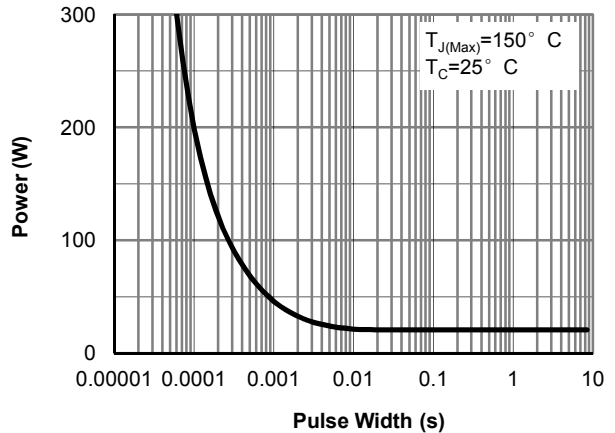


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

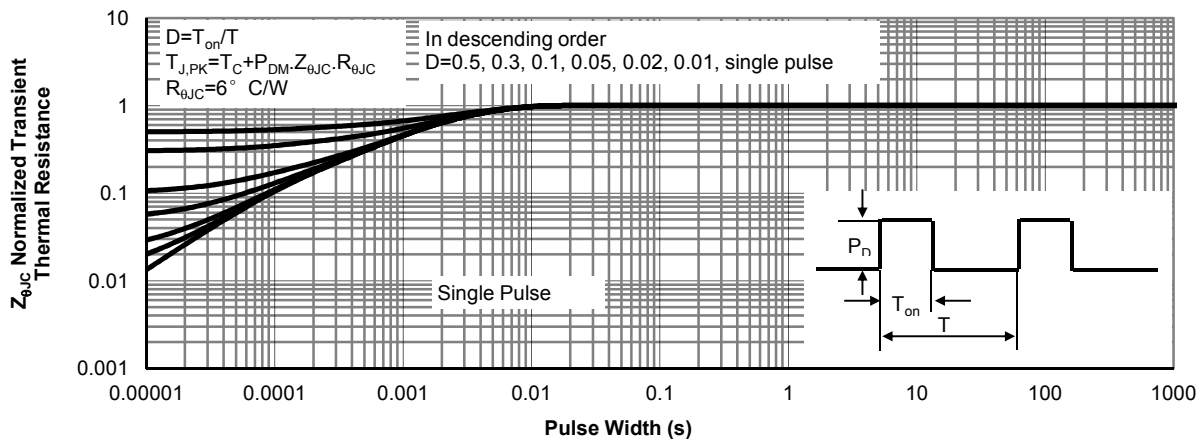


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

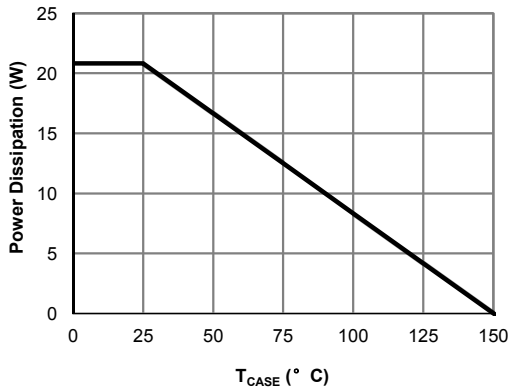


Figure 12: Power De-rating (Note F)

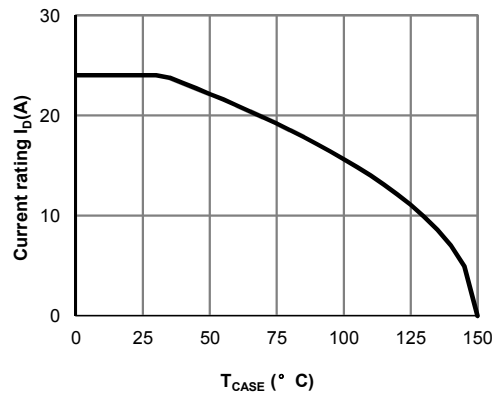


Figure 13: Current De-rating (Note F)

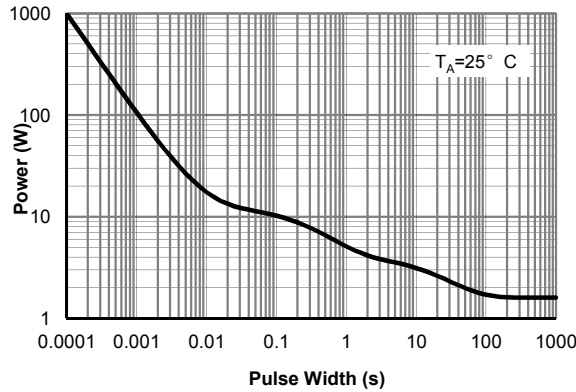


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

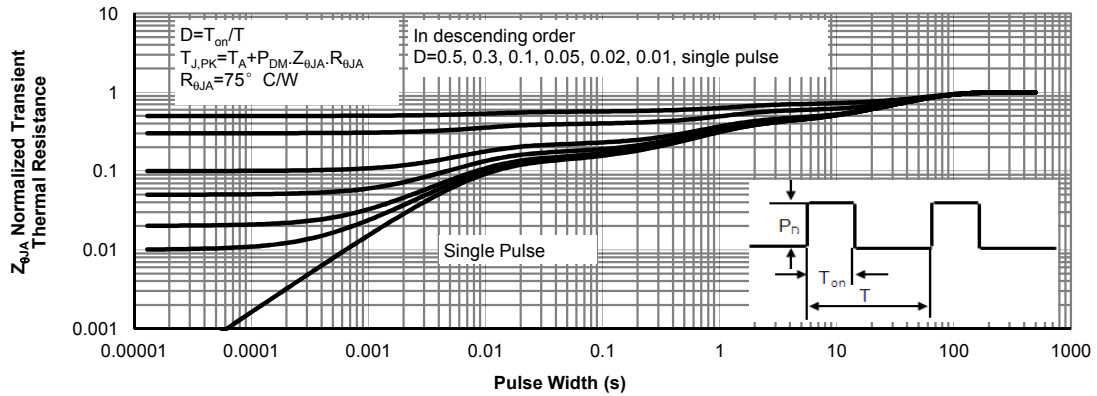
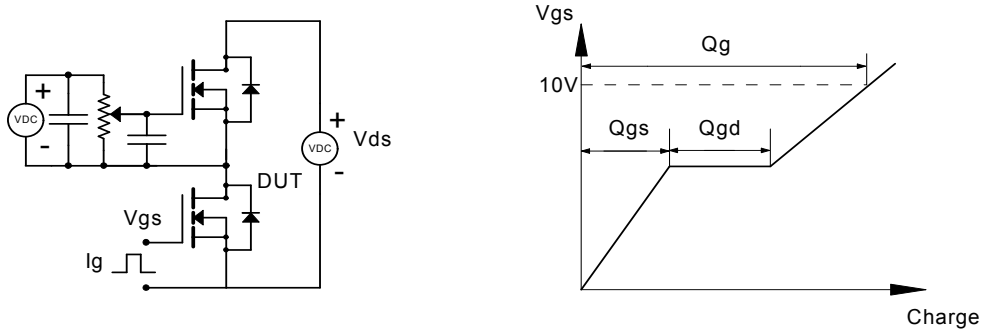
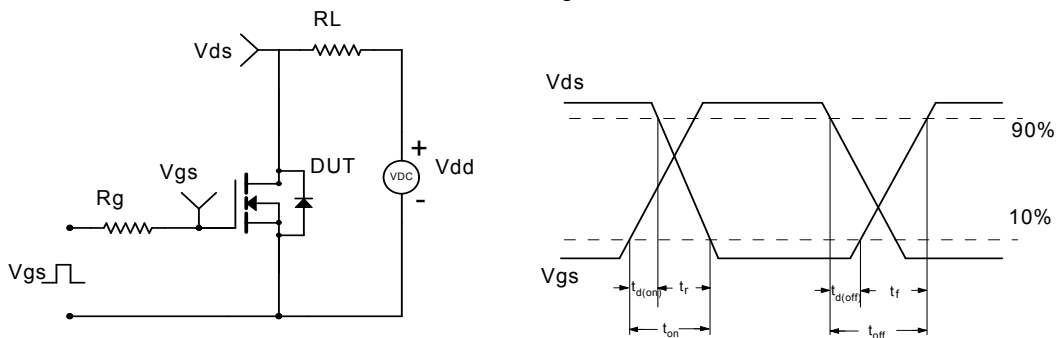


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

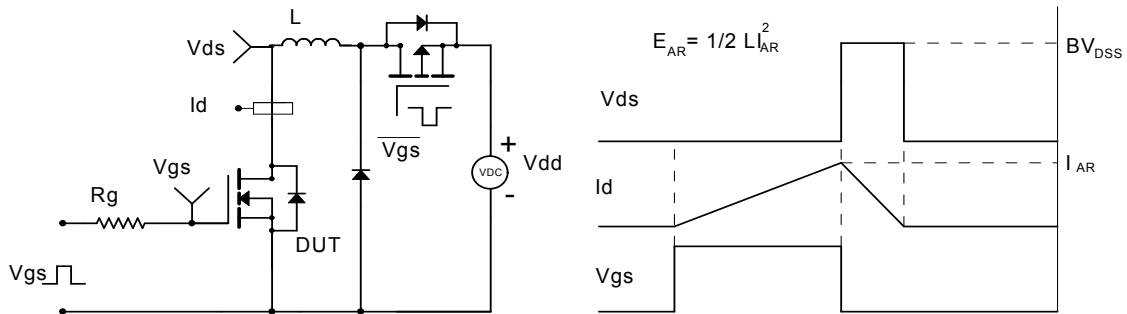
Gate Charge Test Circuit & Waveform



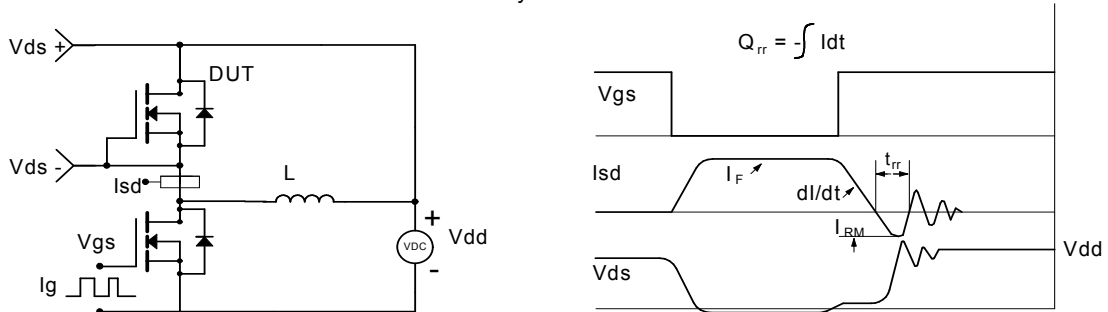
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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