

### General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Integrated Schottky Diode (SRFET)
- Very Low  $R_{DS(on)}$  at 4.5V<sub>GS</sub>
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

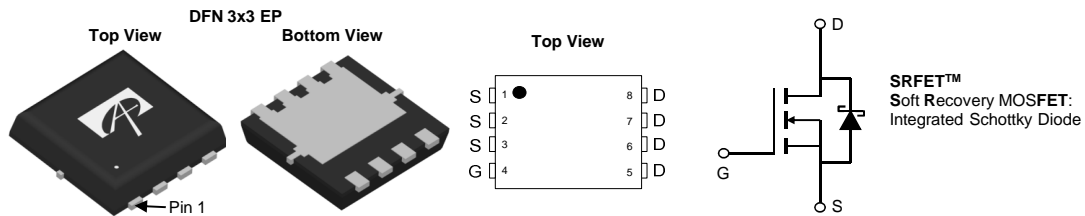
### Application

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

### Product Summary

$V_{DS}$	30V
$I_D$ (at $V_{GS}=10V$ )	16A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 8.2mΩ
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$ )	< 14.5mΩ

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	±20	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$	16
		$T_C=100^\circ\text{C}$	12
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	64	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	15
		$T_A=70^\circ\text{C}$	12
Avalanche Current <sup>C</sup>	$I_{AS}$	22	A
Avalanche energy $L=0.05\text{mH}$ <sup>C</sup>	$E_{AS}$	12	mJ
$V_{DS}$ Spike	$V_{SPIKE}$	36	V
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	20
		$T_C=100^\circ\text{C}$	8.3
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	30	40	°C/W
Maximum Junction-to-Ambient <sup>A,D</sup>		60	75	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	5	6	°C/W

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =10mA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			0.5 100	mA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.5	2	2.5	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =16A T <sub>J</sub> =125°C		6.8 9.8	8.2 12	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		11.6	14.5	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =16A		62		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =0.2A, V <sub>GS</sub> =0V		0.45	0.65	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				16	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance			605		pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		275		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			36.5		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1	2	3	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =16A		11	15	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			5.5	8	nC
Q <sub>gs</sub>	Gate Source Charge			2		nC
Q <sub>gd</sub>	Gate Drain Charge			2.6		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.9Ω, R <sub>GEN</sub> =3Ω		5		ns
t <sub>r</sub>	Turn-On Rise Time			2.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			17		ns
t <sub>f</sub>	Turn-Off Fall Time			3		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =16A, dI/dt=500A/μs		11.5		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =16A, dI/dt=500A/μs		12.5		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

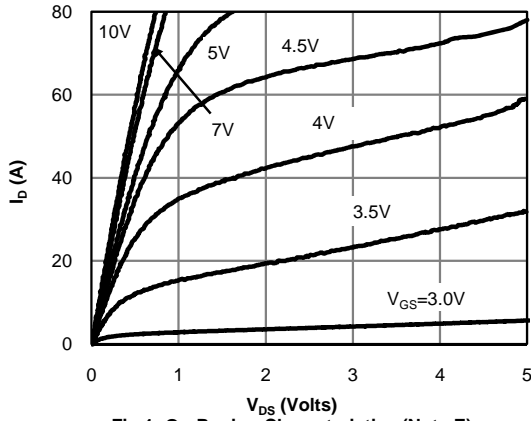
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

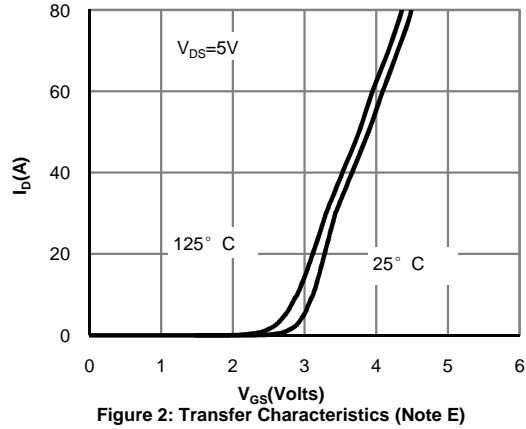
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

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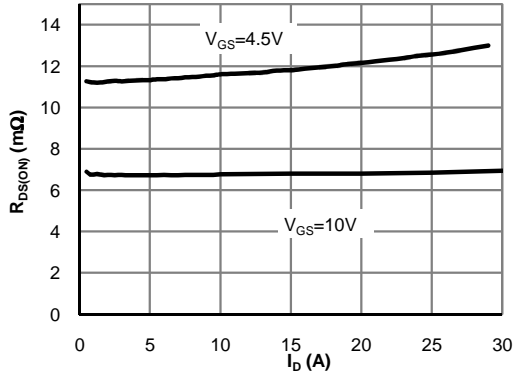
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



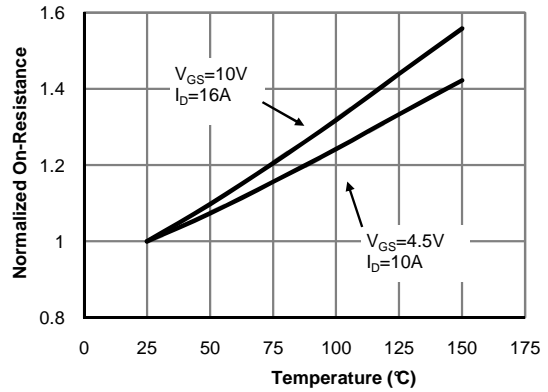
**Fig 1: On-Region Characteristics (Note E)**



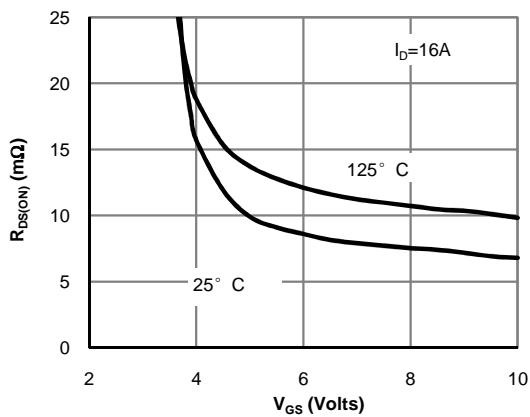
**Figure 2: Transfer Characteristics (Note E)**



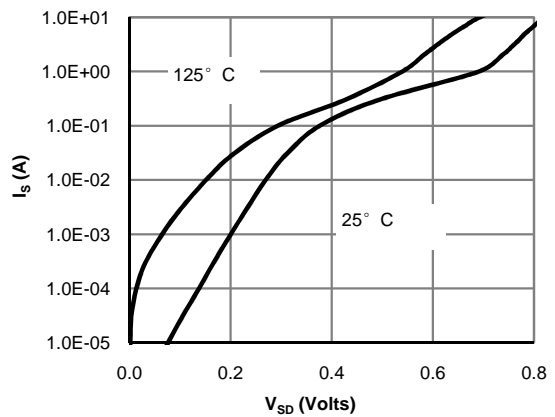
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

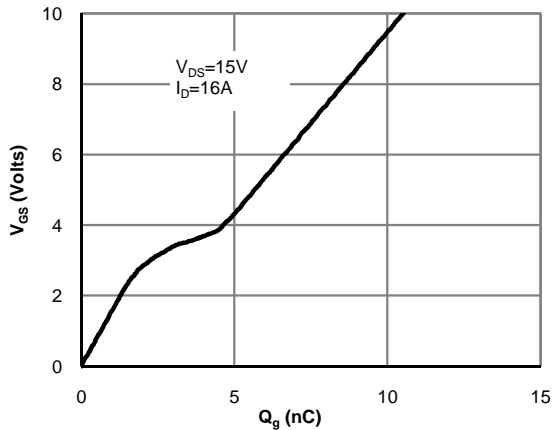


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

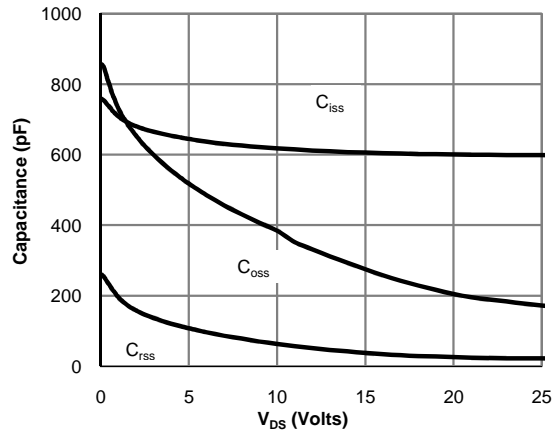


**Figure 6: Body-Diode Characteristics (Note E)**

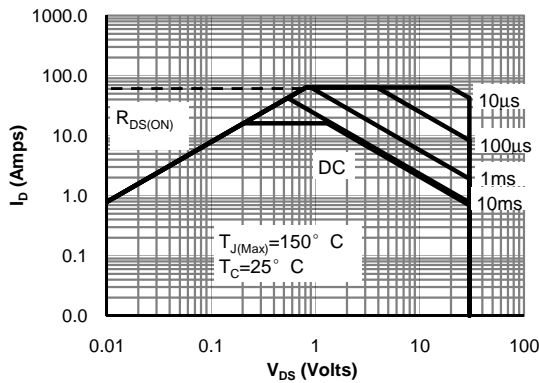
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



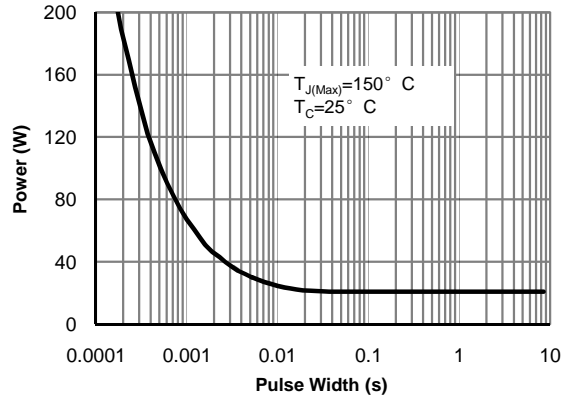
**Figure 7: Gate-Charge Characteristics**



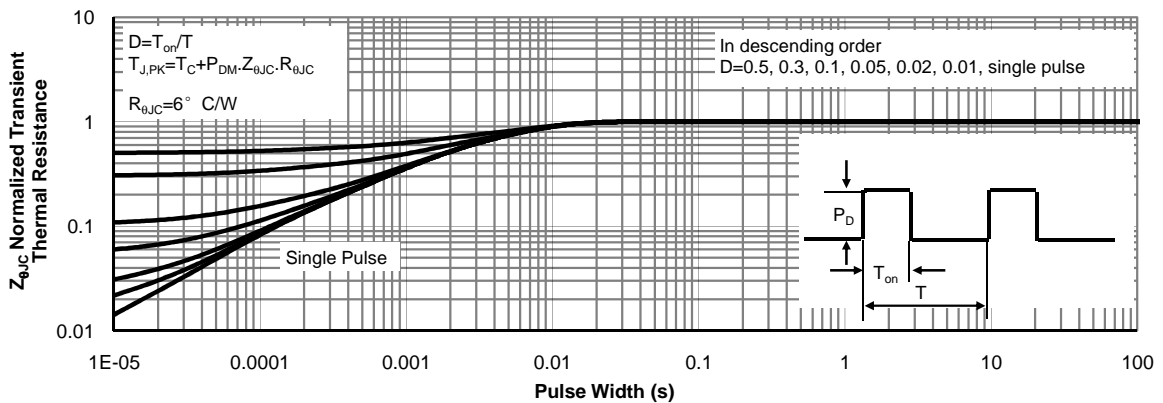
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

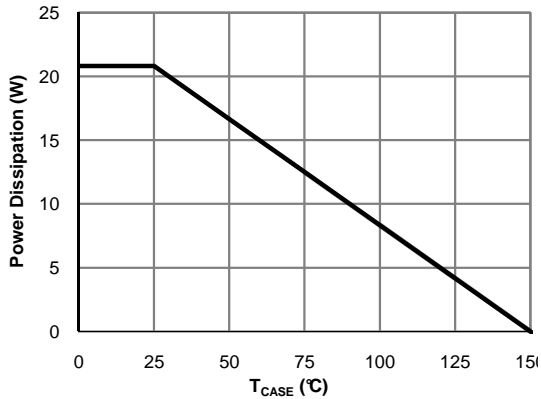


Figure 12: Power De-rating (Note F)

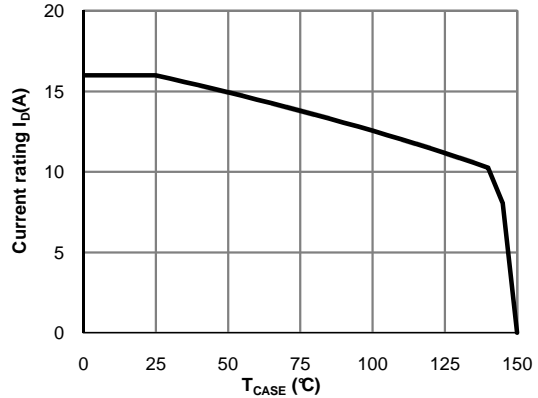


Figure 13: Current De-rating (Note F)

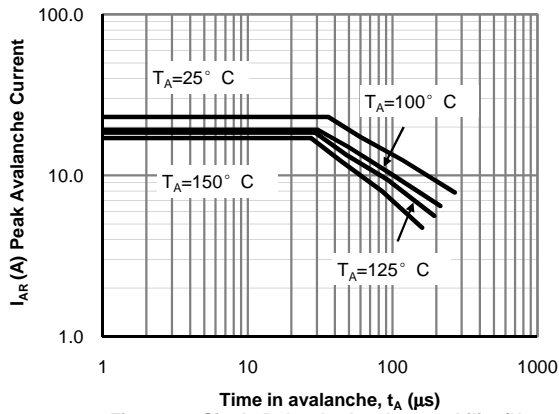


Figure 14: Single Pulse Avalanche capability (Note C)

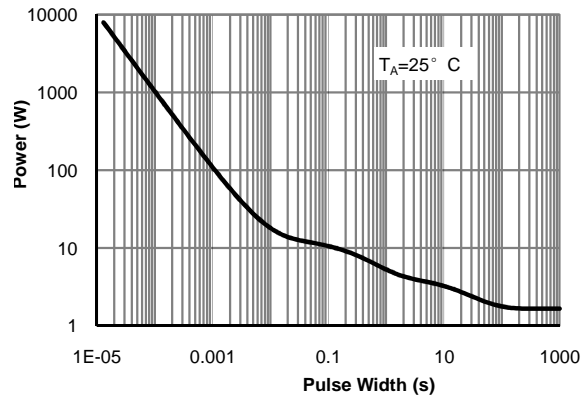


Figure 15: Single Pulse Power Rating Junction-to-Ambie (Note H)

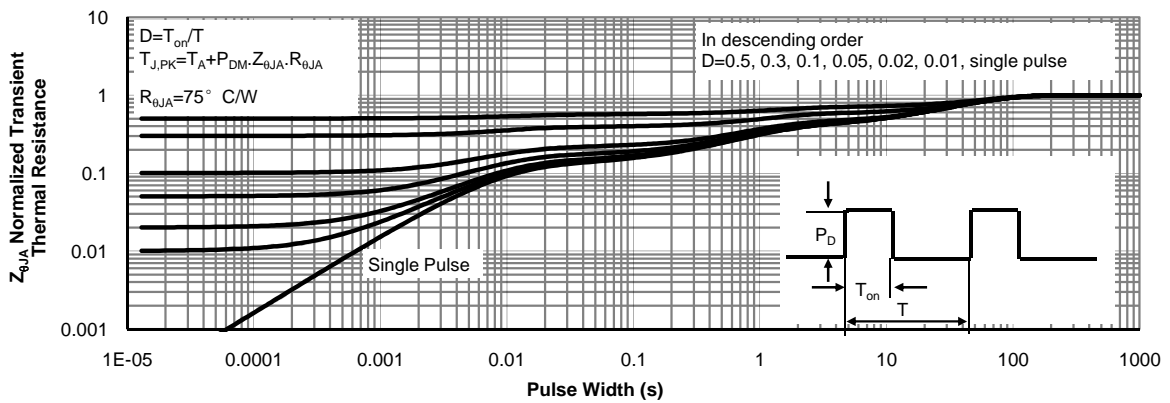


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

**Gate Charge Test Circuit & Waveform**



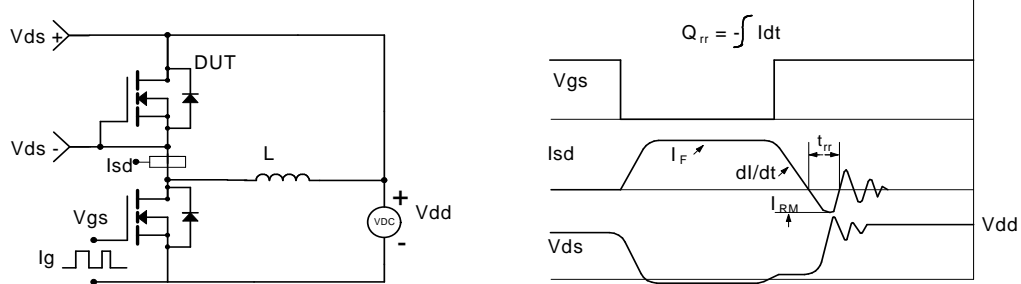
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



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