ALPHA & OMEGA SEMICONDUCTOR

# AON7932

## 30V Dual Asymmetric N-Channel MOSFET

### General Description

The AON7932 is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two specialized MOSFETs in a dual Power DFN3x3A package. The Q1 "High Side" MOSFET is designed to minimize switching losses. The Q2 "Low Side" MOSFET use advance trench technology with a monolithically integrated Schotty to provide excellent $R_{DS(ON)}$ and low gate charge. The AON7932 is well suited for use in compact DC/DC converter applications.

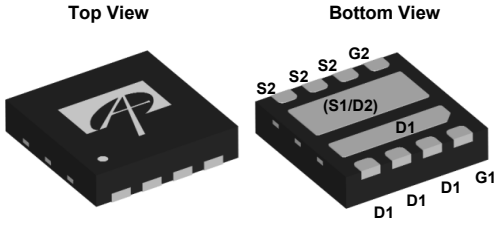
### Product Summary

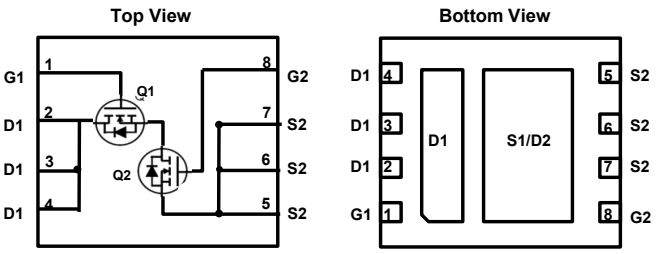
| | Q1 | Q2 |
|---|---|---|
| $V_{DS}$ | 30V | 30V |
| $I_D$ (at $V_{GS}$=10V) | 26A | 35A |
| $R_{DS(ON)}$ (at $V_{GS}$=10V) | <20mΩ | <12mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$ = 4.5V) | <30mΩ | <15mΩ |

100% UIS Tested
100% Rg Tested

Green Product

**Power DFN3x3A**




**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | Max Q1 | Max Q2 | Units |
|---|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 30 | | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | ±12 | V |
| Continuous Drain Current | $T_C$=25°C | $I_D$ | 26 | 35 | A |
| | $T_C$=100°C | | 16 | 22 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 70 | 110 | |
| Continuous Drain Current | $T_A$=25°C | $I_{DSM}$ | 6.6 | 8.1 | A |
| | $T_A$=70°C | | 5.3 | 6.5 | |
| Avalanche Current [C] | | $I_{AS}$, $I_{AR}$ | 18 | 17 | A |
| Avalanche Energy L=0.1mH [C] | | $E_{AS}$, $E_{AR}$ | 16 | 14 | mJ |
| Power Dissipation [B] | $T_C$=25°C | $P_D$ | 23 | 25 | W |
| | $T_C$=100°C | | 9 | 10 | |
| Power Dissipation [A] | $T_A$=25°C | $P_{DSM}$ | 1.4 | 1.4 | W |
| | $T_A$=70°C | | 0.9 | 0.9 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | | °C |

**Thermal Characteristics**

| Parameter | | Symbol | Typ Q1 | Max Q1 | Typ Q2 | Max Q2 | Units |
|---|---|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 40 | 50 | 40 | 50 | °C/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 70 | 90 | 70 | 90 | °C/W |
| Maximum Junction-to-Case | Steady-State | $R_{\theta JC}$ | 4.5 | 5.4 | 4.2 | 5 | °C/W |

**Q1 Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=30V, $V_{GS}$=0V | | | 1 | µA |
| | | $T_J$=55°C | | | 5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±20V | | | 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250µA | 1.4 | 1.9 | 2.4 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 70 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=6.6A | | 16 | 20 | mΩ |
| | | $T_J$=125°C | | 24 | 29 | |
| | | $V_{GS}$=4.5V, $I_D$=5.3A | | 23 | 30 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=6.6A | | 22 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.75 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 20 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=15V, f=1MHz | 300 | 380 | 460 | pF |
| $C_{oss}$ | Output Capacitance | | 110 | 160 | 210 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 7 | 13 | 22 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 0.7 | 1.5 | 2.3 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=15V, $I_D$=6.6A | | 5.4 | 6.5 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 2.3 | | nC |
| $Q_{gs}$ | Gate Source Charge | | | 1.3 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 1 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=15V, $R_L$=2.3Ω, $R_{GEN}$=3Ω | | 10 | | ns |
| $t_r$ | Turn-On Rise Time | | | 3 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 15 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 5 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=6.6A, dI/dt=500A/µs | 6.8 | 8.5 | 10.2 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=6.6A, dI/dt=500A/µs | 12.8 | 16 | 19.2 | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial $T_J$ =25° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with TA=25° C.

## Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

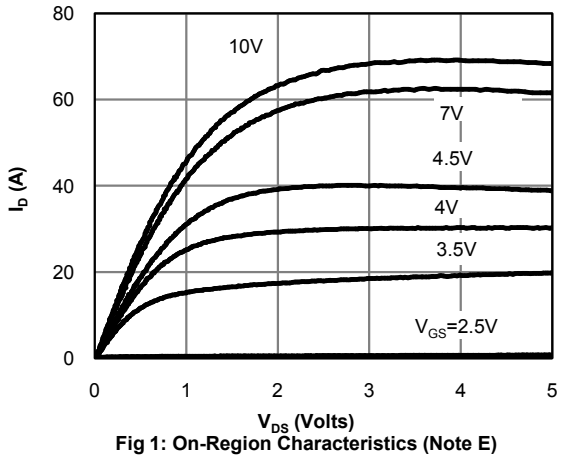



Fig 1: On-Region Characteristics (Note E)

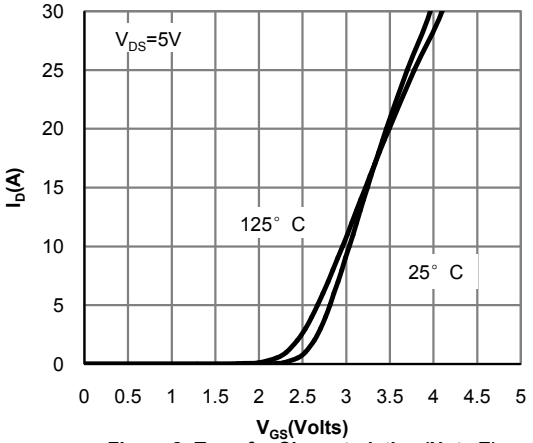



Figure 2: Transfer Characteristics (Note E)

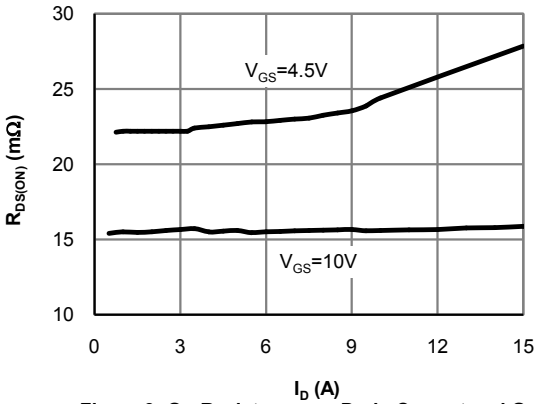



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

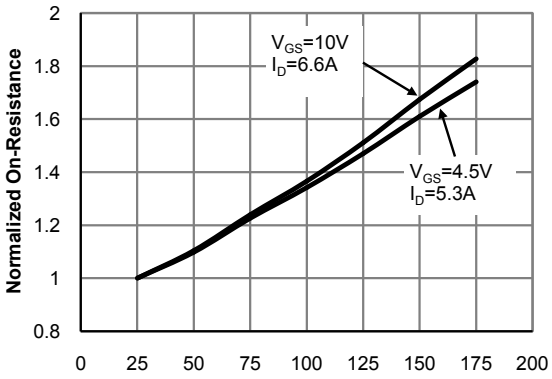



Figure 4: On-Resistance vs. Junction Temperature (Note E)

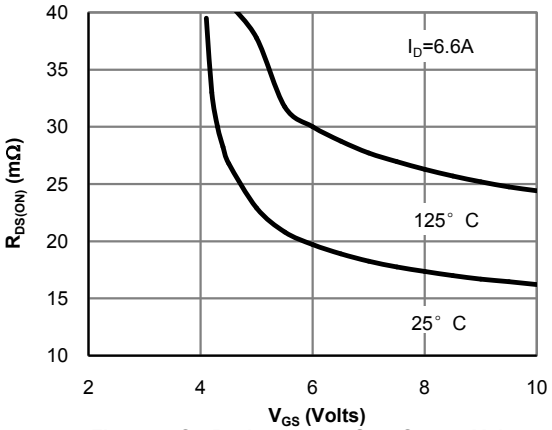



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

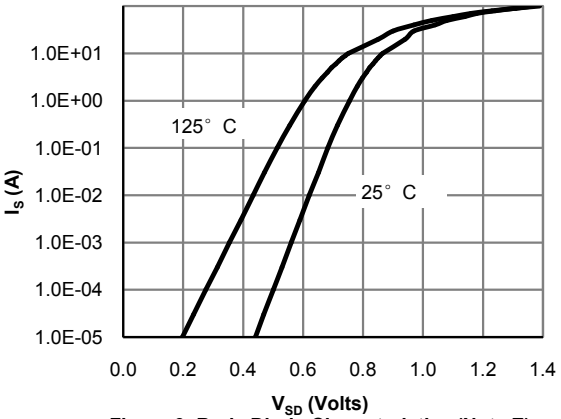



Figure 6: Body-Diode Characteristics (Note E)

## Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

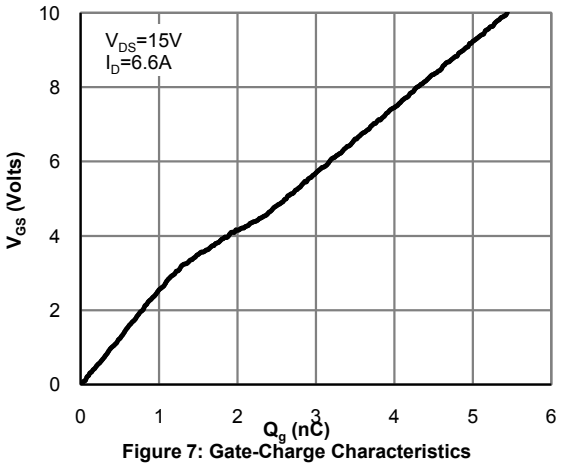



Figure 7: Gate-Charge Characteristics

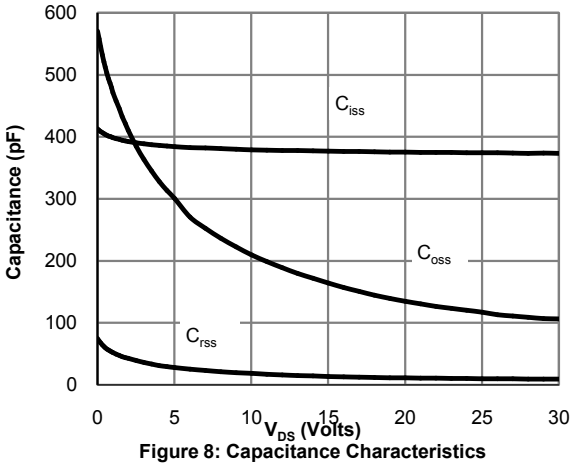



Figure 8: Capacitance Characteristics

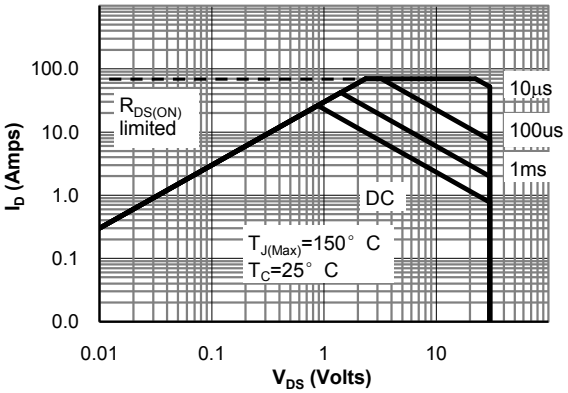



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

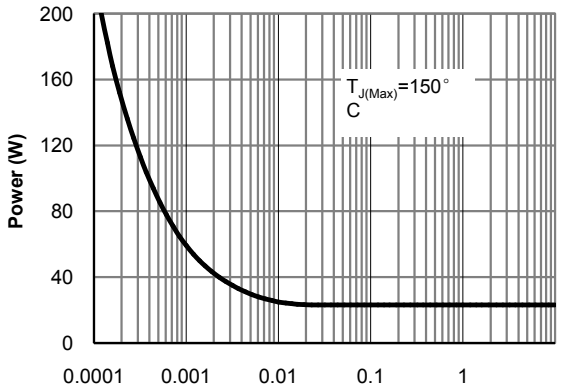



Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

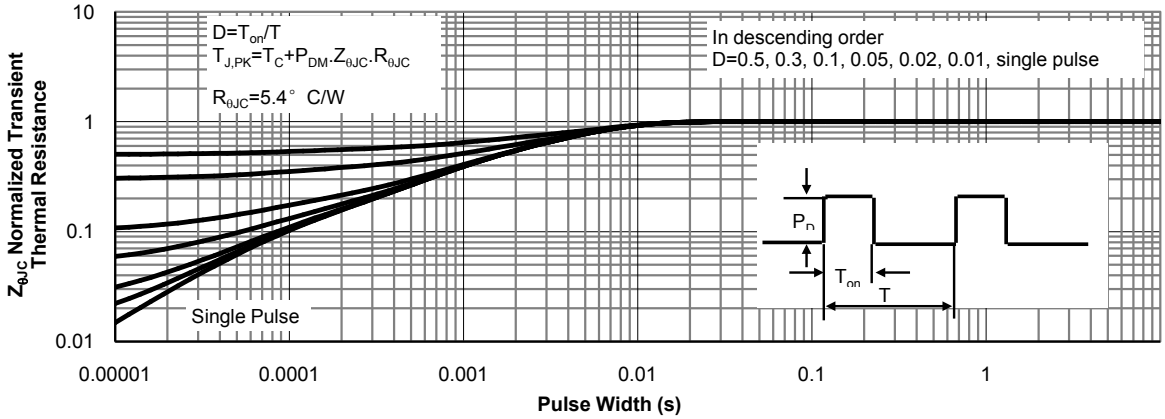



Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

## Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

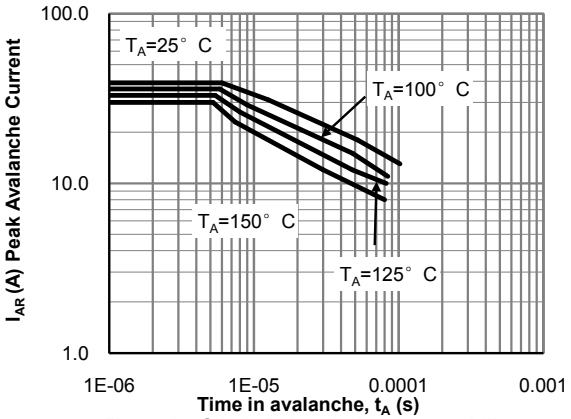



**Figure 12: Single Pulse Avalanche capability (Note C)**

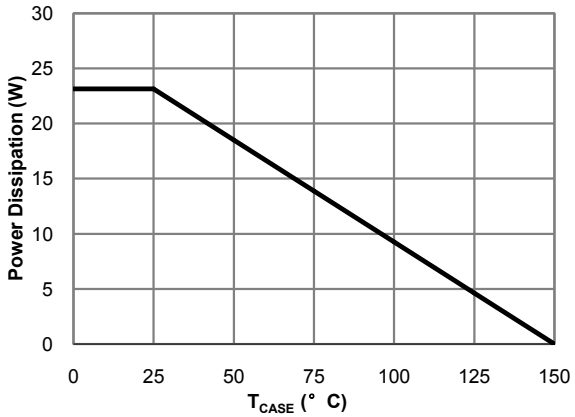



**Figure 13: Power De-rating (Note F)**

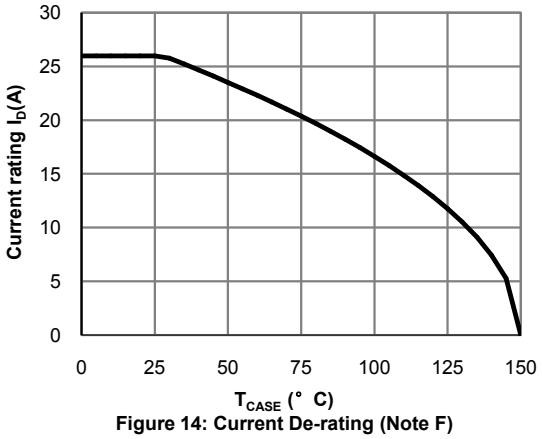



**Figure 14: Current De-rating (Note F)**

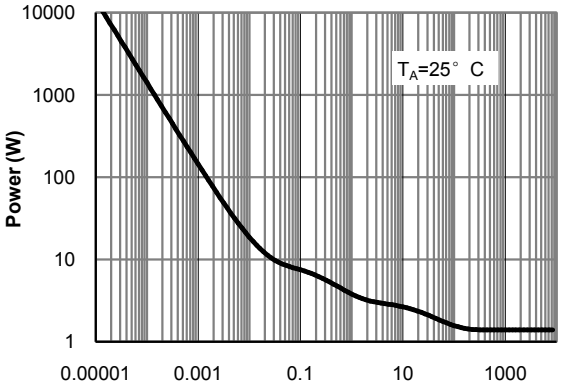



**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

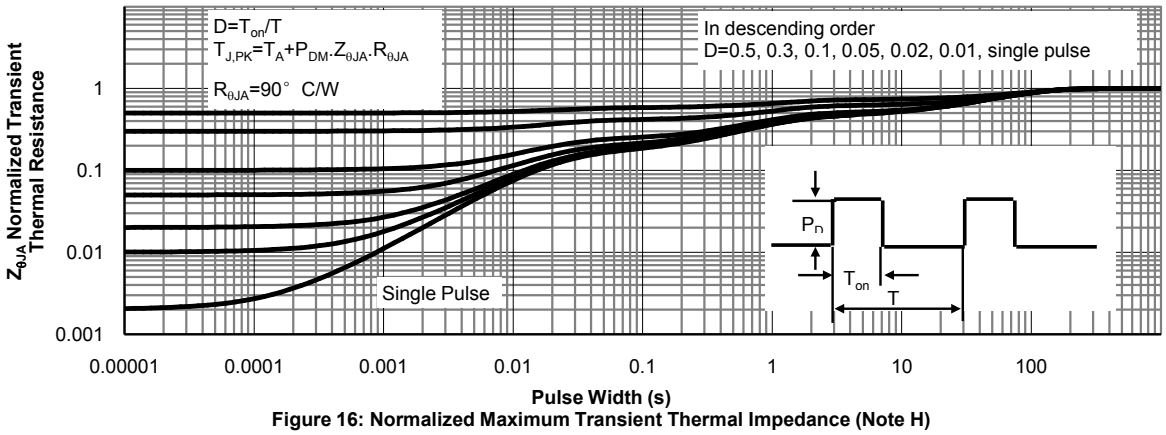



**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

**Q2 Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=10mA, $V_{GS}$=0V | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=30V, $V_{GS}$=0V | | | 0.5 | mA |
| | | $T_J$=55°C | | | 500 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±12V | | | 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250µA | 1.1 | 1.6 | 2.1 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 110 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=8.1A | | 10 | 12 | mΩ |
| | | $T_J$=125°C | | 15 | 18 | |
| | | $V_{GS}$=4.5V, $I_D$=6.5A | | 12 | 15 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=8.1A | | 55 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.45 | 0.7 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 30 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=15V, f=1MHz | 810 | 1020 | 1230 | pF |
| $C_{oss}$ | Output Capacitance | | 77 | 111 | 150 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 45 | 75 | 130 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 0.5 | 1 | 1.5 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=15V, $I_D$=8.1A | | 19 | 23 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 9 | | nC |
| $Q_{gs}$ | Gate Source Charge | | | 4 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 3 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=15V, $R_L$=1.8Ω, $R_{GEN}$=3Ω | | 11 | | ns |
| $t_r$ | Turn-On Rise Time | | | 5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 29 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 6 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=8.1A, dI/dt=500A/µs | 4 | 5.4 | 7 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=8.1A, dI/dt=500A/µs | 4 | 5.3 | 7 | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial $T_J$ =25° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25° C.

## Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

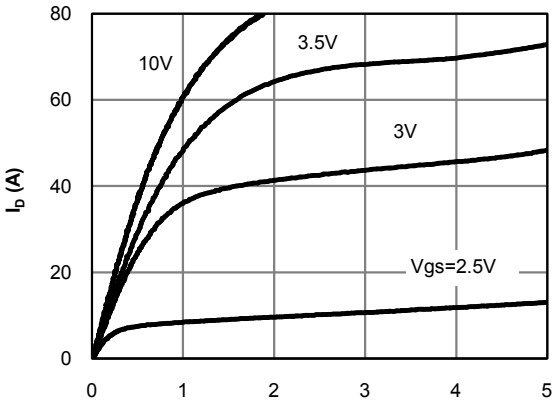



Fig 1: On-Region Characteristics (Note E)

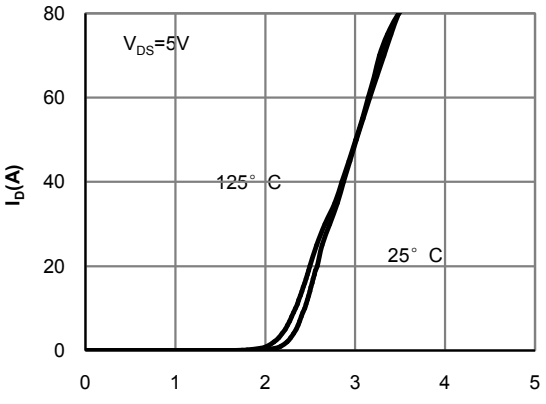



Figure 2: Transfer Characteristics (Note E)

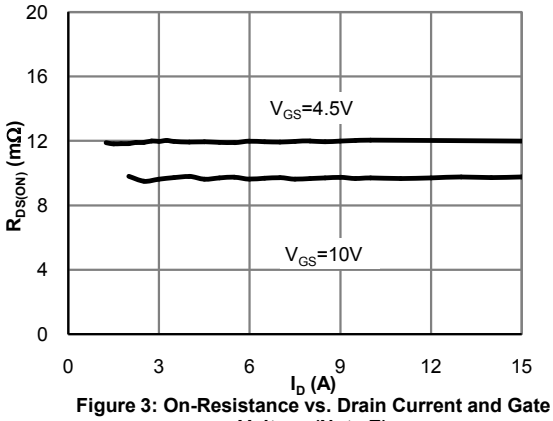



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

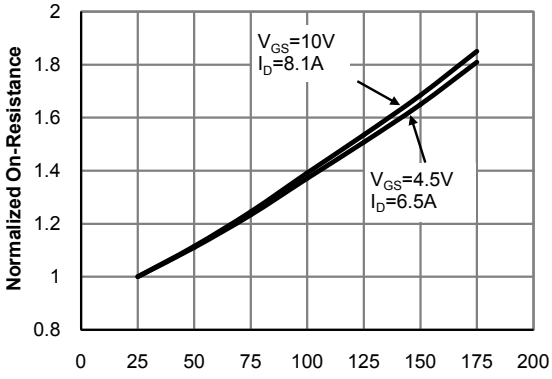



Figure 4: On-Resistance vs. Junction Temperature (Note E)

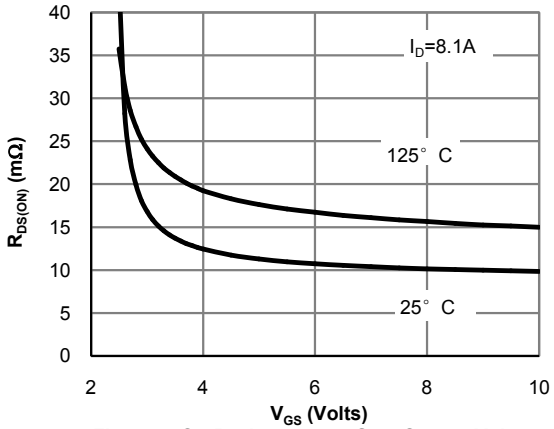



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

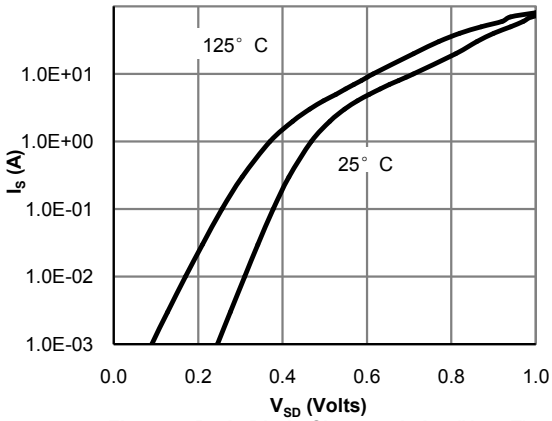



Figure 6: Body-Diode Characteristics (Note E)

## Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

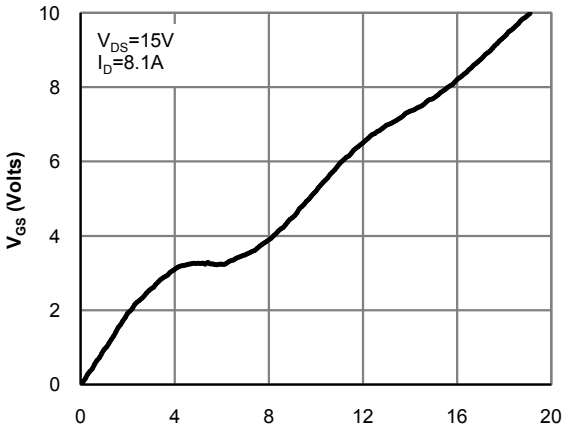



Figure 7: Gate-Charge Characteristics

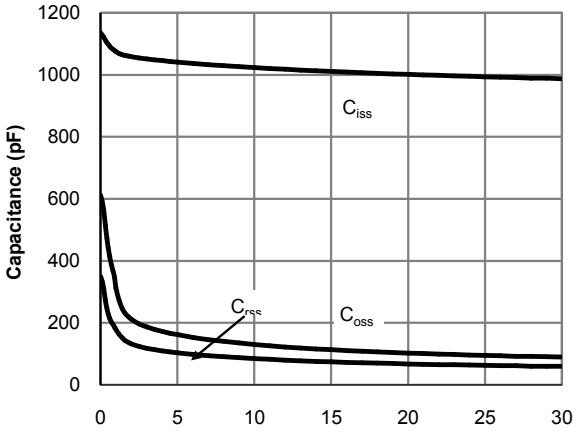



Figure 8: Capacitance Characteristics

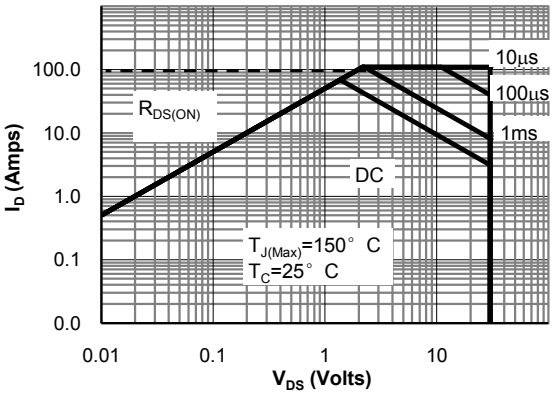



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

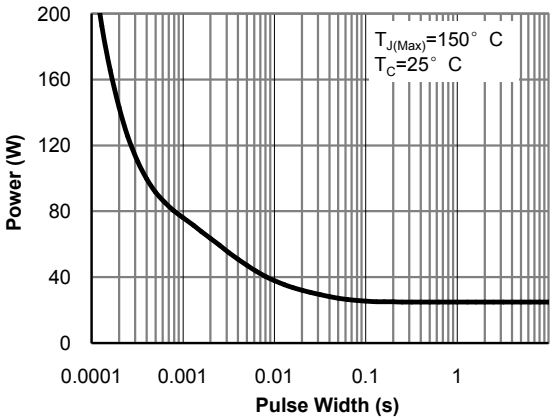



Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

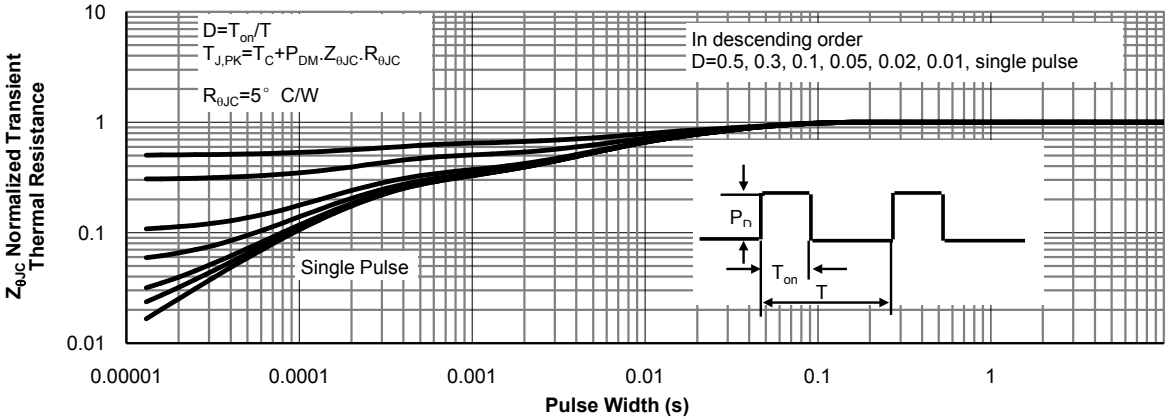



Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

## Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

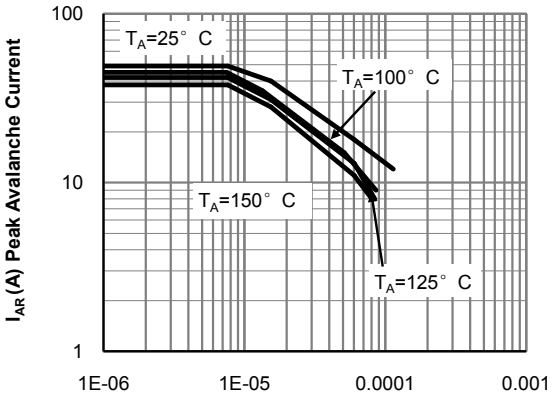



**Figure 12: Single Pulse Avalanche capability (Note C)**

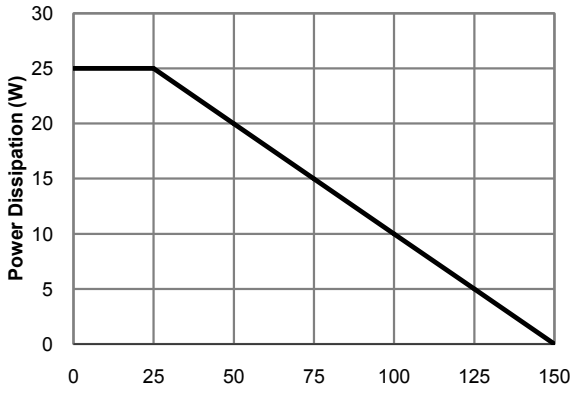



**Figure 13: Power De-rating (Note F)**

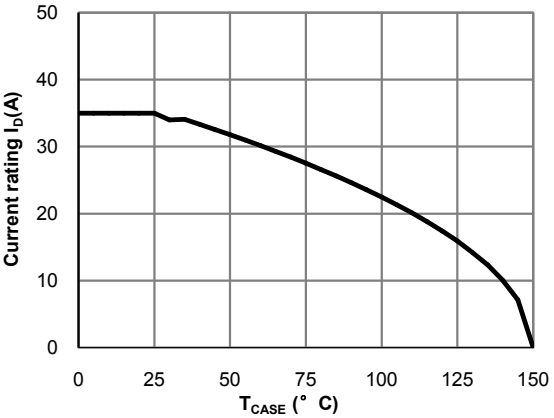



**Figure 14: Current De-rating (Note F)**

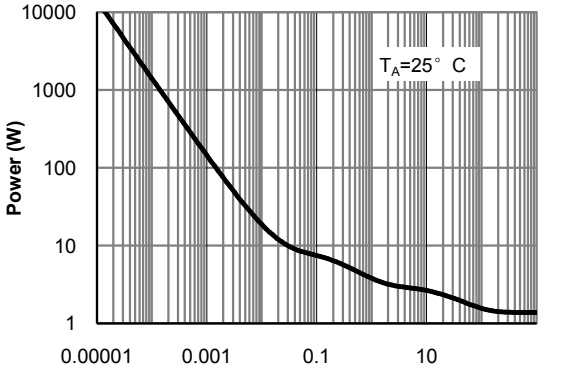



**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)**

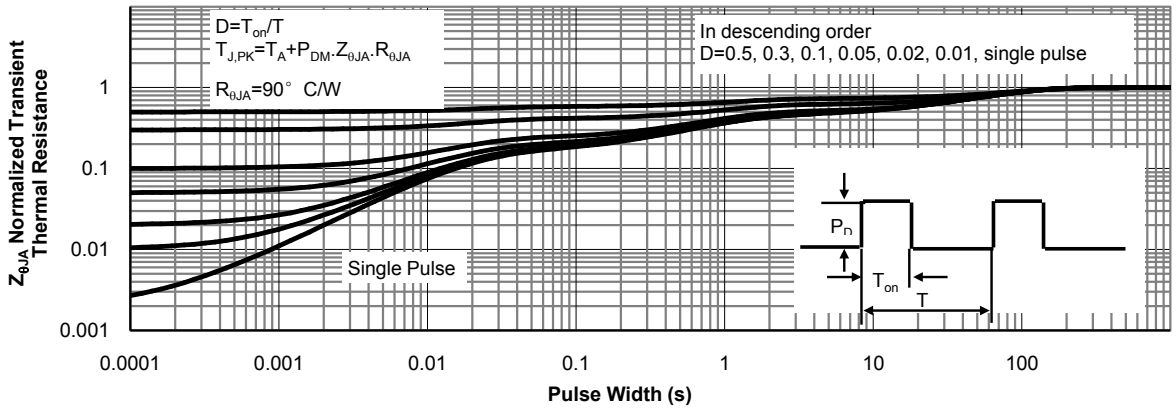



**Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)**

## Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

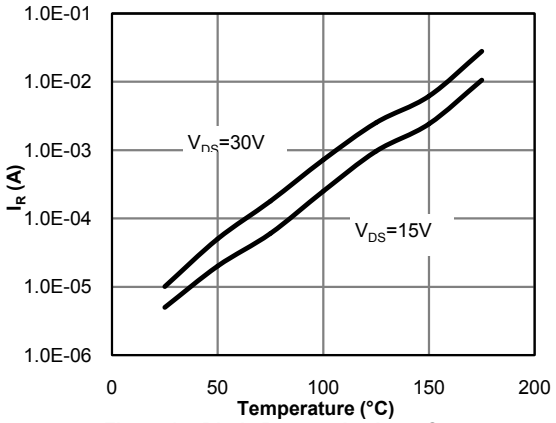



**Figure 17: Diode Reverse Leakage Current vs. Junction Temperature**

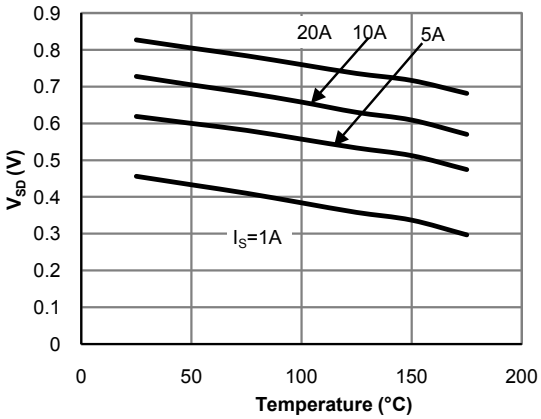



**Figure 18: Diode Forward voltage vs. Junction Temperature**

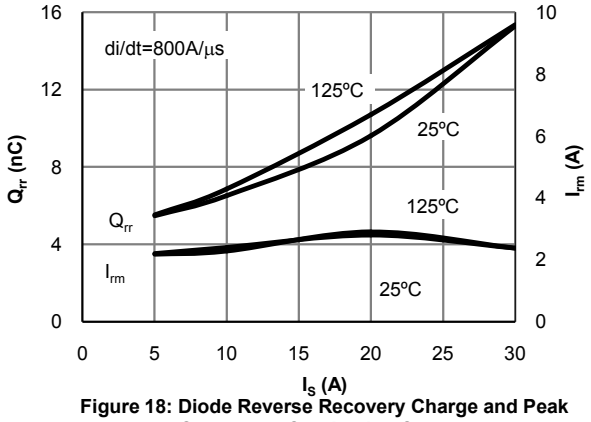



**Figure 18: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current**

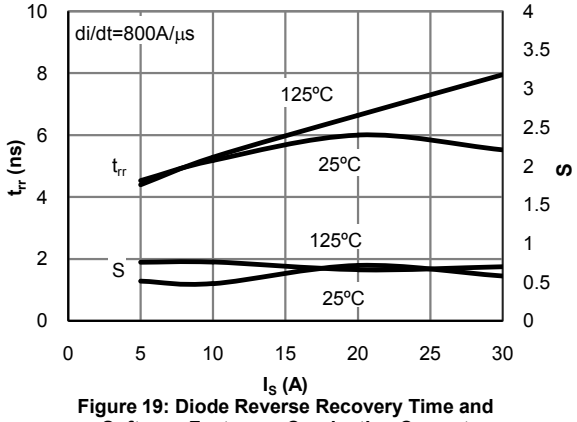



**Figure 19: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current**

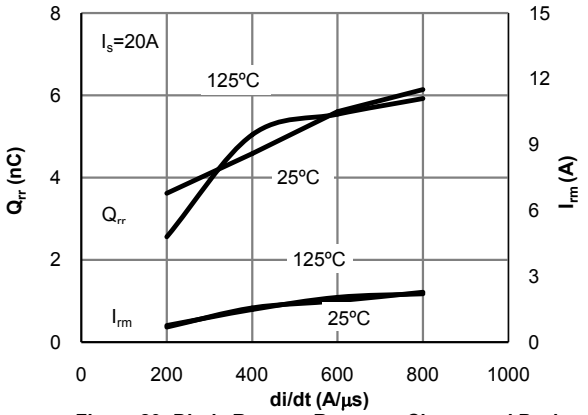



**Figure 20: Diode Reverse Recovery Charge and Peak Current vs. di/dt**

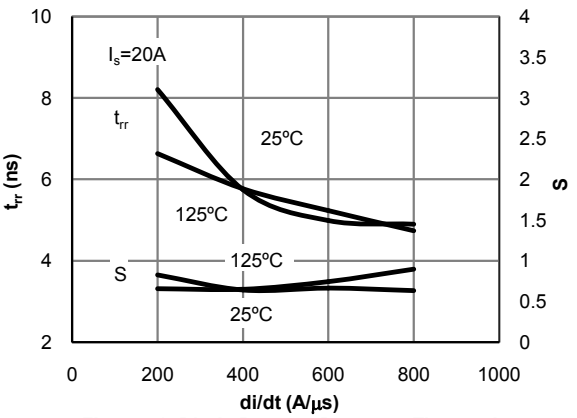
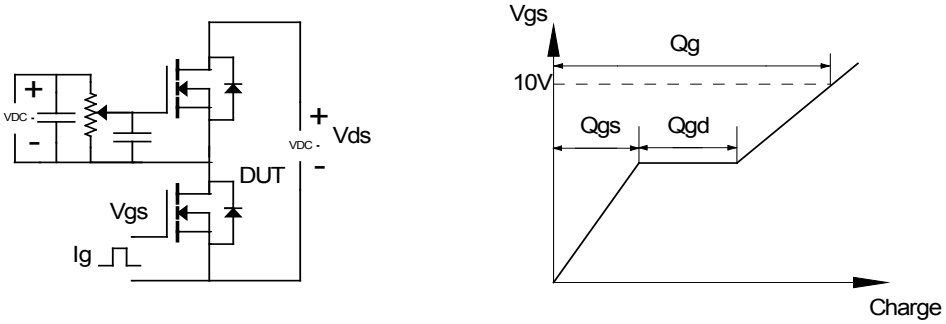
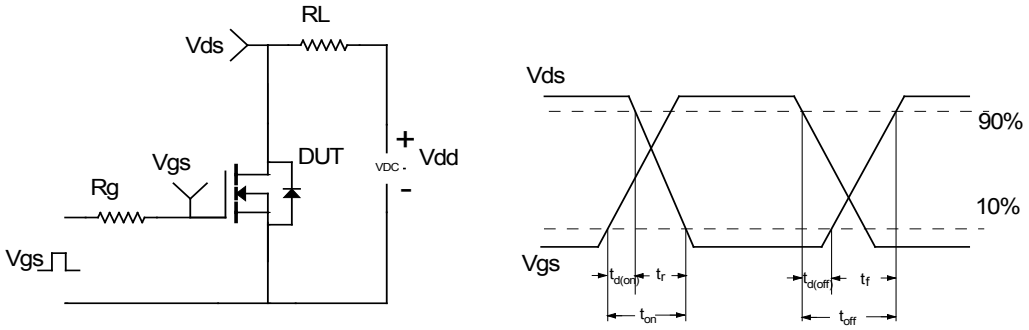



**Figure 21: Diode Reverse Recovery Time and Softness Factor vs. di/dt**

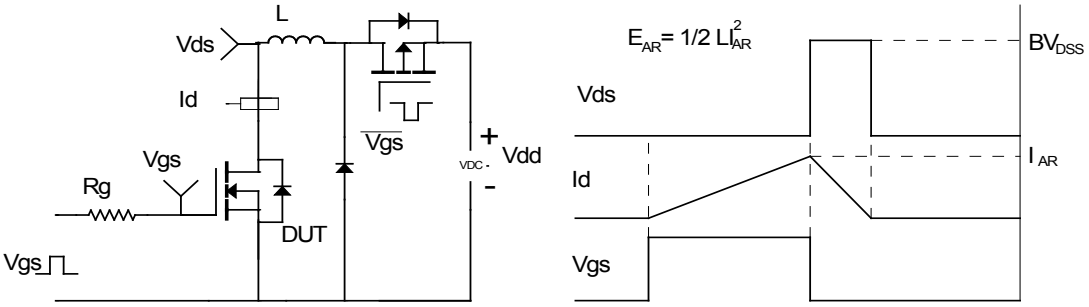
## Gate Charge Test Circuit & Waveform



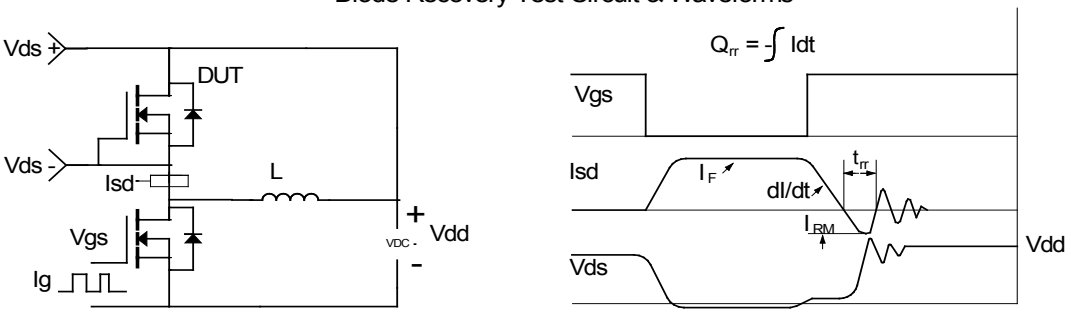

## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms



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