
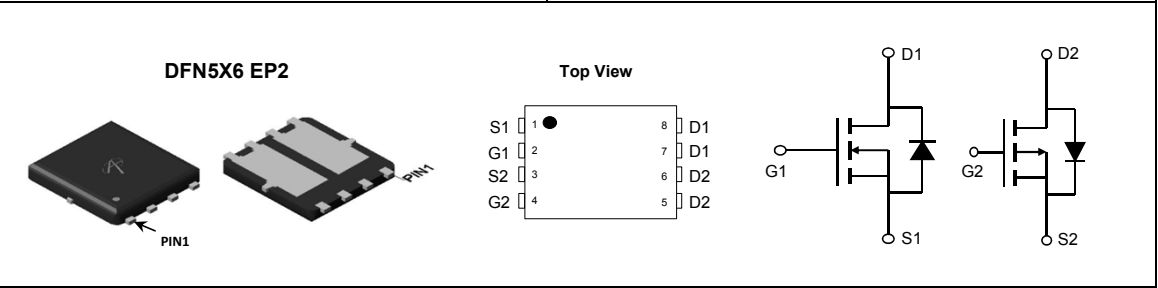


<p><b>General Description</b></p> <ul style="list-style-type: none"> <li>• Pch+Nch Complementary MOSFET</li> <li>• Trench Power MOSFET</li> <li>• Low <math>R_{DS(ON)}</math></li> <li>• Low Gate Charge</li> <li>• Excellent Thermal Performance</li> <li>• RoHS and Halogen Free Compliant</li> </ul> <p><b>Applications</b></p> <ul style="list-style-type: none"> <li>• Motor Drive</li> <li>• DC-FAN</li> </ul>	<p><b>Product Summary</b></p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th style="text-align: center;"><u>Q1</u></th> <th style="text-align: center;"><u>Q2</u></th> </tr> </thead> <tbody> <tr> <td><math>V_{DS}</math></td> <td style="text-align: center;">30V</td> <td style="text-align: center;">-30V</td> </tr> <tr> <td><math>I_D</math> (at <math>V_{GS}=10V</math>)</td> <td style="text-align: center;">16A</td> <td style="text-align: center;">-16A</td> </tr> <tr> <td><math>R_{DS(ON)}</math> (at <math>V_{GS}=10V</math>)</td> <td style="text-align: center;">&lt; 14m<math>\Omega</math></td> <td style="text-align: center;">&lt; 12m<math>\Omega</math></td> </tr> <tr> <td><math>R_{DS(ON)}</math> (at <math>V_{GS}=4.5V</math>)</td> <td style="text-align: center;">&lt; 18m<math>\Omega</math></td> <td style="text-align: center;">&lt; 19.5m<math>\Omega</math></td> </tr> </tbody> </table> <p>100% UIS Tested 100% Rg Tested</p> <div style="text-align: right;">  </div>		<u>Q1</u>	<u>Q2</u>	$V_{DS}$	30V	-30V	$I_D$ (at $V_{GS}=10V$ )	16A	-16A	$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 14m $\Omega$	< 12m $\Omega$	$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	< 18m $\Omega$	< 19.5m $\Omega$
	<u>Q1</u>	<u>Q2</u>														
$V_{DS}$	30V	-30V														
$I_D$ (at $V_{GS}=10V$ )	16A	-16A														
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 14m $\Omega$	< 12m $\Omega$														
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	< 18m $\Omega$	< 19.5m $\Omega$														



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOND32324	DFN 5x6	Tape & Reel	3000

**Absolute Maximum Ratings**  $T_A=25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage	$V_{DS}$	30	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 25$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$ 16	-16	A
Current <sup>G</sup>		$T_C=100^\circ\text{C}$ 16	-16	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	50	-65	
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$ 13	-15	A
Current		$T_A=70^\circ\text{C}$ 10	-12	
Avalanche Current <sup>C</sup>	$I_{AS}$	22	33	A
Avalanche energy	$E_{AS}$	24	54	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$ 12.5	30	W
		$T_C=100^\circ\text{C}$ 5	12	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$ 3.5	4.1	W
		$T_A=70^\circ\text{C}$ 2.2	2.6	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		°C

**Thermal Characteristics**

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10s$ 25	20	35	30	°C/W
Maximum Junction-to-Ambient <sup>A,B</sup>		Steady-State 50	48	70	65	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	7	3.5	10	4.2	°C/W

**Q1 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.5	1.9	2.5	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =12A T <sub>J</sub> =125°C		11 16	14 20	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		14	18	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =12A		43		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.75	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				10	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		760		pF
C <sub>oss</sub>	Output Capacitance			125		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			70		pF
R <sub>g</sub>	Gate resistance	f=1MHz	0.8	1.6	2.4	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =12A		14	20	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			6.6	10	nC
Q <sub>gs</sub>	Gate Source Charge			2.4		nC
Q <sub>gd</sub>	Gate Drain Charge			3		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =1.25Ω, R <sub>GEN</sub> =3Ω		4.4		ns
t <sub>r</sub>	Turn-On Rise Time			9		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			17		ns
t <sub>f</sub>	Turn-Off Fall Time			6		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =12A, di/dt=500A/μs		7		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =12A, di/dt=500A/μs		8		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

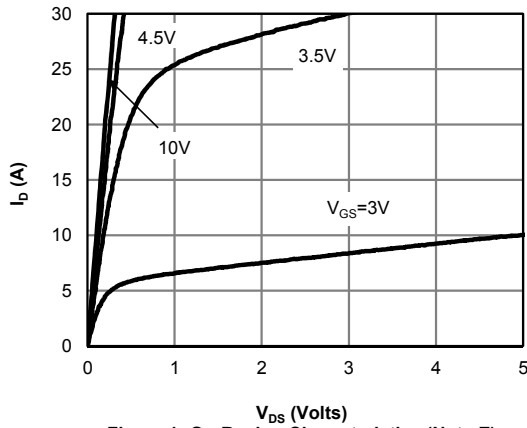


Figure 1: On-Region Characteristics (Note E)

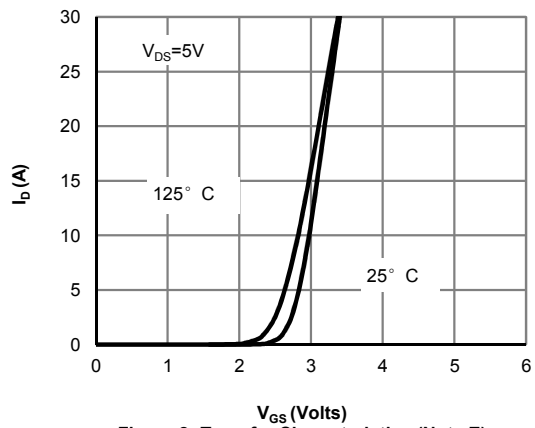


Figure 2: Transfer Characteristics (Note E)

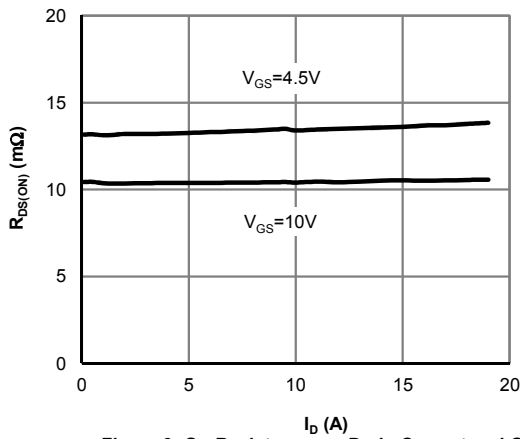


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

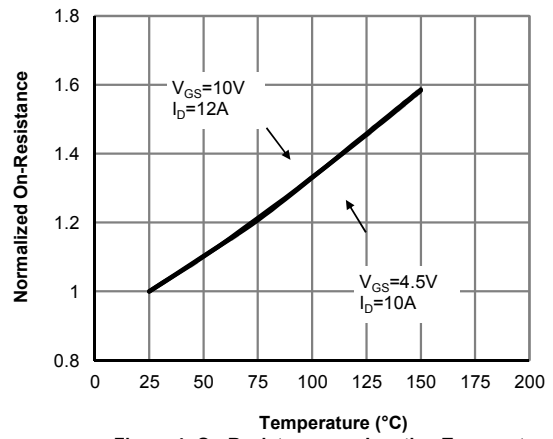


Figure 4: On-Resistance vs. Junction Temperature (Note E)

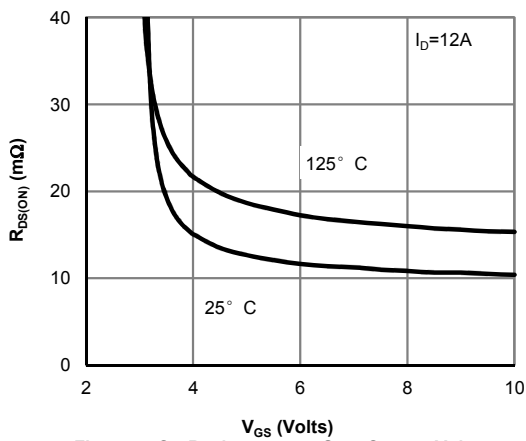


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

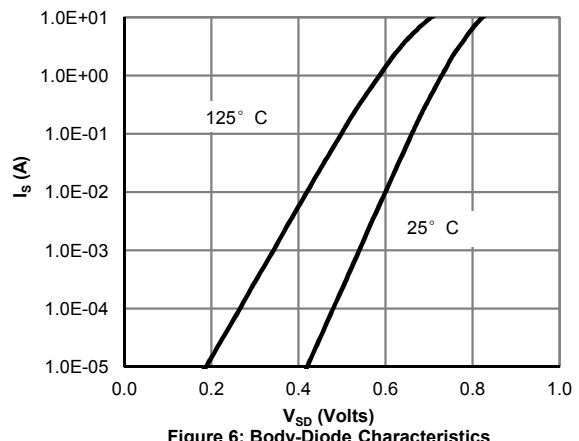


Figure 6: Body-Diode Characteristics (Note E)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

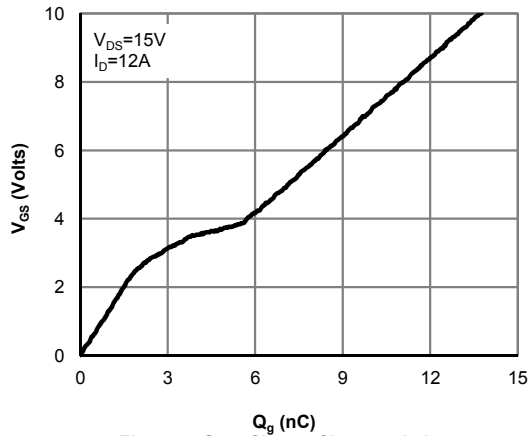


Figure 7: Gate-Charge Characteristics

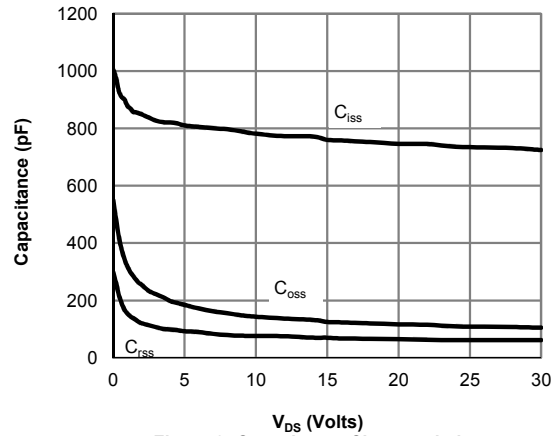


Figure 8: Capacitance Characteristics

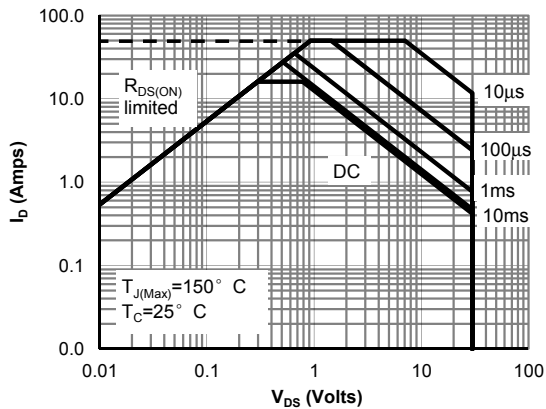


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

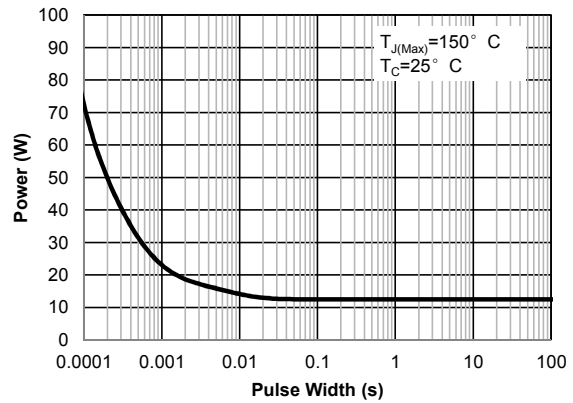


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

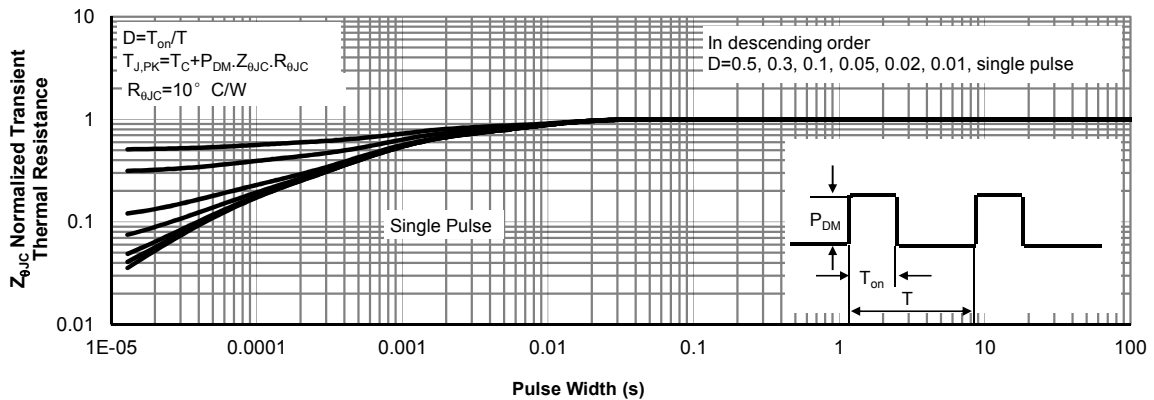


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

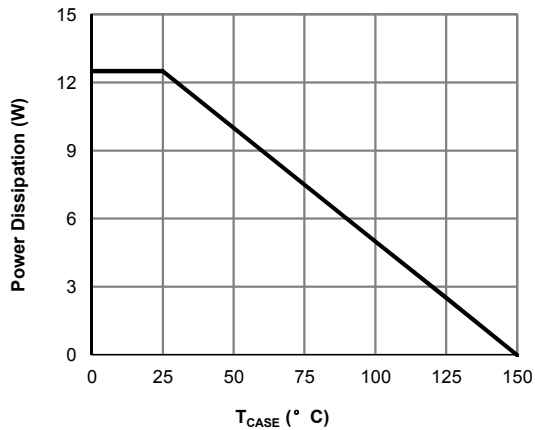


Figure 12: Power De-rating (Note F)

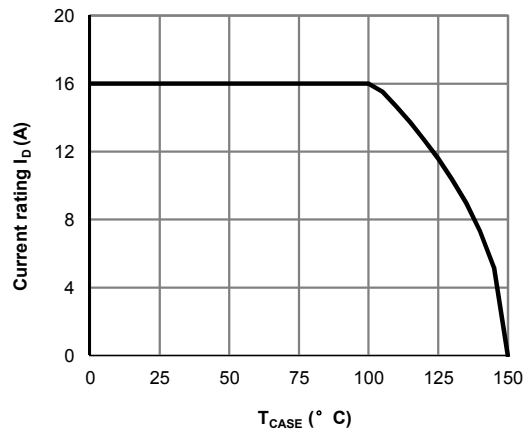


Figure 13: Current De-rating (Note F)

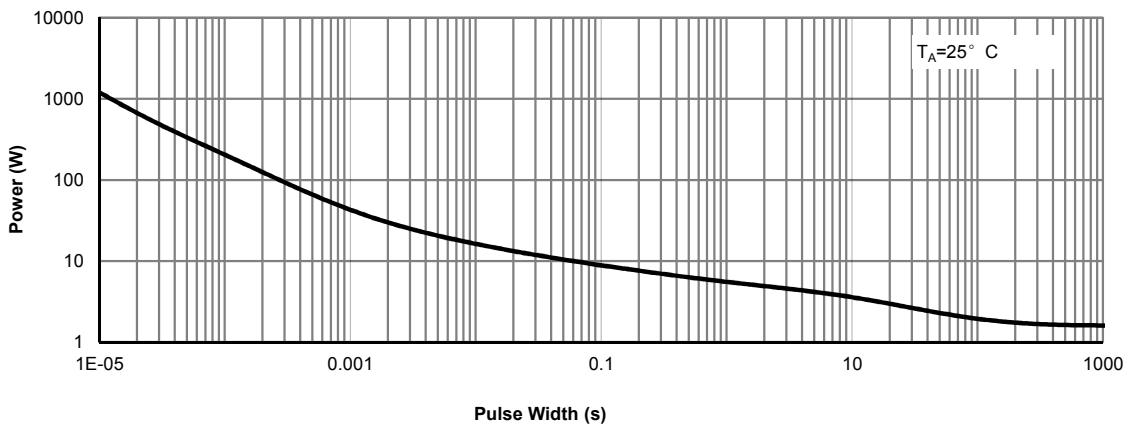


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

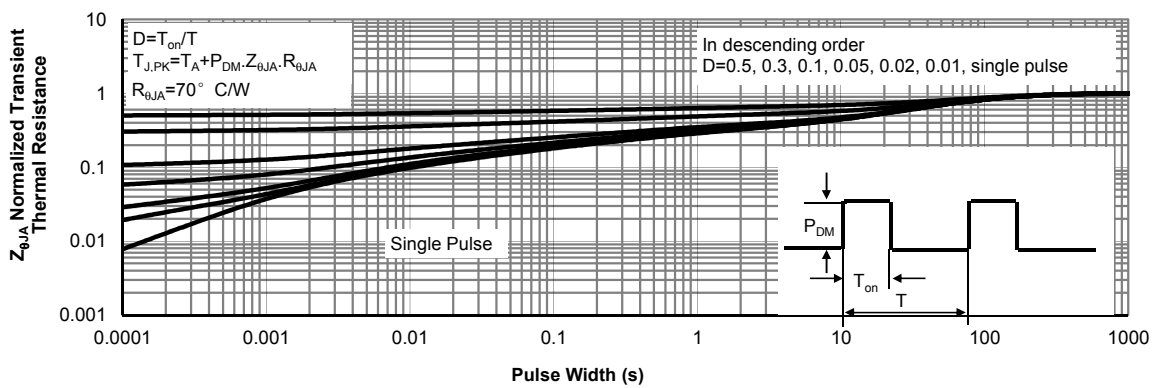


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

**Q2 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±25V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.3	-1.8	-2.3	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-16A T <sub>J</sub> =125°C		10 14	12 16.8	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-12A		15.4	19.5	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-16A		43		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.7	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				-16	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz		1995		pF
C <sub>oss</sub>	Output Capacitance			300		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			260		pF
R <sub>g</sub>	Gate resistance	f=1MHz		4.5	9	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-16A		35	50	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			17	25	nC
Q <sub>gs</sub>	Gate Source Charge			5.7		nC
Q <sub>gd</sub>	Gate Drain Charge			8.8		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =0.9Ω, R <sub>GEN</sub> =3Ω		11		ns
t <sub>r</sub>	Turn-On Rise Time			7.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			43.5		ns
t <sub>f</sub>	Turn-Off Fall Time			17.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-16A, di/dt=500A/μs		13.3		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-16A, di/dt=500A/μs		20		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

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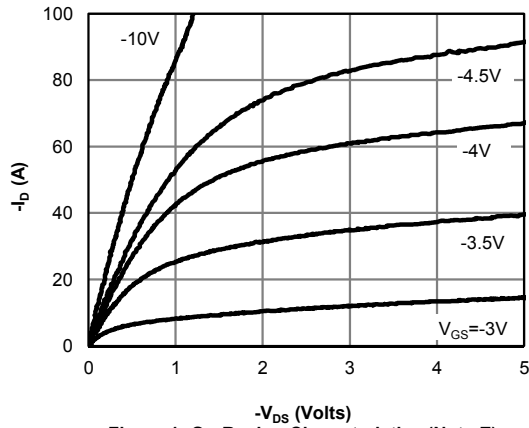


Figure 1: On-Region Characteristics (Note E)

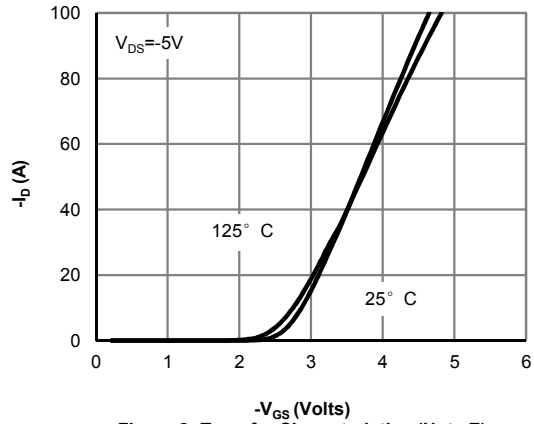


Figure 2: Transfer Characteristics (Note E)

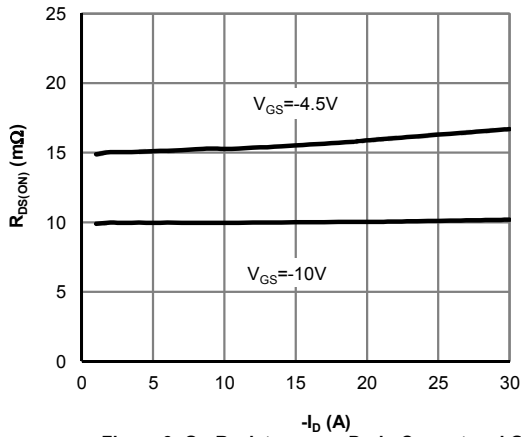


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

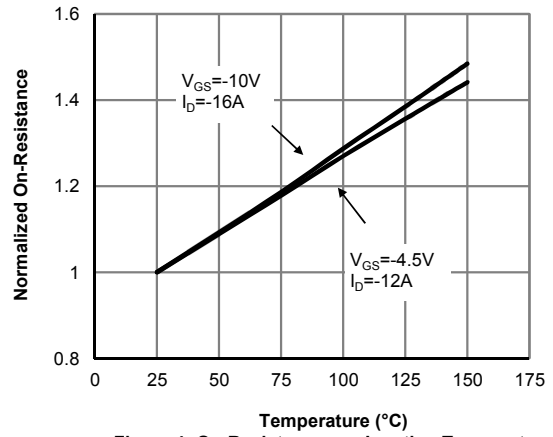


Figure 4: On-Resistance vs. Junction Temperature (Note E)

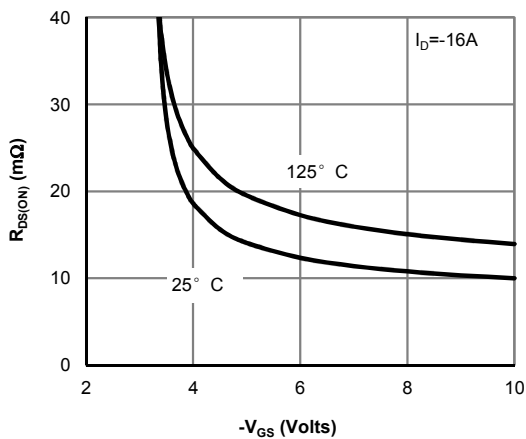


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

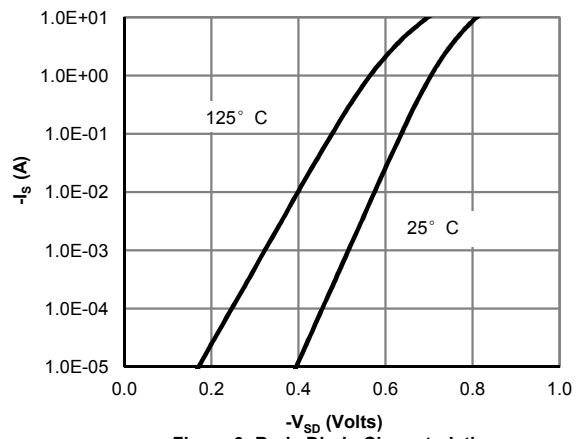


Figure 6: Body-Diode Characteristics (Note E)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

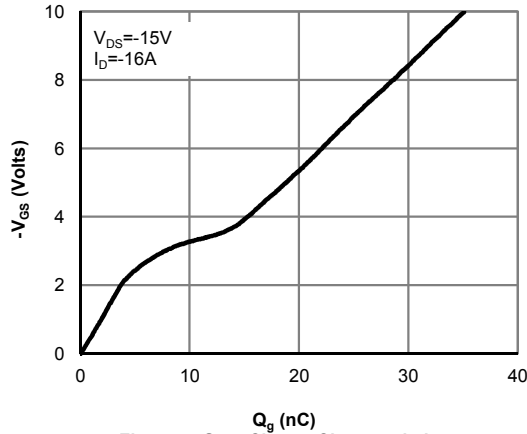


Figure 7: Gate-Charge Characteristics

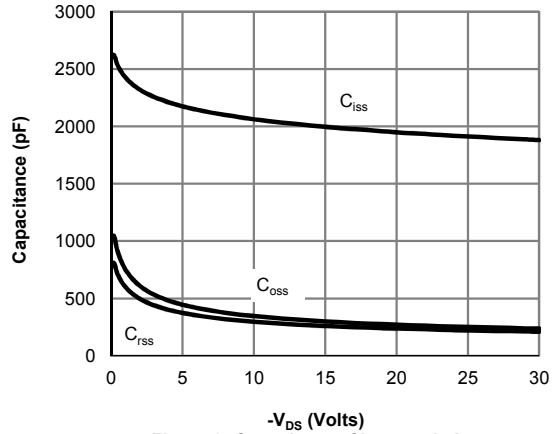


Figure 8: Capacitance Characteristics

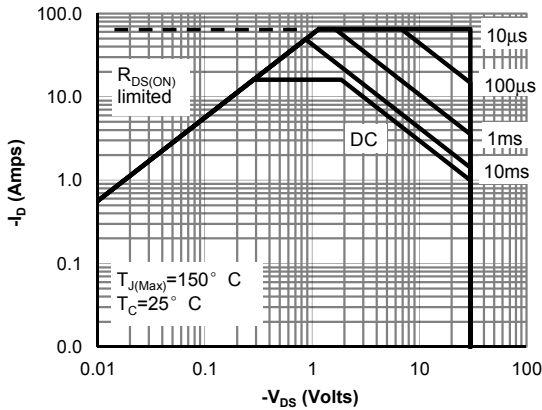


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

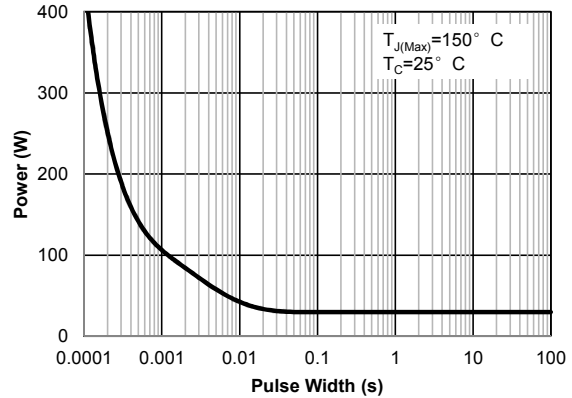


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

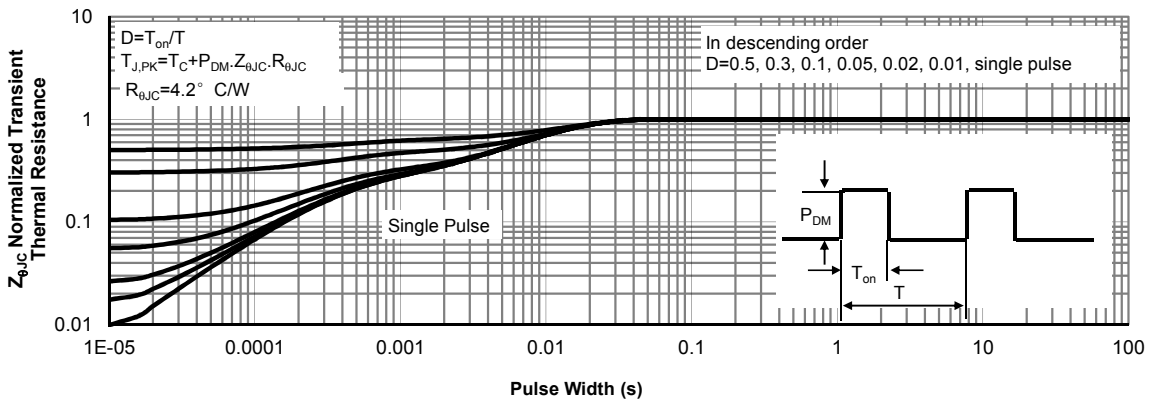


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

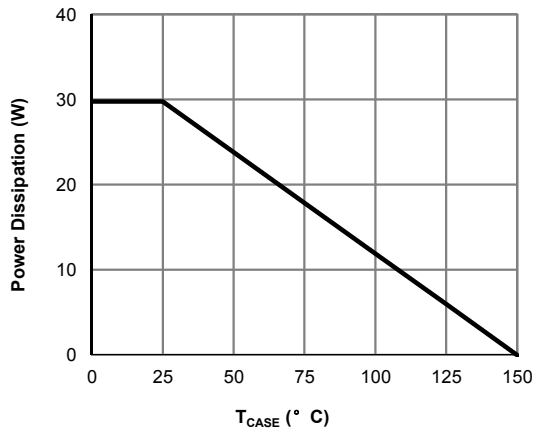


Figure 12: Power De-rating (Note F)

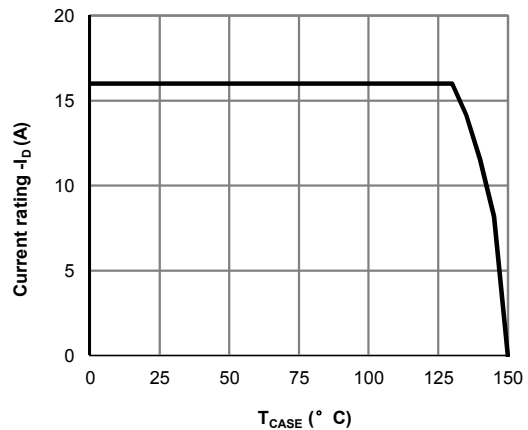


Figure 13: Current De-rating (Note F)

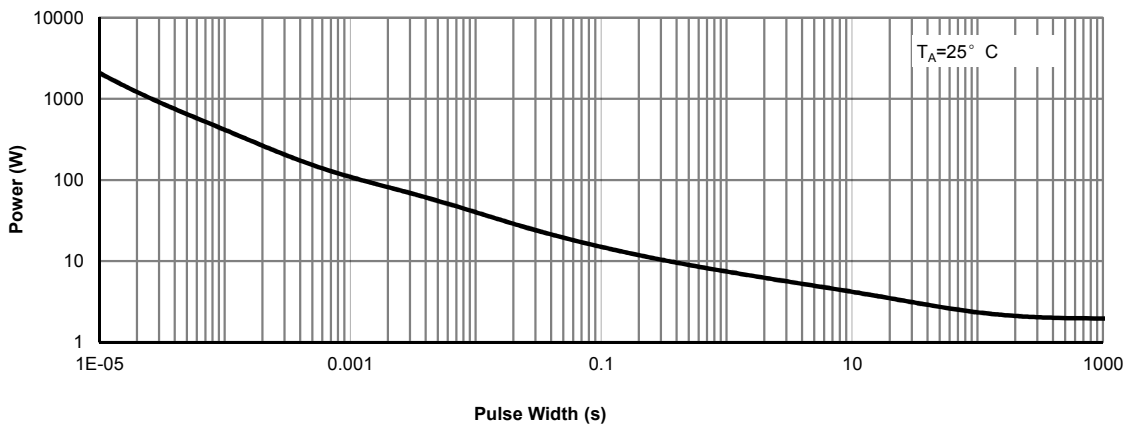


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

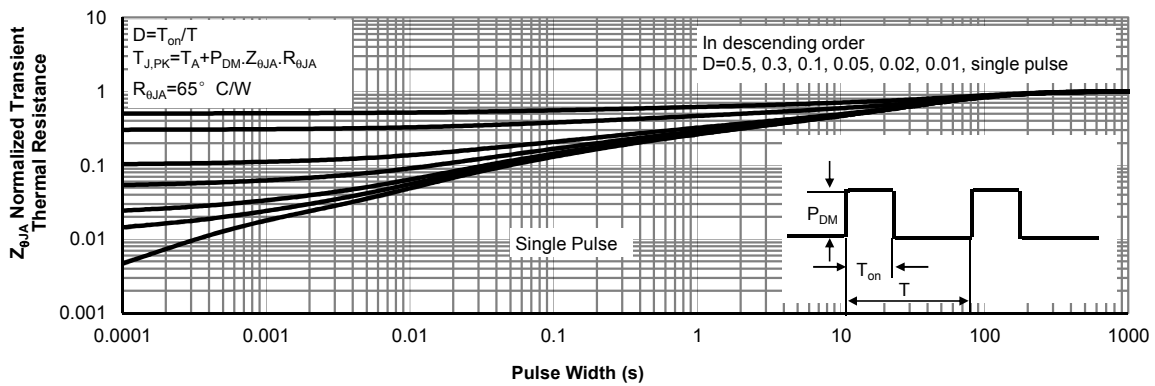


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

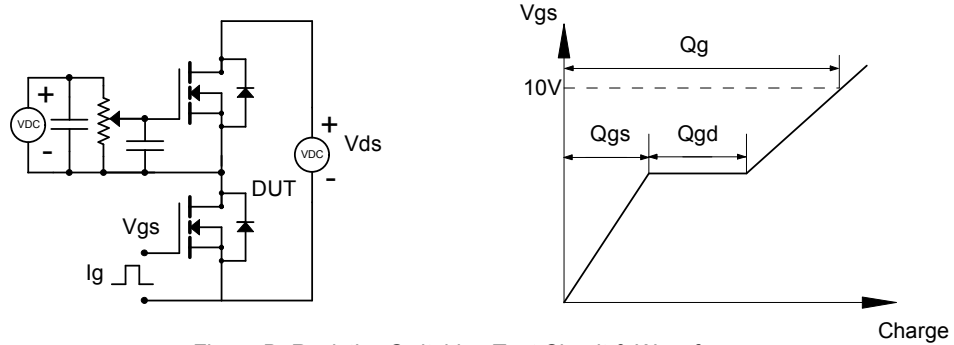


Figure B: Resistive Switching Test Circuit & Waveforms

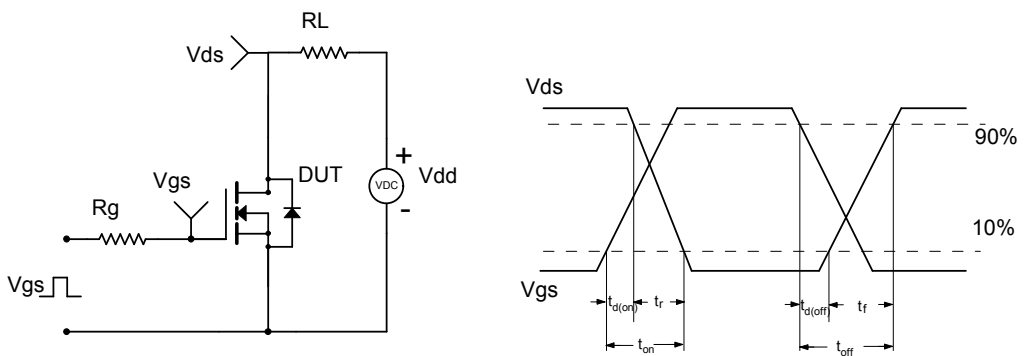


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

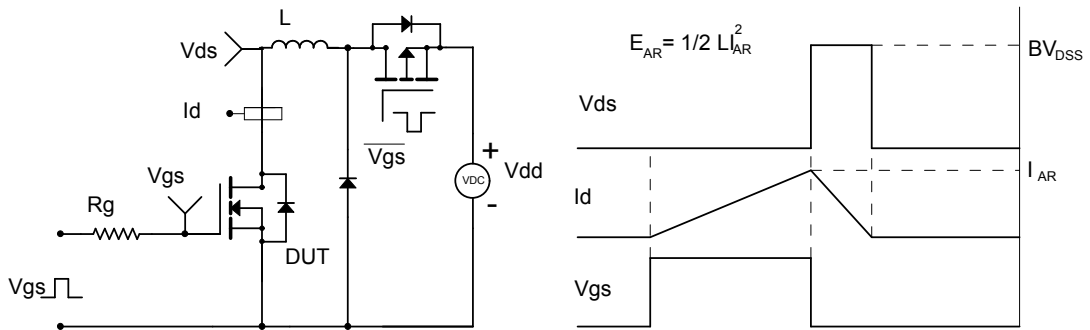
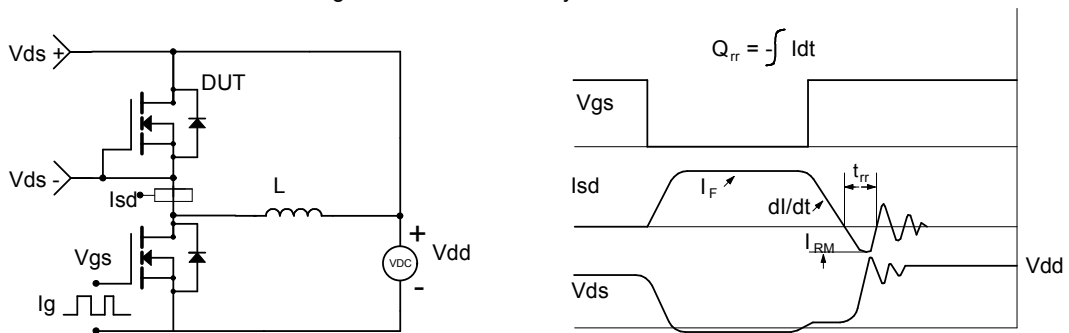
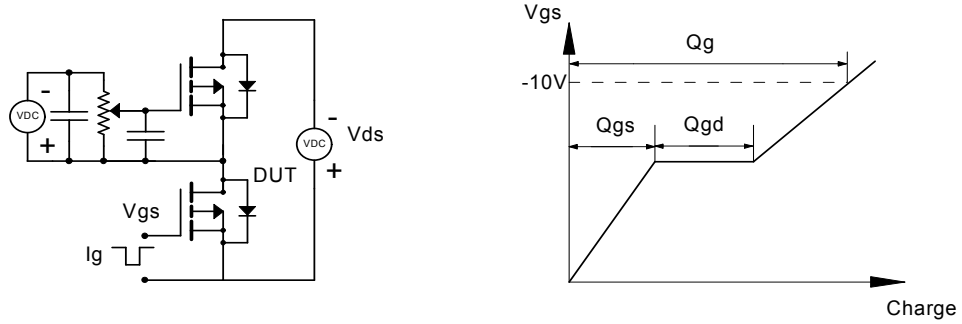


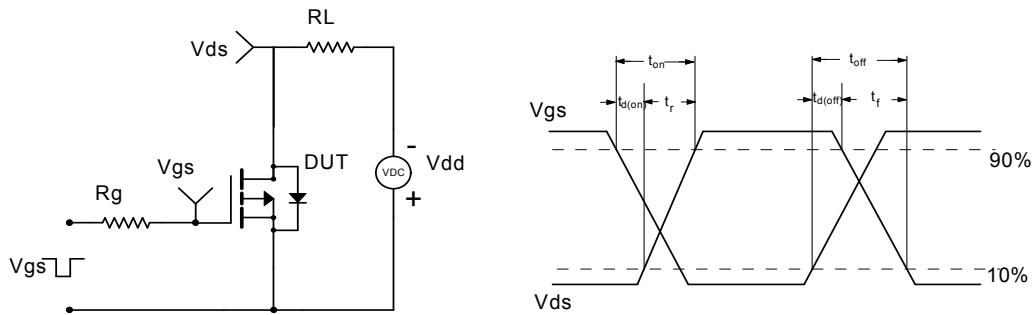
Figure D: Diode Recovery Test Circuit & Waveforms



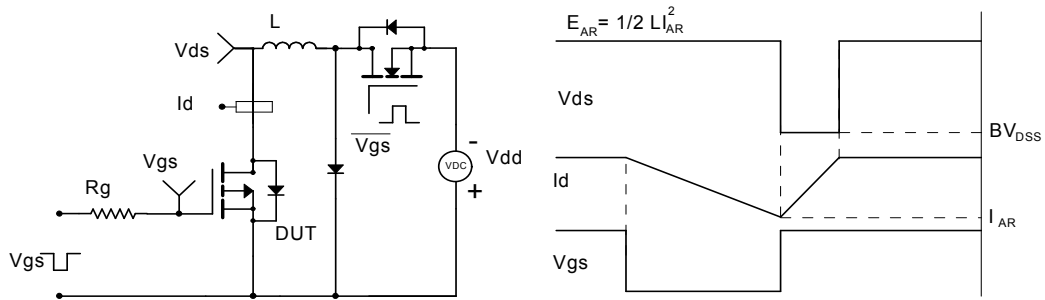
Gate Charge Test Circuit & Waveform



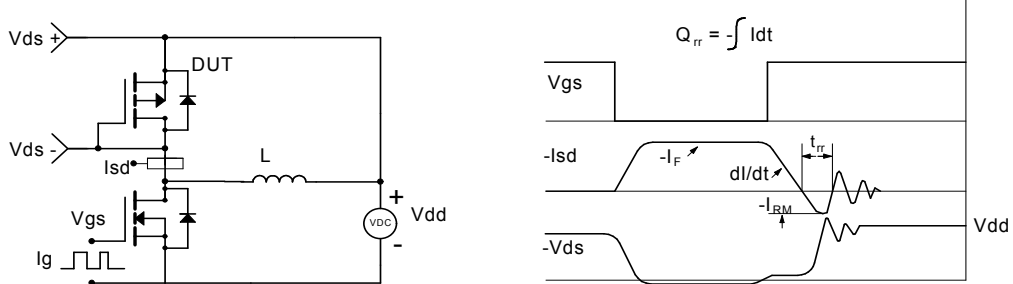
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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