AONE36132

25V Dual Asymmetric N-Channel MOSFET

General Description

- Bottom Source Technology
- Very Low $R_{DS(ON)}$
- High Current Capability
- RoHS and Halogen-Free Compliant

Applications

- DC/DC Converters in PC, Servers
- Point of load Converters

Product Summary

	Q1	Q2
V_{DS}	25V	25V
I_D (at V_{GS}=10V)	17A	34A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 4.6mΩ	< 1.4mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 6mΩ	< 1.7mΩ

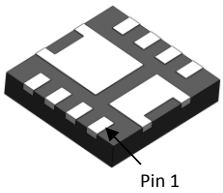
100% UIS Tested
100% Rg Tested

Green Product

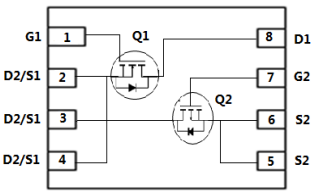
DFN3.3x3.3A

Top View

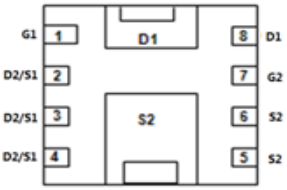
Bottom View



Top View



Transparent View



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONE36132	DFN3.3x3.3A	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	25	25	V
Gate-Source Voltage		V_{GS}	±12	±12	V
Continuous Drain Current	T_C=25°C	I_D	60[G]	60[G]	A
	T_C=100°C		38	60[G]	
Pulsed Drain Current [C]		I_{DM}	160	200	
Continuous Drain Current	T_A=25°C	I_{DSM}	17	34	A
	T_A=70°C		13.5	27	
Avalanche Current [C]		I_{AS}	48	60	A
Avalanche energy	L=0.01mH [C]	E_{AS}	12	18	mJ
Power Dissipation [B]	T_C=25°C	P_D	25	35.5	W
	T_C=100°C		10	14	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2	2.5	W
	T_A=70°C		1.3	1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	50	40	60	50	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		75	65	90	80	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	4	2.5	5	3.5	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=25V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1	1.4	1.8	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=17A		3.8	4.6	mΩ
		T_J=125°C		5.3	6.4	
		V_{GS}=4.5V, I_D=15A		4.8	6	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=17A		100		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				30	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=12.5V, f=1MHz		880		pF
C_{oss}	Output Capacitance			250		pF
C_{rss}	Reverse Transfer Capacitance			55		pF
R_g	Gate resistance	f=1MHz	0.35	0.7	1.05	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=12.5V, I_D=17A		14.5	21	nC
Q_g(4.5V)	Total Gate Charge			6.5	10	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			2.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=12.5V, R_L=0.75Ω, R_{GEN}=3Ω		4.5		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(off)}$	Turn-Off DelayTime			20		ns
t_f	Turn-Off Fall Time			2.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=17A, di/dt=500A/µs		9		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=17A, di/dt=500A/µs		11.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

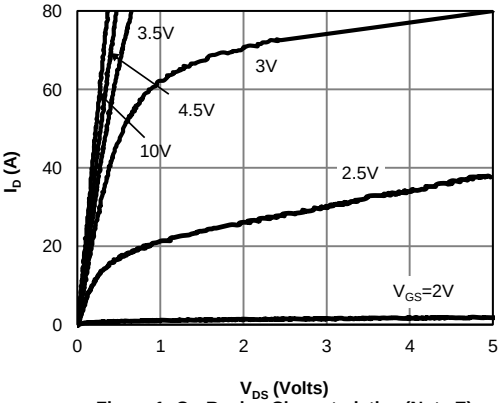


Figure 1: On-Region Characteristics (Note E)

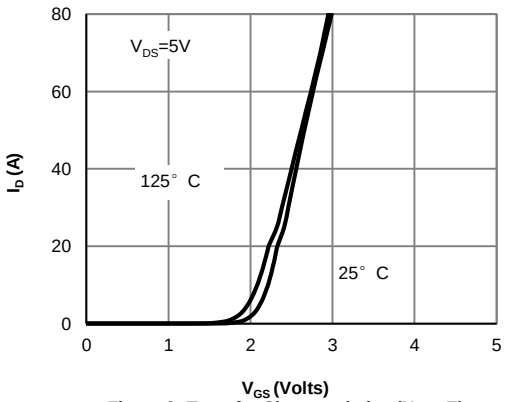


Figure 2: Transfer Characteristics (Note E)

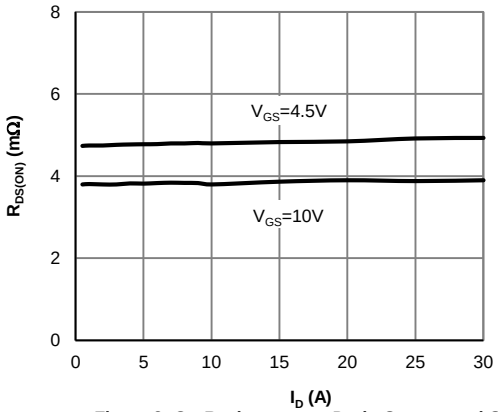


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

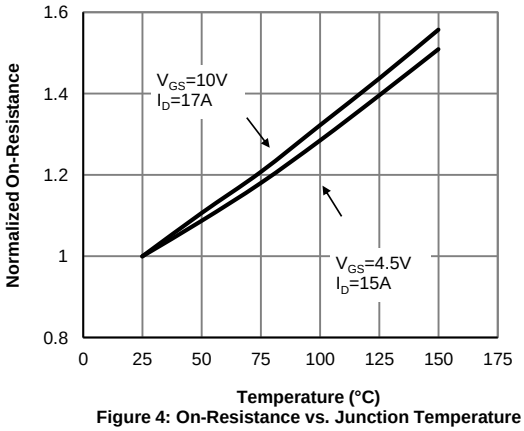


Figure 4: On-Resistance vs. Junction Temperature (Note E)

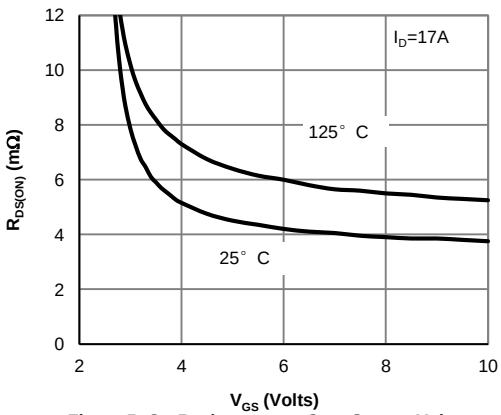


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

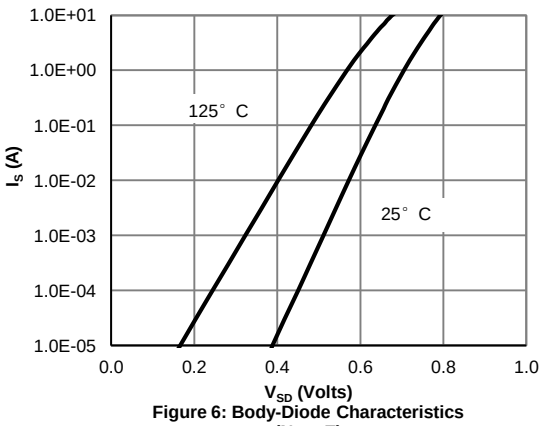


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

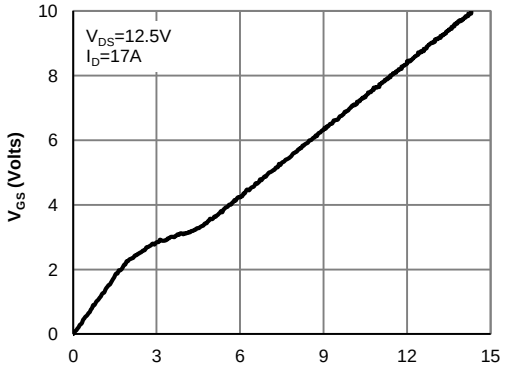


Figure 7: Gate-Charge Characteristics

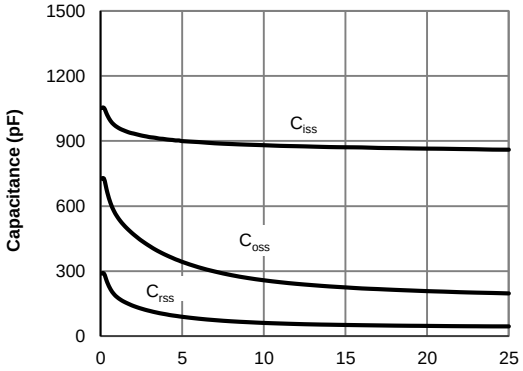


Figure 8: Capacitance Characteristics

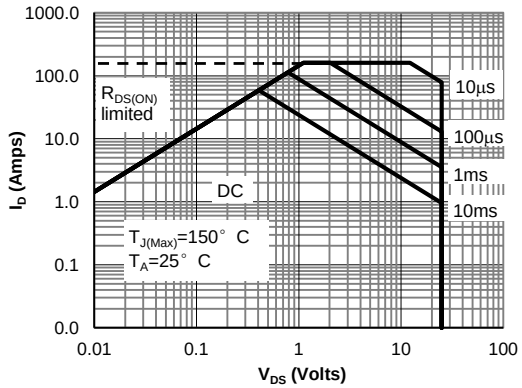


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

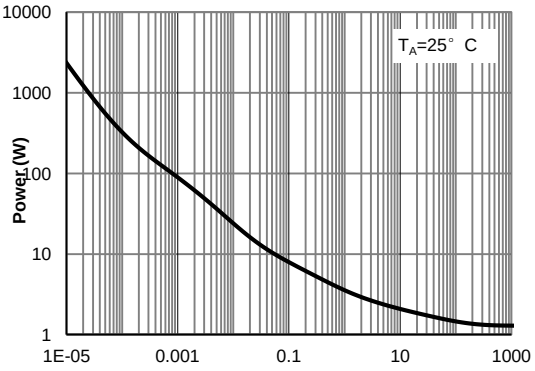


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

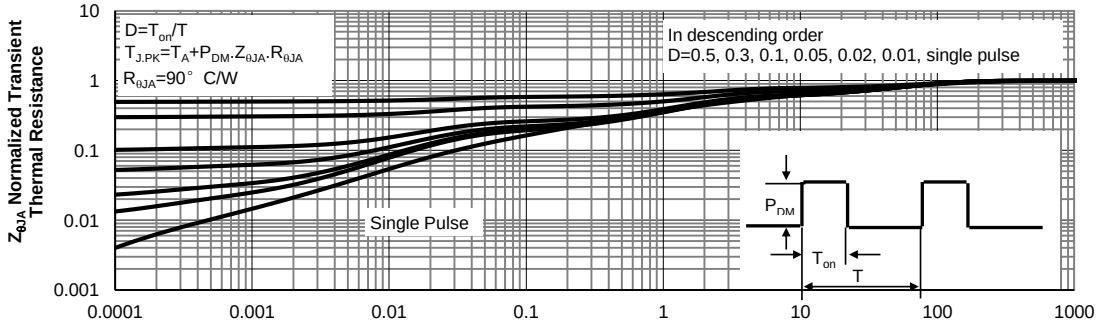


Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=25V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1	1.4	1.8	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		1.1	1.4	mΩ
		T_J=125°C		1.5	1.9	
		V_{GS}=4.5V, I_D=20A		1.3	1.7	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		165		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=12.5V, f=1MHz		3215		pF
C_{oss}	Output Capacitance			860		pF
C_{rss}	Reverse Transfer Capacitance			200		pF
R_g	Gate resistance	f=1MHz	0.4	0.8	1.2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=12.5V, I_D=20A		55	80	nC
Q_g(4.5V)	Total Gate Charge			25	35	nC
Q_{gs}	Gate Source Charge			9.5		nC
Q_{gd}	Gate Drain Charge			5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=12.5V, R_L=0.6Ω, R_{GEN}=3Ω		8		ns
t_r	Turn-On Rise Time			5.5		ns
$t_{D(off)}$	Turn-Off DelayTime			39.5		ns
t_f	Turn-Off Fall Time			7		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, di/dt=500A/µs		16		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=500A/µs		33.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

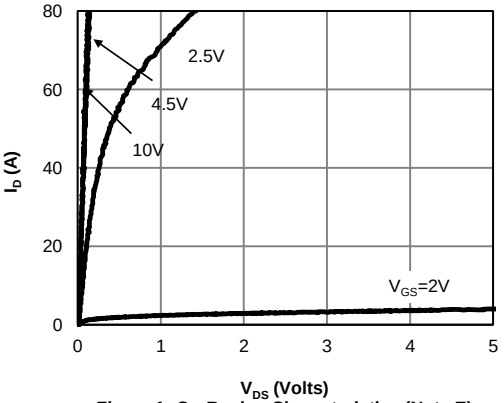


Figure 1: On-Region Characteristics (Note E)

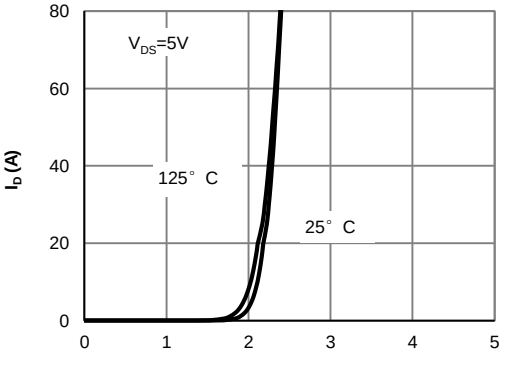


Figure 2: Transfer Characteristics (Note E)

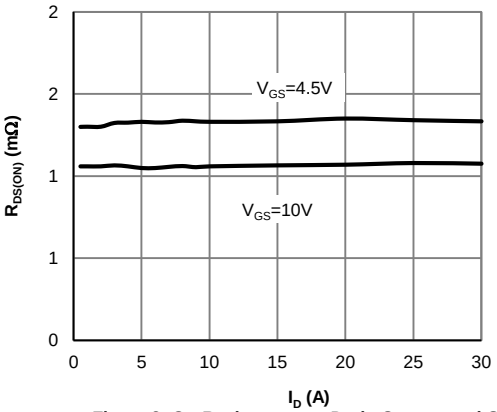


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

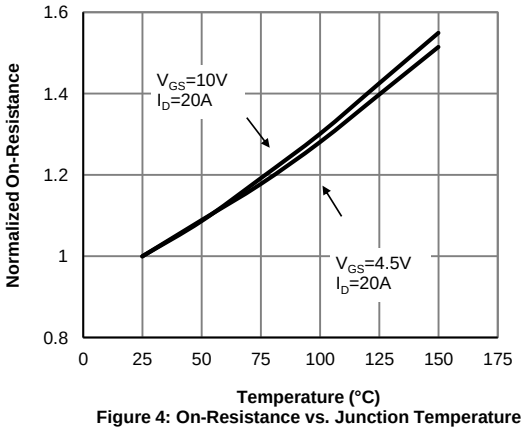


Figure 4: On-Resistance vs. Junction Temperature (Note E)

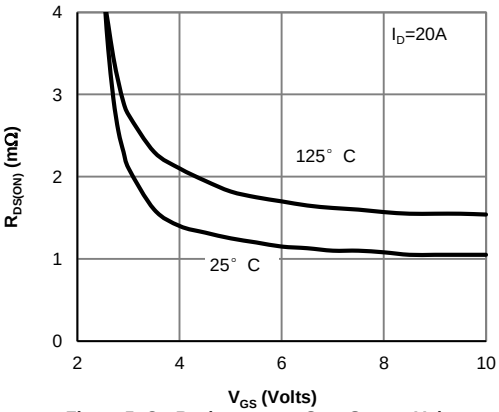


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

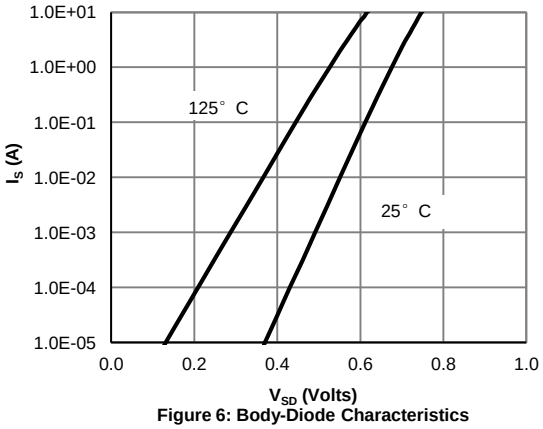


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

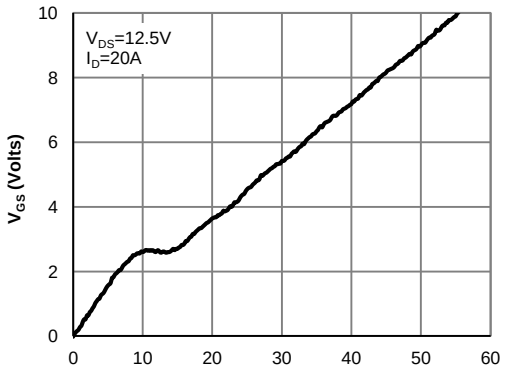


Figure 7: Gate-Charge Characteristics

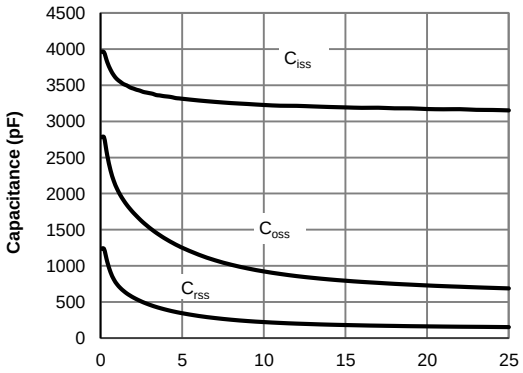


Figure 8: Capacitance Characteristics

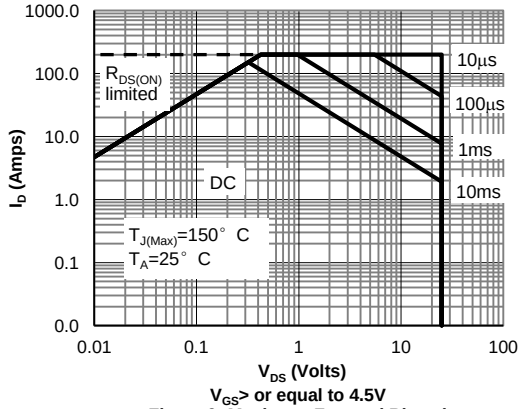


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

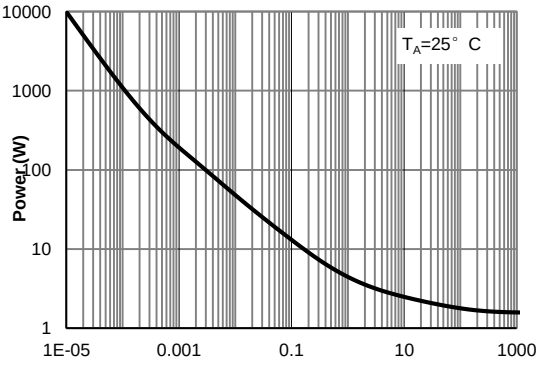


Figure 13: Single Pulse Power Rating Junction-to-Ambient (Note H)

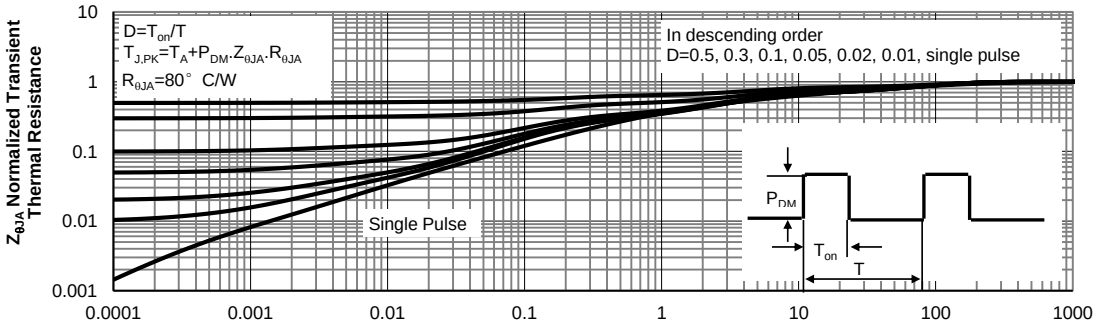


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

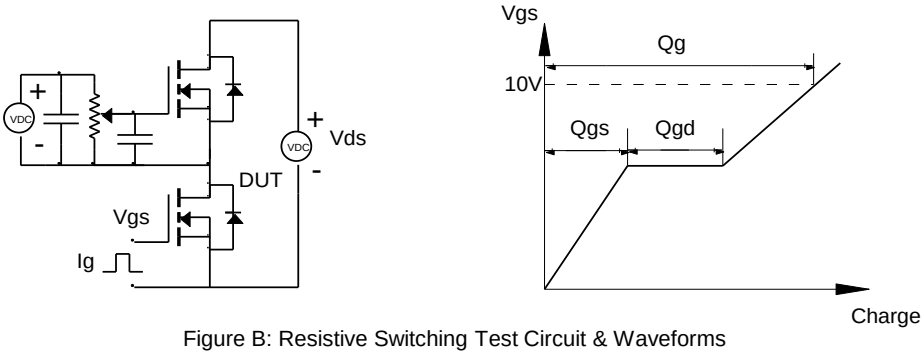


Figure B: Resistive Switching Test Circuit & Waveforms

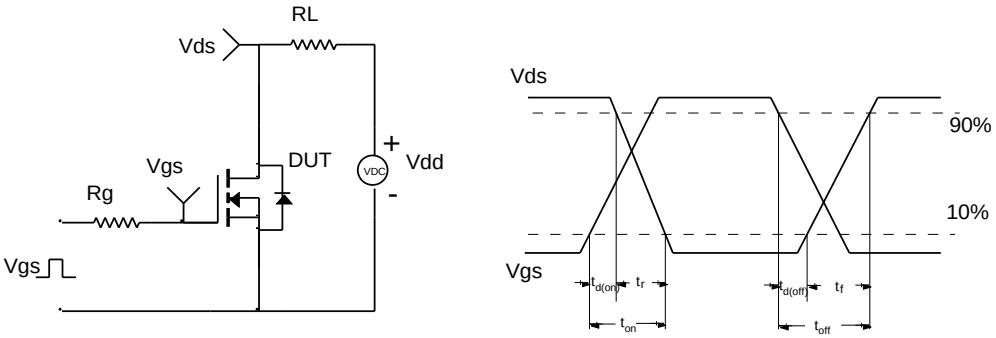


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

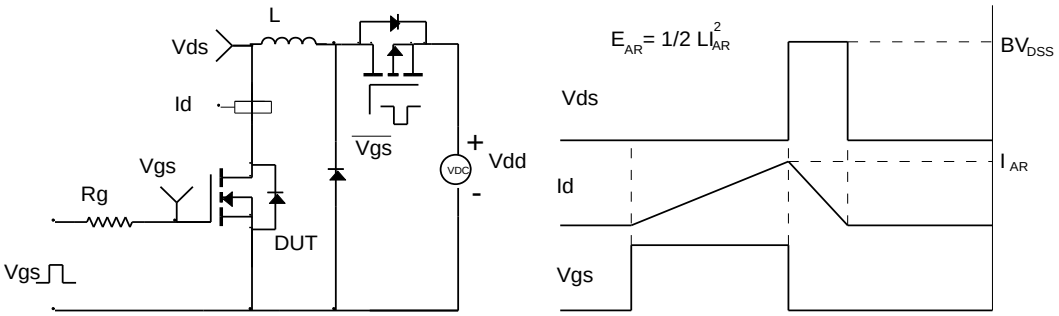


Figure D: Diode Recovery Test Circuit & Waveforms