

**General Description**

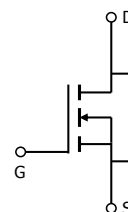
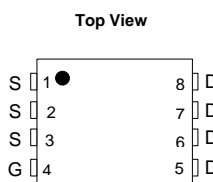
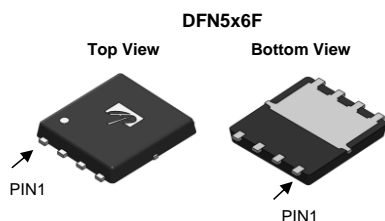
- Proprietary  $\alpha$ MOS5™ technology
- Low  $R_{DS(ON)}$
- Optimized switching parameters for better EMI performance
- Enhanced body diode for robustness and fast reverse recovery

**Applications**

- SMPS with PFC, Flyback and LLC topologies
- Silver ATX, adapter, TV, lighting, Server power

**Product Summary**

$V_{DS} @ T_{j,max}$	700V
$I_{DM}$	44A
$R_{DS(ON),max}$	< 0.42 $\Omega$
$Q_{g,typ}$	18nC
$E_{oss} @ 400V$	2.6 $\mu$ J

 100% UIS Tested  
 100%  $R_g$  Tested


Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS420A60	DFN5x6F	Tape & Reel	3000

**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Gate-Source Voltage (dynamic) AC ( $f > 1\text{Hz}$ )	$V_{GS}$	$\pm 30$	V
Continuous Drain Current	$T_C=25^\circ\text{C}$	11	A
	$T_C=100^\circ\text{C}$	8.3	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	44	
Continuous Drain Current	$T_A=25^\circ\text{C}$	2.2	A
	$T_A=70^\circ\text{C}$	1.8	
Avalanche Current <sup>C</sup>	$I_{AR}$	2.5	A
Repetitive avalanche energy <sup>C</sup>	$E_{AR}$	3.1	mJ
Single pulsed avalanche energy <sup>G</sup> ( $T_J=25^\circ\text{C}$ , $V_{GS}=10\text{V}$ , $I_L=2\text{A}$ , $L=105\text{mH}$ , $R_{GS}=25\Omega$ )	$E_{AS}$	210	mJ
MOSFET dv/dt ruggedness	dv/dt	100	V/ns
Diode reverse recovery	dv/dt	20	V/ns
$V_{DS}=0$ to $400\text{V}$ , $I_F \leq 10\text{A}$ , $T_J=25^\circ\text{C}$	di/dt	100	A/us
Power Dissipation <sup>B</sup>	$T_C=25^\circ\text{C}$	156	W
	Derate above $25^\circ\text{C}$	1.3	W/ $^\circ\text{C}$
Power Dissipation <sup>A</sup>	$T_A=25^\circ\text{C}$	4.2	W
	$T_A=70^\circ\text{C}$	2.7	W/ $^\circ\text{C}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	25	30	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	45	55
Maximum Junction-to-Case	$R_{\theta JC}$	0.5	0.8	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	600			V
		I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C		700		
BV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V		0.5		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =480V, T <sub>J</sub> =125°C			10	
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA		3.2		V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =5.5A		0.38	0.42	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =5.5A		9.3		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =5.5A, V <sub>GS</sub> =0V		0.86	1.2	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				11	A
I <sub>SM</sub>	Maximum Body-Diode Pulsed Current <sup>C</sup>				44	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz		955		pF
C <sub>oss</sub>	Output Capacitance			29		pF
C <sub>o(er)</sub>	Effective output capacitance, energy related <sup>I</sup>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0 to 480V, f=1MHz		30		pF
C <sub>o(tr)</sub>	Effective output capacitance, time related <sup>J</sup>			122		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz		2.4		pF
R <sub>g</sub>	Gate resistance	f=1MHz		4.8		Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =480V, I <sub>D</sub> =5.5A		18		nC
Q <sub>gs</sub>	Gate Source Charge			7		nC
Q <sub>gd</sub>	Gate Drain Charge			4.5		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =400V, I <sub>D</sub> =5.5A, R <sub>G</sub> =5Ω		20		ns
t <sub>r</sub>	Turn-On Rise Time			13		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			43		ns
t <sub>f</sub>	Turn-Off Fall Time			16		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time			251		ns
I <sub>rm</sub>	Peak Reverse Recovery Current	I <sub>F</sub> =5.5A, di/dt=100A/μs, V <sub>DS</sub> =400V		19		A
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge			3.1		μC

A. The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> t<sub>s</sub> ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I<sub>AS</sub>=1A, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25°C.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

I. C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

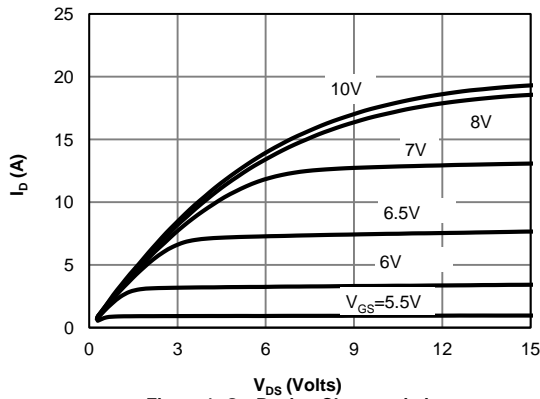
J. C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

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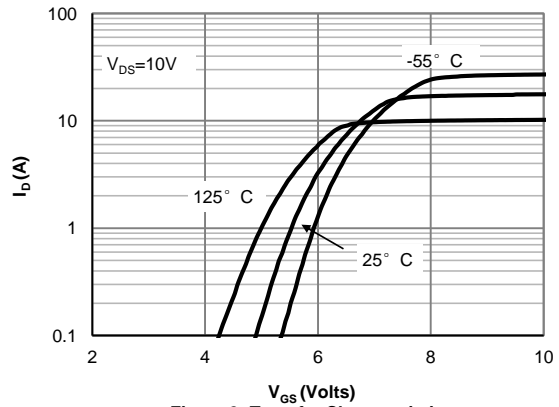
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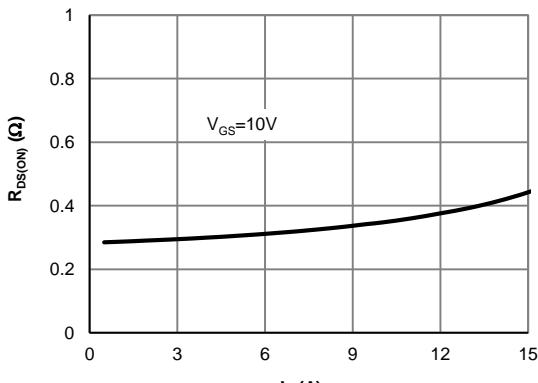
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



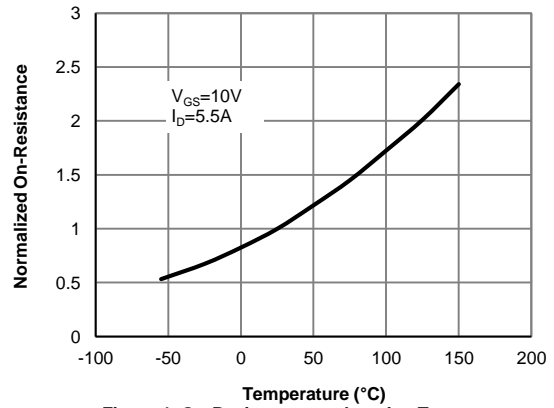
**Figure 1: On-Region Characteristics**



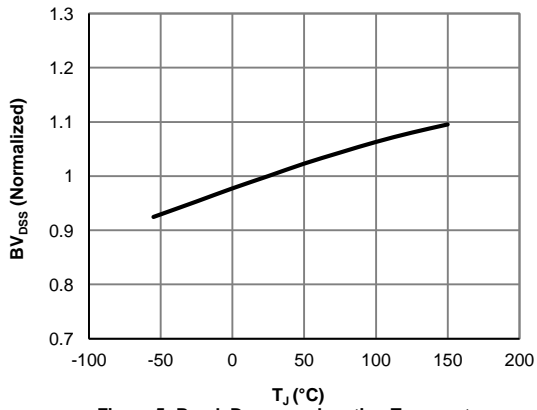
**Figure 2: Transfer Characteristics**



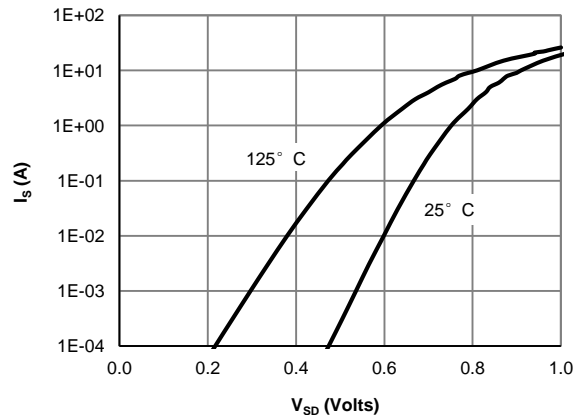
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**

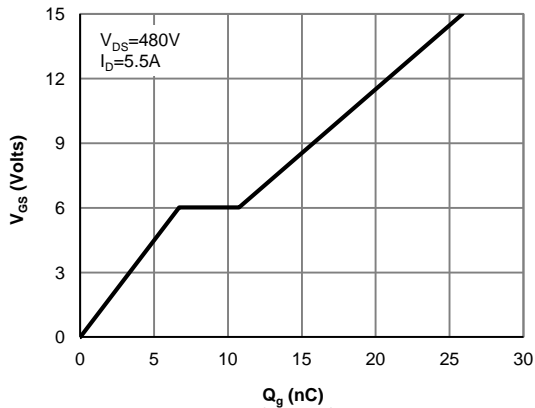


**Figure 5: Break Down vs. Junction Temperature**

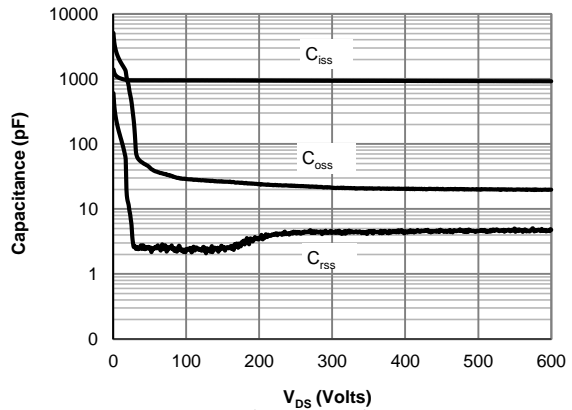


**Figure 6: Body-Diode Characteristics**

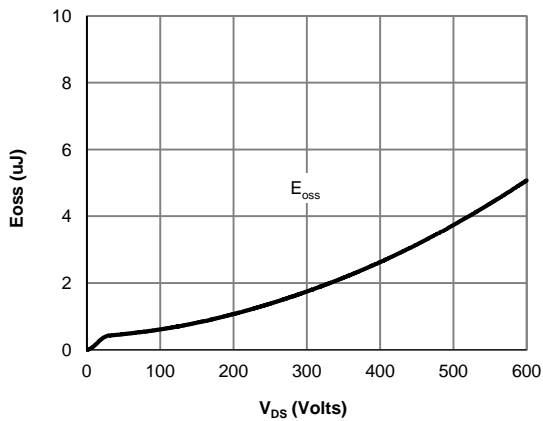
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



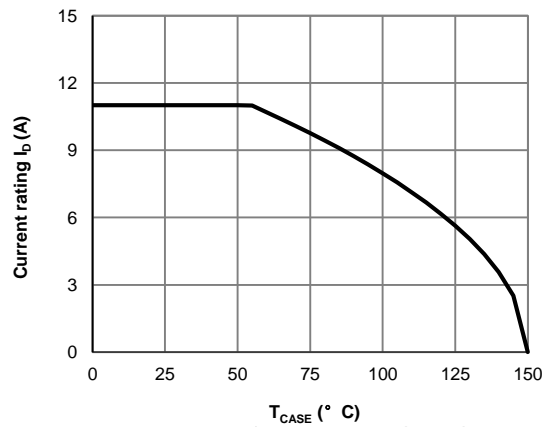
**Figure 7: Gate-Charge Characteristics**



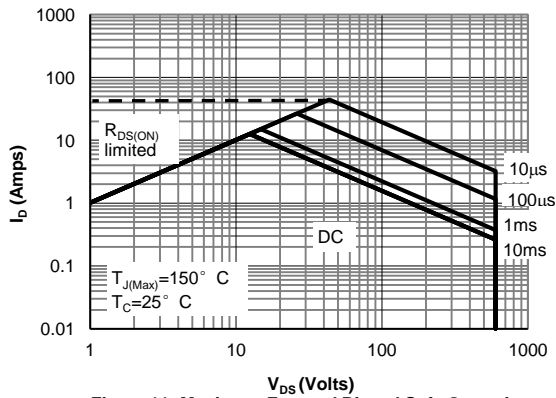
**Figure 8: Capacitance Characteristics**



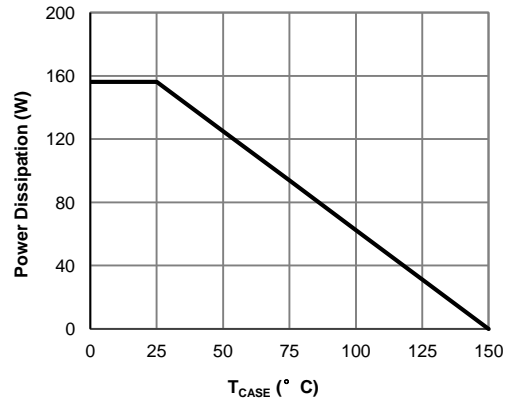
**Figure 9: Coss stored Energy**



**Figure 10: Current De-rating (Note F)**

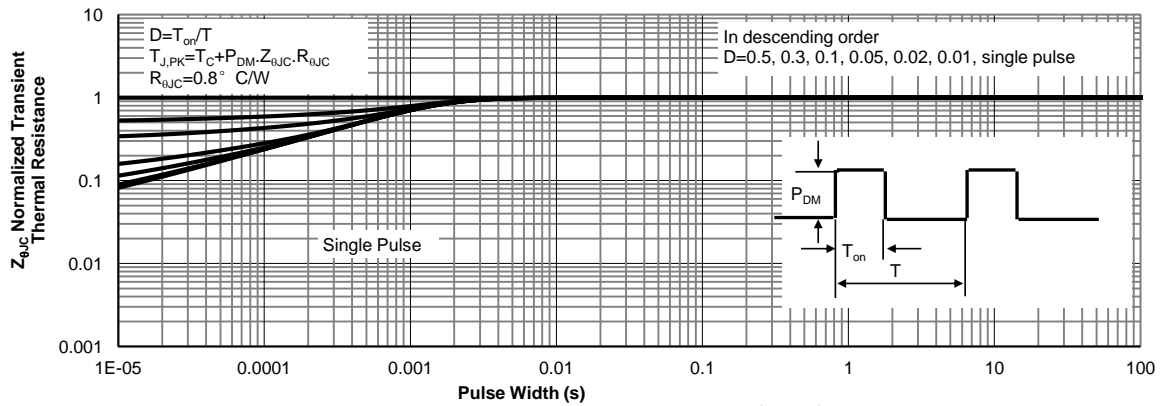


**Figure 11: Maximum Forward Biased Safe Operating Area (Note F)**

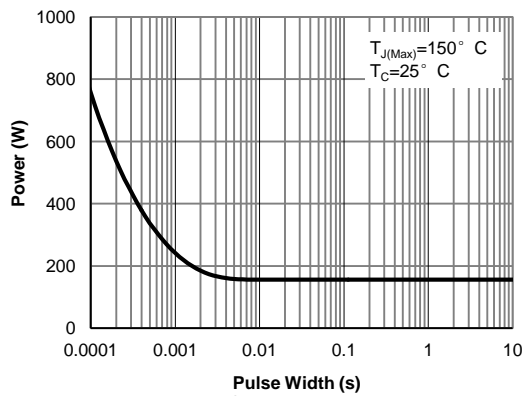


**Figure 12: Power De-rating (Note F)**

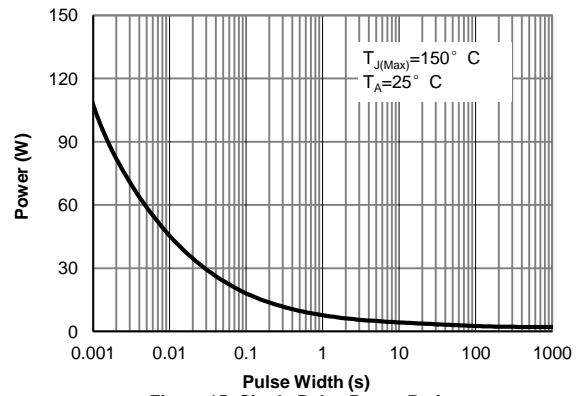
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



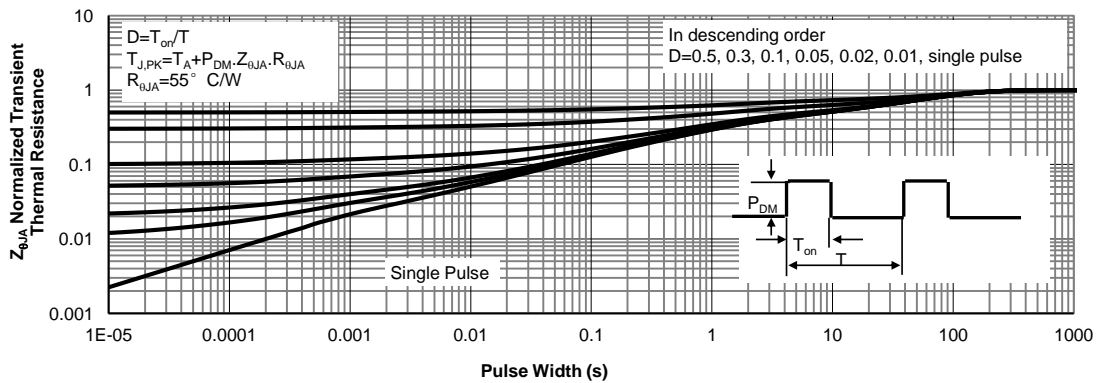
**Figure 13: Normalized Maximum Transient Thermal Impedance (Note F)**



**Figure 14: Single Pulse Power Rating Junction-to-Case (Note F)**

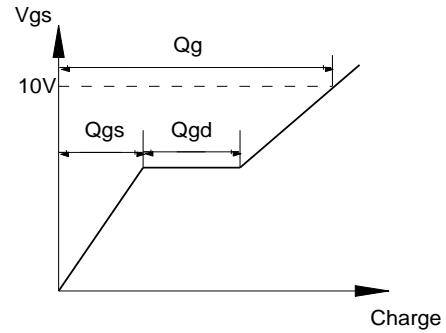


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

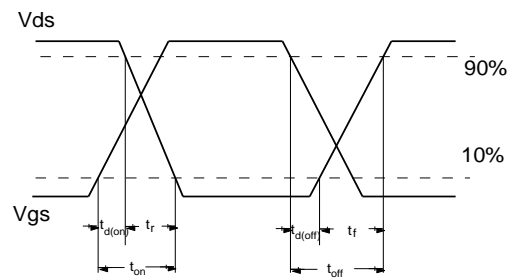
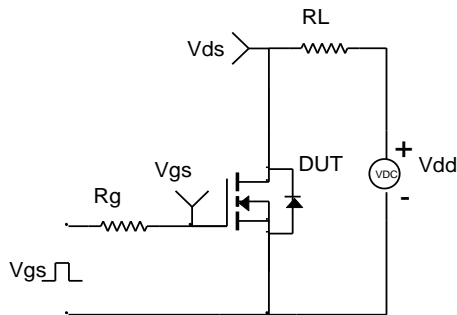


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

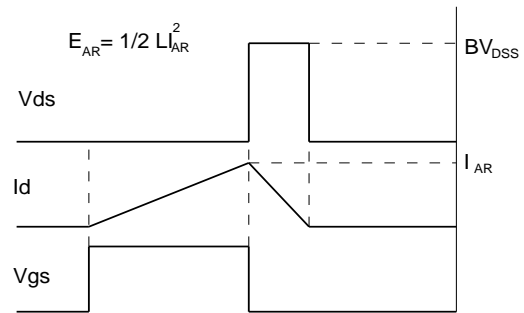
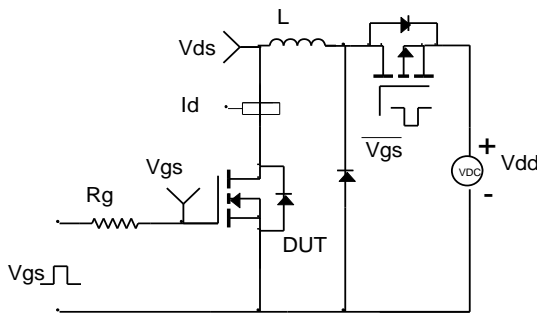
Gate Charge Test Circuit & Waveform



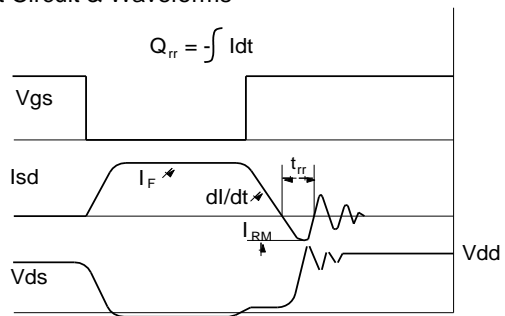
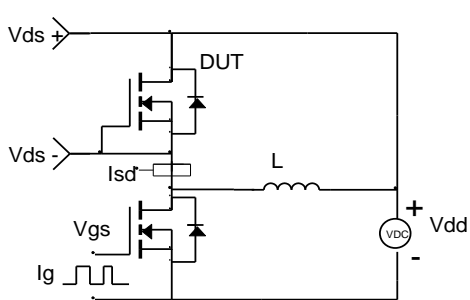
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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