

General Description

- Trench Power AlphaSGT™ technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- Low Eoss

Applications

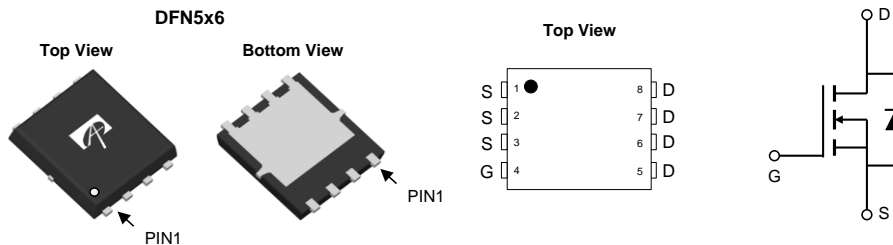
- Secondary Synchronous Rectification MOSFET for Server and Telecom

Product Summary

V_{DS}	80V
I_D (at $V_{GS}=10V$)	100A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 2.6m Ω
$R_{DS(ON)}$ (at $V_{GS}=6V$)	< 3.5m Ω

100% UIS Tested
 100% Rg Tested

Max Tj=175°C



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS62814T	DFN 5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	372	
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	33
Avalanche Current ^C	I_{AS}	73	A
Avalanche energy	E_{AS}	266	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	258
		$T_C=100^\circ\text{C}$	129
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	8.8
		$T_A=70^\circ\text{C}$	6.1
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	14	17	°C/W
Maximum Junction-to-Ambient ^{A,D}		Steady-State	40	50
Maximum Junction-to-Case	$R_{\theta JC}$	0.43	0.58	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	80			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.1	2.6	3.2	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		2.2	2.6	mΩ
		V _{GS} =6V, I _D =20A		3.7	4.5	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		100		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.68	1	V
I _S	Maximum Body-Diode Continuous Current ^G				100	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =40V, f=1MHz		4940		pF
C _{oss}	Output Capacitance			770		pF
C _{riss}	Reverse Transfer Capacitance			40		pF
R _g	Gate resistance	f=1MHz	0.3	0.7	1.2	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =40V, I _D =20A		68	100	nC
Q _{gs}	Gate Source Charge			14.5		nC
Q _{gd}	Gate Drain Charge			14		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =40V, R _L =2.0Ω, R _{GEN} =3Ω		14		ns
t _r	Turn-On Rise Time			8.5		ns
t _{D(off)}	Turn-Off DelayTime			40		ns
t _f	Turn-Off Fall Time			10		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		32		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		168		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=175° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO MAKE CHANGES TO PRODUCT SPECIFICATIONS WITHOUT NOTICE. IT IS THE RESPONSIBILITY OF THE CUSTOMER TO EVALUATE SUITABILITY OF THE PRODUCT FOR THEIR INTENDED APPLICATION. CUSTOMER SHALL COMPLY WITH APPLICABLE LEGAL REQUIREMENTS, INCLUDING ALL APPLICABLE EXPORT CONTROL RULES, REGULATIONS AND LIMITATIONS.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:

http://www.aosmd.com/terms_and_conditions_of_sale

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

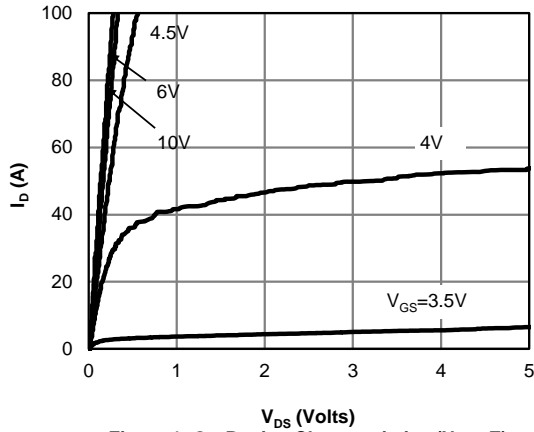


Figure 1: On-Region Characteristics (Note E)

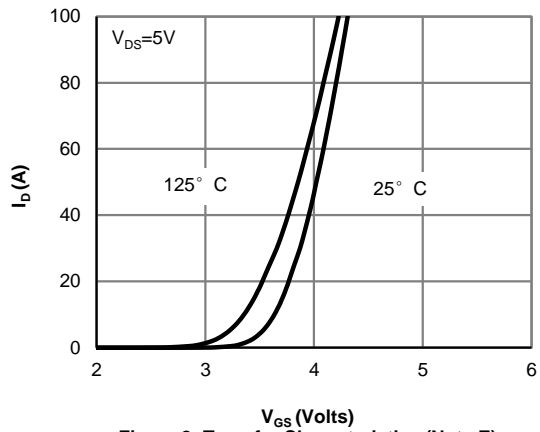


Figure 2: Transfer Characteristics (Note E)

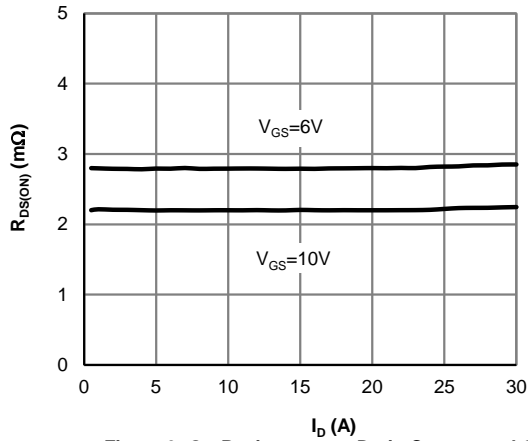


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

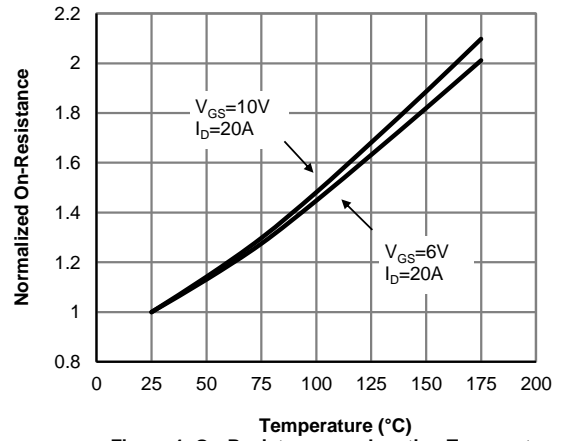


Figure 4: On-Resistance vs. Junction Temperature (Note E)

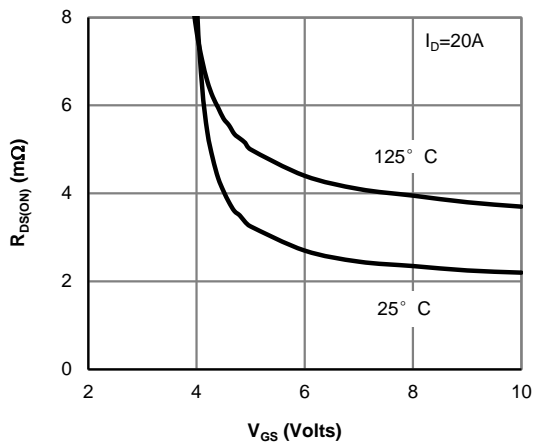


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

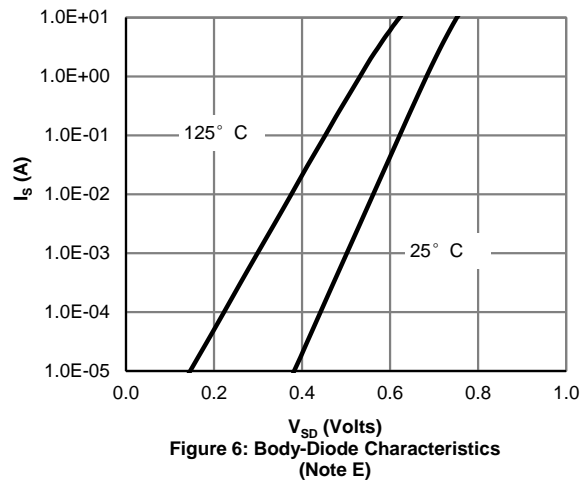


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

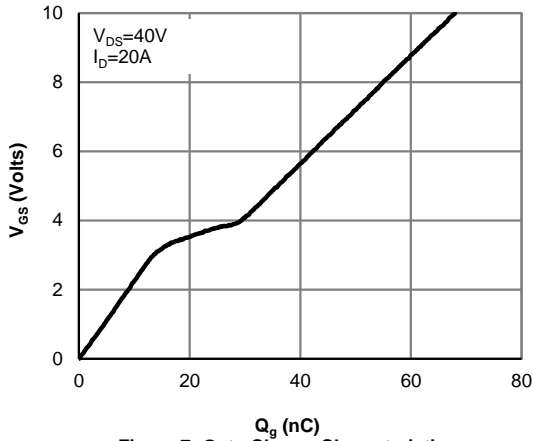


Figure 7: Gate-Charge Characteristics

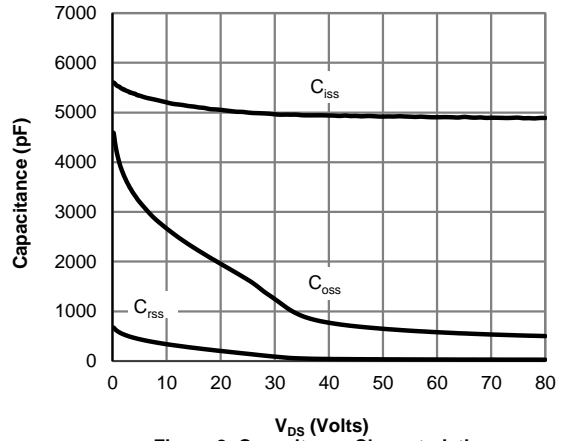


Figure 8: Capacitance Characteristics

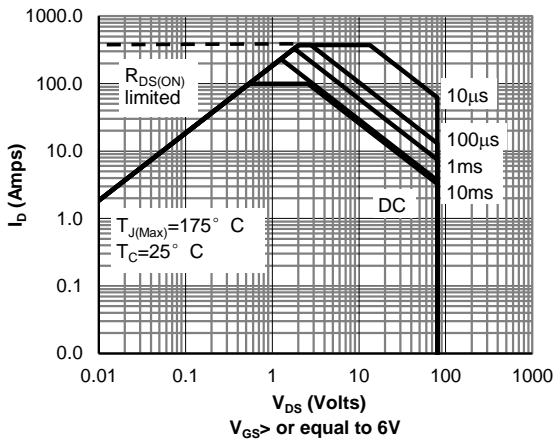


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

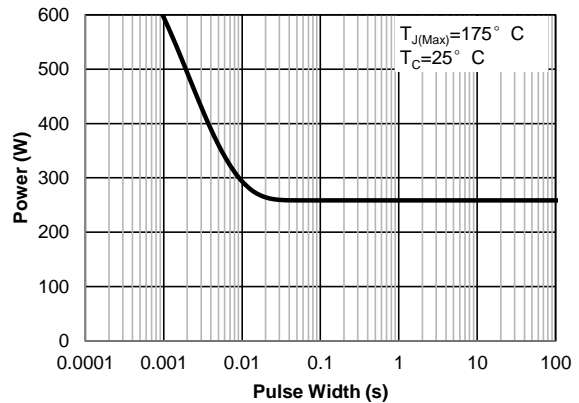


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

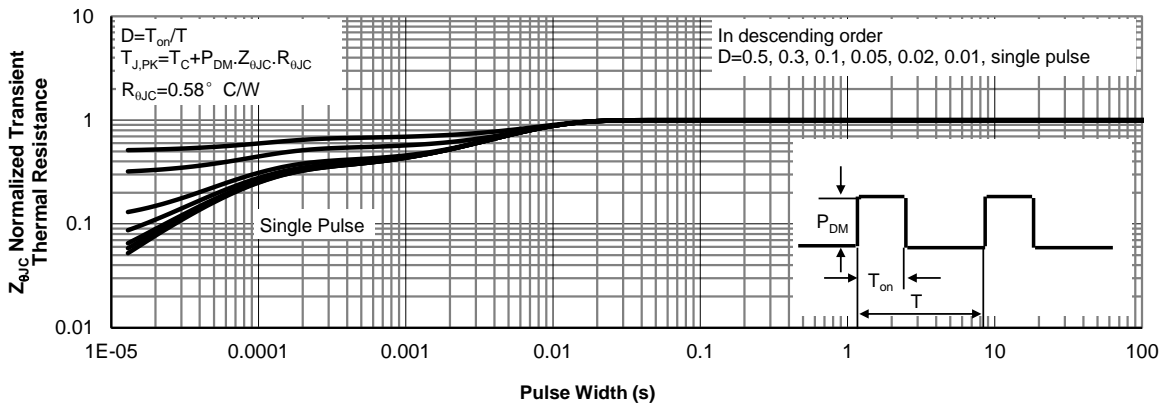


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

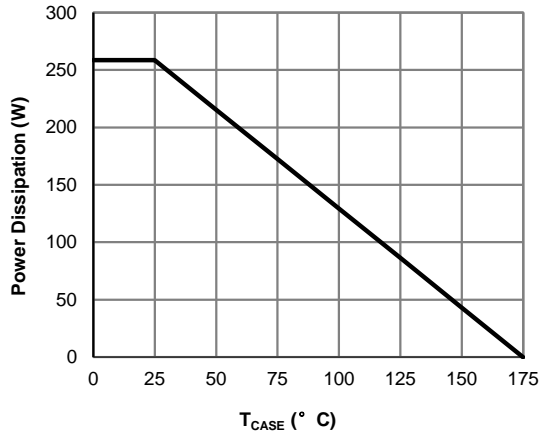


Figure 12: Power De-rating (Note F)

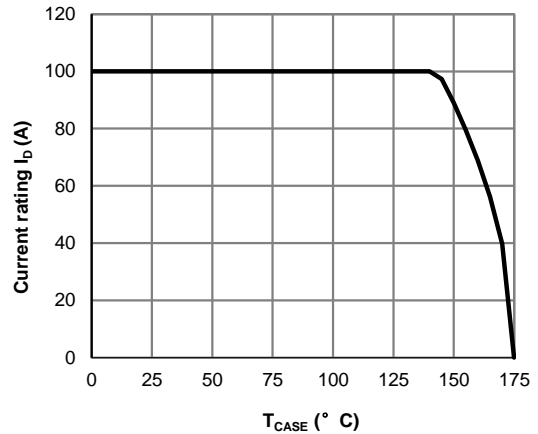


Figure 13: Current De-rating (Note F)

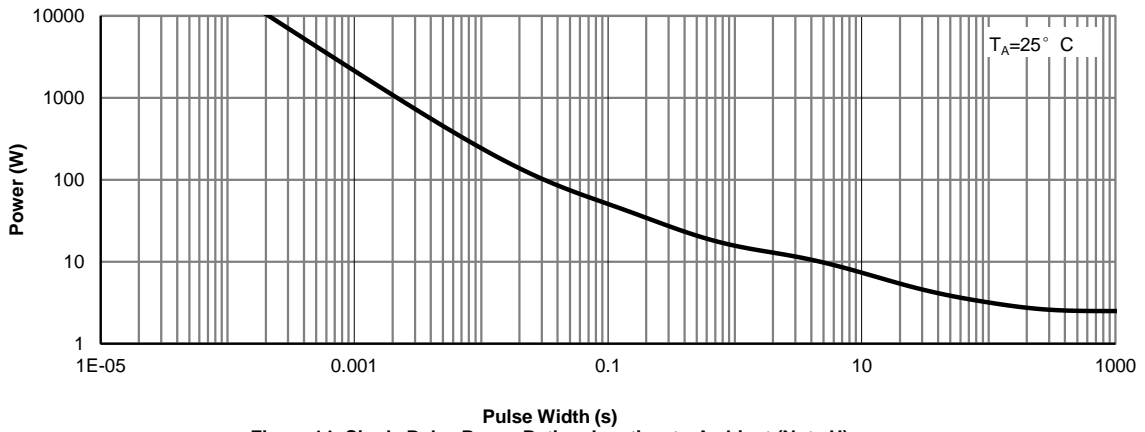


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

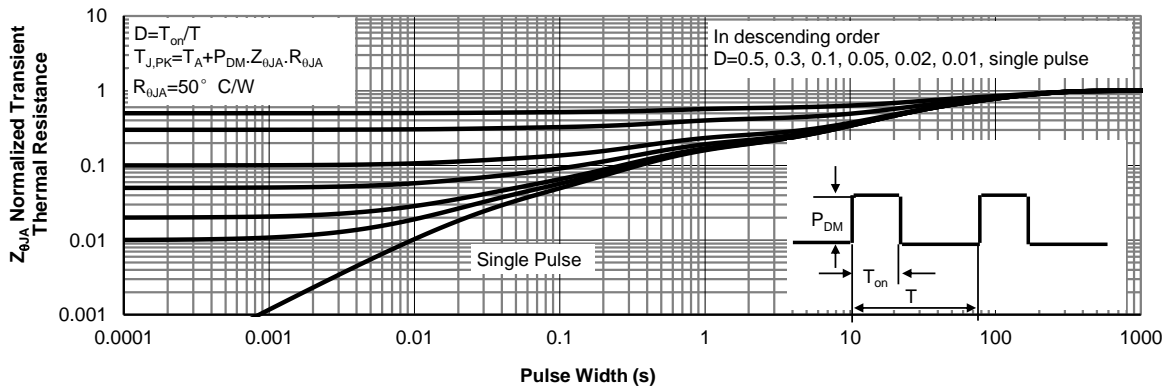


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

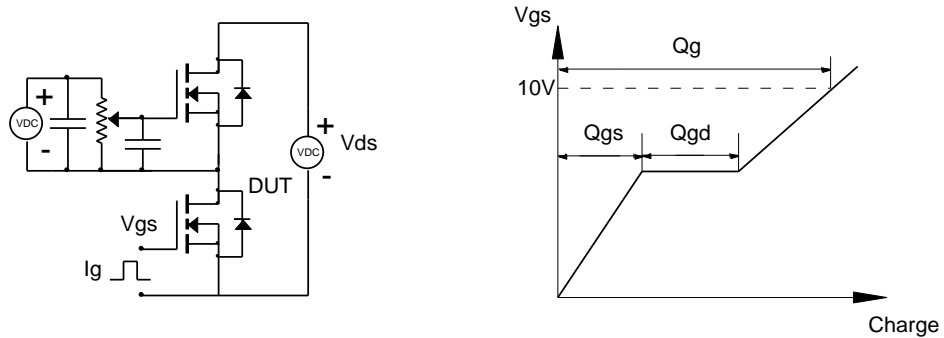


Figure B: Resistive Switching Test Circuit & Waveforms

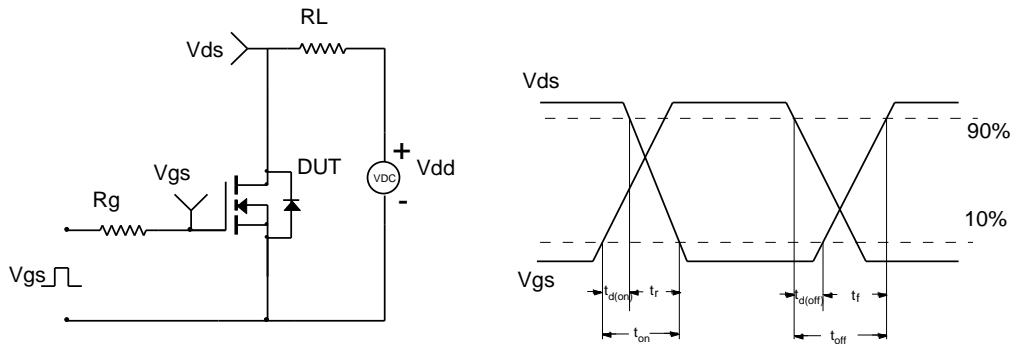


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

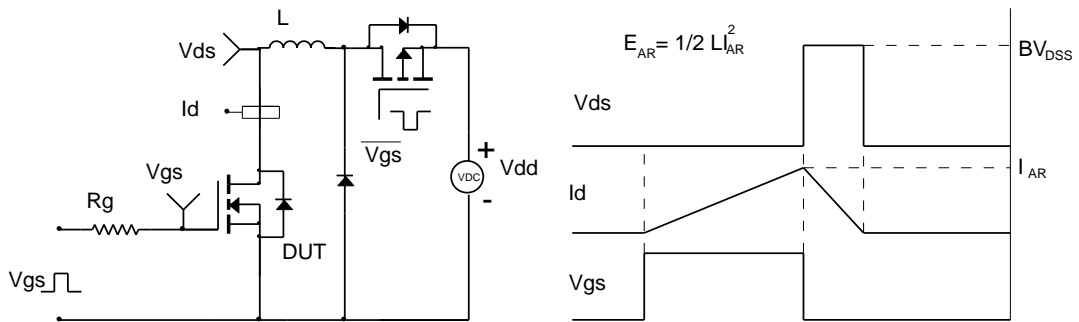
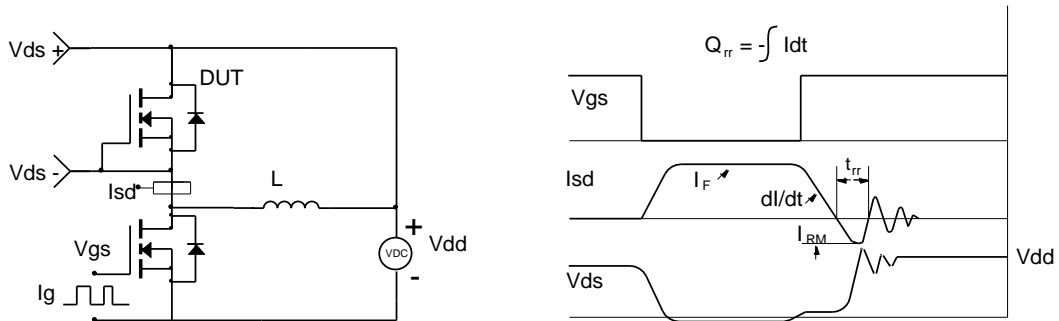


Figure D: Diode Recovery Test Circuit & Waveforms



单击下面可查看定价，库存，交付和生命周期等信息

[>>AOS\(万代\)](#)